Impact of Stray Inductance on EliteSiC Power and VE-Trac™ IGBT Module's Switching Characteristics

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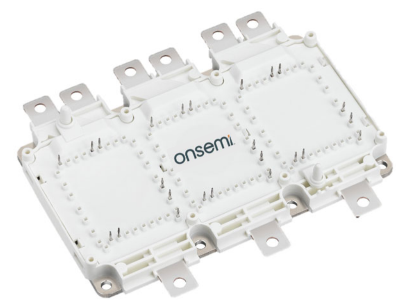
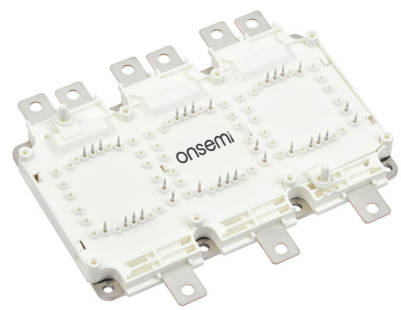


VE−Trac Direct Module − NVH950S75L4SPB



EliteSiC Power Module − NVXR17S90M2SPB

Introduction

The IGBT and SiC module's switching characteristics are affected by many external parameters such as voltage, current, temperature, gate configurations and stray elements. This document centers around the influence of the DC−link loop inductance and gate loop inductance on the switching characteristics for the VE−Trac IGBT and EliteSiC Power modules.

Test Setup

The Double Pulse Test (DPT) setup is used to extract the switching characteristics of the SiC and IGBT modules. For the DC−link loop inductance impact analysis, added the busbars between the DC−link capacitor and module, as shown in Table 1 And for the gate loop inductance impact analysis, the external sockets or wires were added between the gate driver board and module, as shown in Table 10. In order to investigate the module switching characteristics, the 900 V, 1.7 mΩ class EliteSiC Power Module (NVXR17S90M2SPC) and 750 V class Field Stop 4 VE−Trac Direct Module (NVH950S75L4SPB) are used as DUTs.

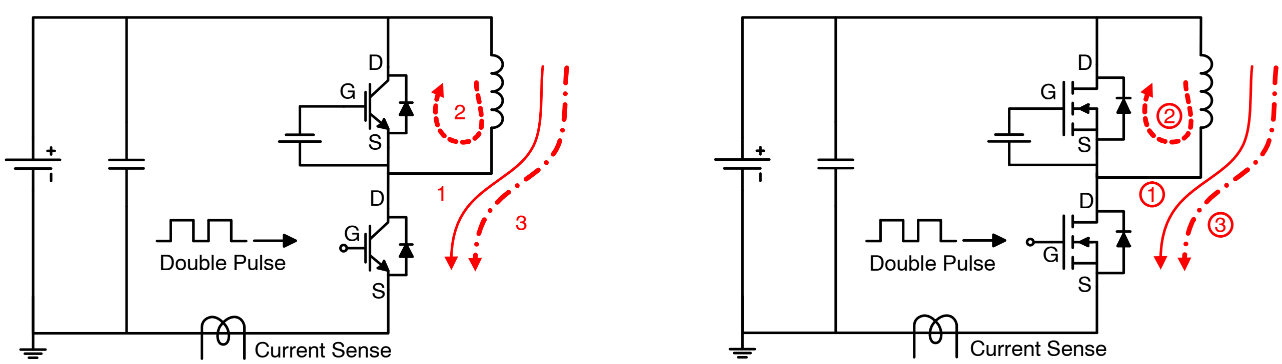
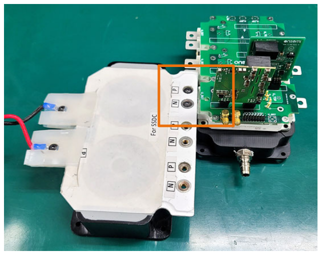
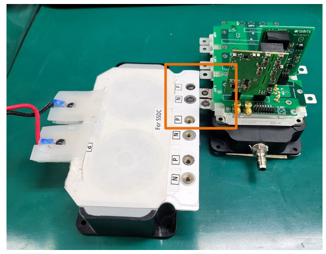
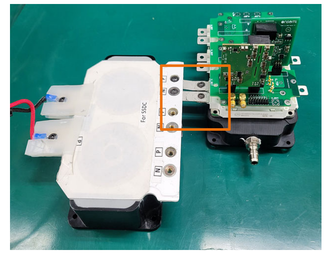


Figure 1. Double Pulse Test Setup

Table 1. DC−LINK LOOP INDUCTANCE TEST SETUP

Test Case (Loop Inductance)	23 nH	30 nH	37 nH
Test Configuration	 No additional bus bar	 + short bus bar (7 nH)	 + long bus bar (14 nH)

IGBT Switching Characteristics vs. DC−Link Loop Inductance (L_S)

This section analyzes the impact of different DC−link inductances on the IGBT switching characteristics. A double pulse test was performed on the NVH950S75L4SPB module with the following conditions.

- DUT: FS4 750V 950A IGBT Module (NVH950S75L4SPB) Low side
- VDC = 400 V
- I_C = 600 A
- V_{GE} = +15/−8 V
- $R_{G(on)}$ = 4.0 Ω
- $R_{G(off)}$ = 12.0 Ω
- T_{vj} = 25°C

Table 1 shows test setups for three different DC−link loop inductance configurations to analyze the impact of DC−link loop inductance.

Figure 2 illustrates waveform comparison by different DC−link loop inductance setups during the IGBT turn−on, and summarized characteristics are described in Table 1 below. A higher loop inductance setup shows a higher inductive V_{CE} voltage drop with a slower turn−on di/dt. As a result, a higher loop inductance leads to lower turn−on loss because the loss is an integral of V_{CE} and I_C with time.

In terms of the diode, after the reverse recovery peak current (I_{rrm}), higher loop inductance impacts the diode peak voltage overshoot. Therefore, a higher loop inductance configuration setup impacts higher reverse recovery loss from snappy recovery. Consequently, $R_{G(on)}$ increase is necessary for EMI compatibility.

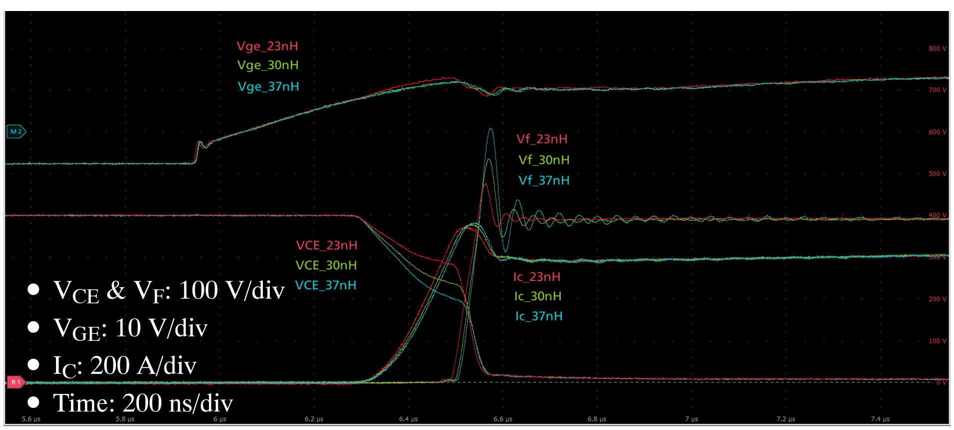


Figure 2. IGBT Turn−on Waveforms vs. DC−Link Loop Inductance (L_S)

Table 2. IGBT TURN−ON CHARACTERISTICS VS. DC−LINK LOOP INDUCTANCE

Test Case	23 nH	30 nH	37 nH
E_{on}	24.0 mJ	21.4 mJ	18.6 mJ
di/dt $_{(20–80\%)}$	4.5 A/ns	4.4 A/ns	4.3 A/ns
$V_{F.peak}$	475 V	535 V	609 V
E_{rr}	3.0 mJ	3.4 mJ	3.7 mJ

Figure 3 illustrates a waveform comparison between different DC−link loop inductance setups during the IGBT turn−off event. Summarized characteristics are described in Table 3 below. A higher loop inductance setup shows a slower di/dt during the turn−off but a higher V_{CE} peak voltage due to the stray inductance. As a result, higher loop inductance leads to higher turn−off loss because the losses are integral of V_{CE} and I_C with time. However, a higher V_{CE} peak voltage can exceed the V_{CE} voltage breakdown limit during high current driving. Hence increasing the $R_{G(off)}$ is highly recommended to suppress the peak voltage and oscillations. Additionally, the adherence to reverse bias safe operating area (RBSOA) is an essential system design factor that shall be considered according to the stray inductance and turn−off speed.

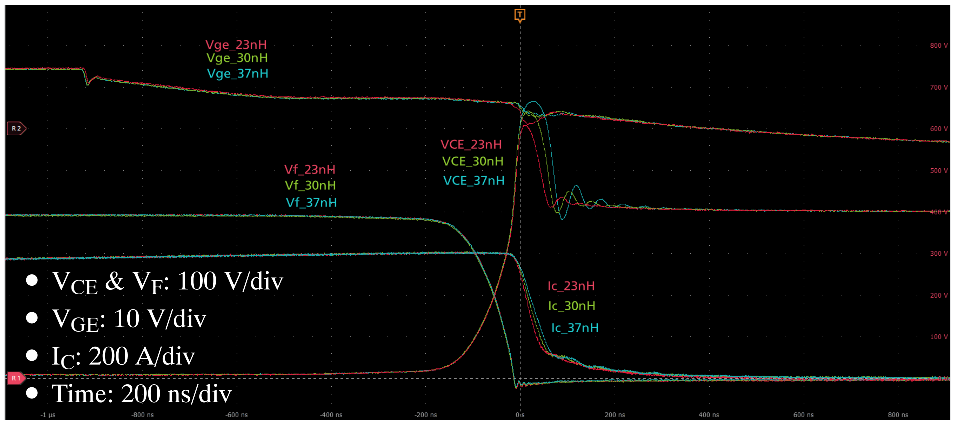


Figure 3. IGBT Turn−off Waveforms vs. DC−Link Loop Inductance (L_S)

Table 3. IGBT TURN−OFF CHARACTERISTICS VS. DC−LINK LOOP INDUCTANCE

Test Case	23 nH	30 nH	37 nH
E_{off}	33.8 mJ	37.6 mJ	40.0 mJ
dV/dt $_{(20–80\%)}$	5.0 V/ns	5.4 V/ns	5.7 V/ns
−di/dt $_{(85–55\%)}$	9.1 A/ns	8.1 A/ns	7.2 A/ns
$V_{CE.peak}$	608 V	643 V	666 V

IGBT Switching Characteristics vs. DC−Link Loop Inductance (L_G) with Optimized R_G

A higher DC−Link loop inductance setup has a lower Eon by higher V_{CE} voltage drop during the turn−on. By the way, from the system level consideration, it is mandatory to increase $R_{G(on)}$ to have a similar EMI level with the lower DC−Link inductance.

In the case of the IGBT, the DC−link inductance plays an important role in the level of the V_{CE} overshoot voltage during the turn−off because the turn−off di/dt is not that significantly affected by the external $R_{G(off)}$. A higher V_{CE} overvoltage causes a worse RBSOA performance, so adjusting the $R_{G(off)}$ is required based on the DC−link loop inductance. Figure 4 illustrates a waveform comparison between the DC−link loop inductance setups with optimized $R_{G(on)}$ during the IGBT turn−on. Tuned the $R_{G(on)}$ till it has a similar V_F level with the original 23 nH test setup because the V_F peak and oscillation is one of the significant EMI noise sources at the MHz range. As a result, a higher DC−link loop inductance setup with an optimized $R_{G(on)}$ shows a higher E_{on} with a slower di/dt.

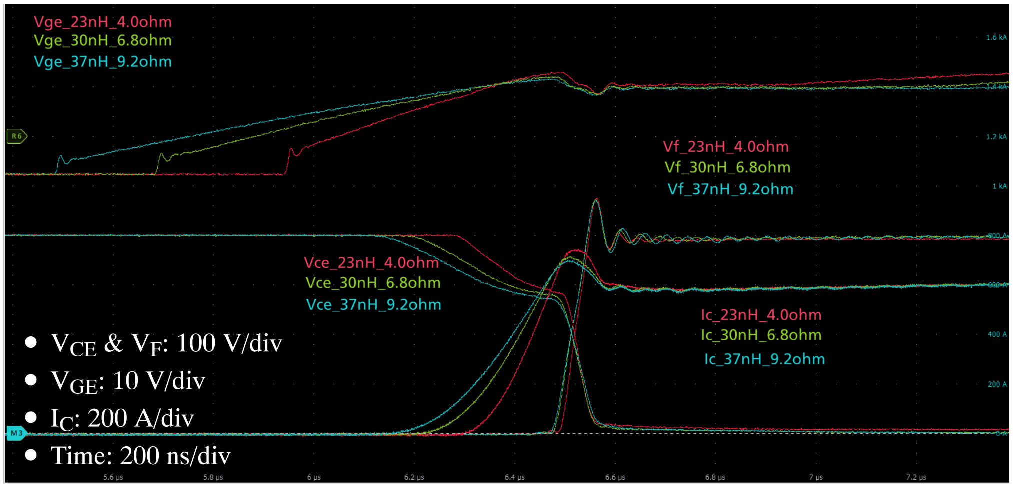


Figure 4. IGBT Turn−on Waveforms vs. DC−Link Loop Inductance with Optimized $R_{G(on)}$

Table 4. IGBT TURN−ON CHARACTERISTICS VS. DC−LINK LOOP INDUCTANCE WITH OPTIMIZED $R_{G(on)}$

Test Case	23 nH	30 nH	37 nH
$R_{G(on)}$	4.0 Ω	6.8 Ω	9.2 Ω
E_{on}	24.0 mJ	27.7 mJ	31.3 mJ
di/dt $_{(20–80\%)}$	4.5 A/ns	3.3 A/ns	2.7 A/ns
$V_{E.peak}$	475 V	472 V	470 V
E_{rr}	3.0 mJ	2.4 mJ	2.3 mJ

Figure 5 illustrates a waveform comparison between the DC−link loop inductance setups with optimized $R_{G(off)}$ during the IGBT Turn−off. To keep the V_{CE} overshoot level similar to the original 23 nH setup, a higher $R_{G(off)}$ was used for the higher loop inductance setups. As a result, a higher DC−link loop inductance setup shows a higher E_{off} with a slower dV/dt.

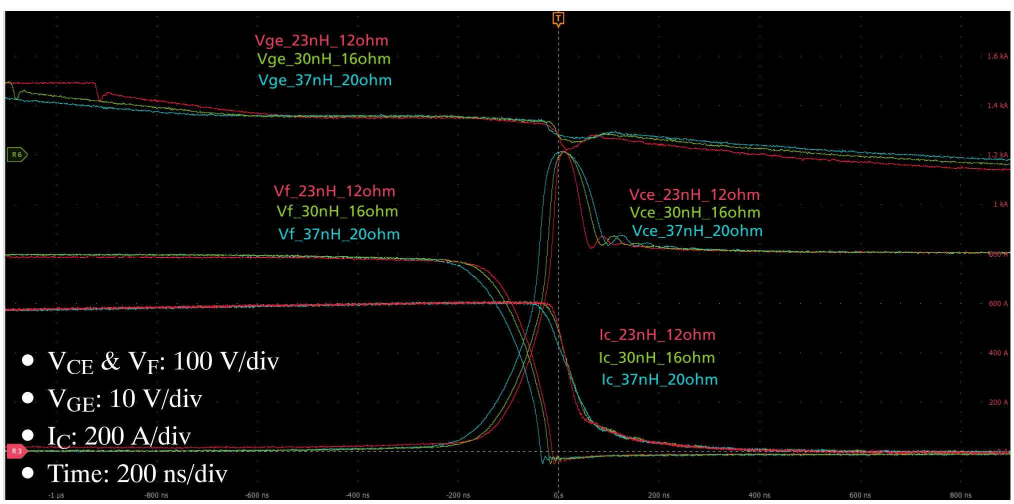


Figure 5. IGBT Turn−off Waveforms vs. DC−Link Loop Inductance with Optimized $R_{G(off)}$

Table 5. IGBT TURN–OFF CHARACTERISTICS VS. DC–LINK LOOP INDUCTANCE WITH OPTIMIZED $R_{G(off)}$

Test Case	23 nH	30 nH	37 nH
$R_{G(off)}$	12.0 Ω	16.0 Ω	20.0 Ω
E_{off}	33.8 mJ	35.0 mJ	39.4 mJ
dV/dt $_{(20–80\%)}$	5.0 V/ns	4.8 V/ns	4.6 V/ns
–di/dt $_{(85–55\%)}$	9.1 A/ns	7.1 A/ns	5.2 A/ns
$V_{CE.peak}$	608 V	606 V	607 V

SiC MOSFET Switching Characteristics vs. DC–Link Loop Inductance (L_S)

In this section, the impact of different DC–link inductances on the SiC MOSFET switching characteristics is analyzed. A double pulse test was performed on the NVXR17S90M2SPC module in the same test setup as Table 1 with the following conditions.

- DUT: NVXR17S90M2SPC Low side
- VDC = 400 V
- I_D = 600 A
- V_{GS} = +18/–5 V
- $R_{G(on)}$ = 3.9 Ω
- $R_{G(off)}$ = 1.8 Ω
- T_{vj} = 25°C

Figure 6 illustrates waveform comparison by different DC–link loop inductance setups during the SiC MOSFET turn–on and summarized characteristics are described in Table 6 below. The higher loop inductance setup shows a higher inductive V_{DS} voltage drop with a slower turn–on di/dt. As a result, this leads to lower turn–on loss because the loss is integral of V_{DS} and I_D with time.

In terms of the body diode, after the reverse recovery peak current, higher loop inductance impacts the diode peak voltage. Therefore, a higher loop inductance configuration setup impacts higher reverse recovery loss with snappy recovery. As a consequence of snappy recovery, increasing the $R_{G(on)}$ may require compatibility with the EMI. Additionally, in the SiC MOSFET case, the EMI compatibility is more critical than the IGBT because it has a larger oscillation amplitude and frequency that can work as a noise source.

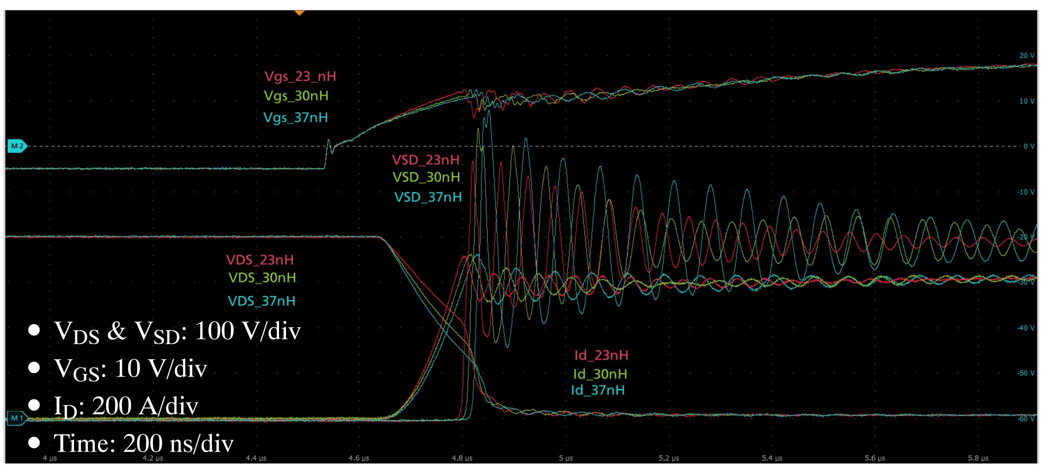


Figure 6. SiC MOSFET Turn–on Waveforms vs. DC–Link Loop Inductance

Table 6. SiC MOSFET TURN–ON CHARACTERISTICS VS. DC–LINK LOOP INDUCTANCE

Test Case	23 nH	30 nH	37 nH
E_{on}	14.3 mJ	12.7 mJ	10.4 mJ
di/dt $_{(20–80\%)}$	6.0 A/ns	5.7 A/ns	5.4 A/ns
$V_{SD.peak}$	567 V	639 V	679 V
E_{rr}	0.7 mJ	1.0 mJ	1.6 mJ

Figure 7 illustrates waveform comparison by different DC−link loop inductance setups during the SiC MOSFET turn−off and summarized characteristics are described in Table 9 below. A higher loop inductance setup shows a slower di/dt during the turn−off but a higher V_{DS} peak voltage due to the inductance. As a result, a higher loop inductance leads to higher turn−off loss because the loss is an integral of V_{DS} and I_D with time. However, a higher V_{DS} peak voltage can exceed the V_{DS} voltage limit during high current driving. Hence increasing the $R_{G(off)}$ is highly recommended to suppress the peak voltage and oscillations. Additionally, the adherence to reverse bias safe operating area (RBSOA) and compatibility with the EMI regulation is an essential system design factor that shall be considered according to the stray inductance and turn−off speed.

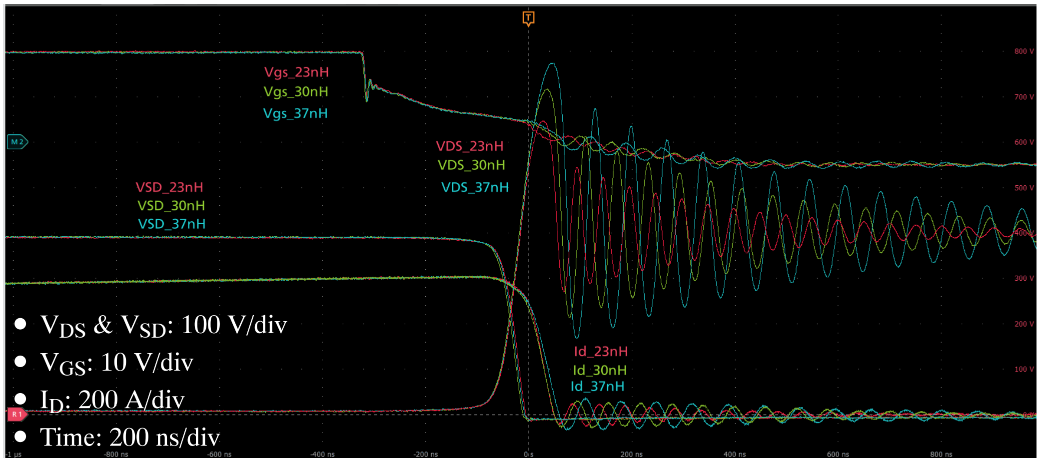


Figure 7. SiC MOSFET Turn−off Waveforms vs. DC−Link Loop Inductance

Table 7. SiC MOSFET TURN−OFF CHARACTERISTICS VS. DC−LINK LOOP INDUCTANCE

Test Case	23 nH	30 nH	37 nH
E_{off}	17.0 mJ	19.4 mJ	21.8 mJ
dV/dt $_{(20−80\%)}$	8.9 V/ns	9.0 V/ns	9.1 V/ns
−di/dt $_{(80−20\%)}$	10.4 A/ns	8.9 A/ns	8.5 A/ns
$V_{DS.peak}$	647 V	717 V	774 V

SiC MOSFET Switching Characteristics vs. DC−Link Loop Inductance (L_G) – Optimized R_G

A higher DC−Link loop inductance setup has a lower Eon by higher V_{DS} voltage drop during the turn−on. By the way, from the system level consideration, it is mandatory to increase $R_{G(on)}$ to compensate for the V_{SD} voltage peak/amplitude and EMI level. Furthermore, higher V_{DS} overvoltage causes a worse RBSOA performance, so adjusting the $R_{G(off)}$ is required based on the DC−link loop inductance setup. Figure 8 illustrates a waveform comparison between the DC−link loop inductance setups with optimized $R_{G(on)}$ during the SiC MOSFET Turn−on. Tuned the $R_{G(on)}$ till it has a similar V_{SD} level with the original 23 nH test setup because the V_{SD} peak and oscillation is one of the significant EMI noise sources at the MHz range. As a result, a higher DC−link loop inductance setup shows a higher Eon with a slower di/dt.

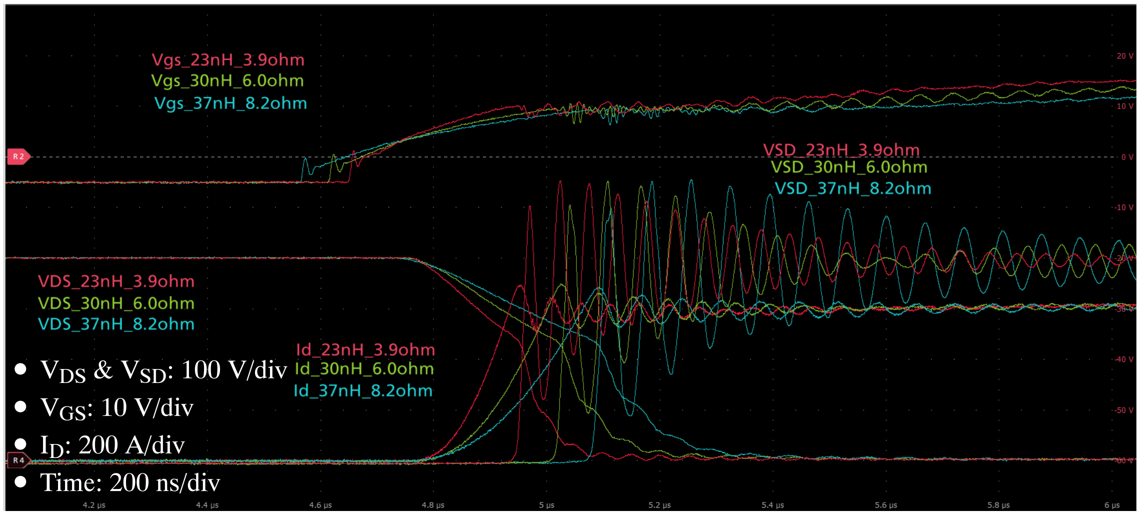


Figure 8. SiC MOSFET Turn−on Waveforms vs. DC−Link Loop Inductance with Optimized $R_{G(on)}$

Table 8. SiC MOSFET TURN−ON CHARACTERISTICS VS. DC−LINK LOOP INDUCTANCE WITH OPTIMIZED $R_{G(on)}$

Test Case	23 nH	30 nH	37 nH
$R_{G(on)}$	4.0 Ω	6.0 Ω	8.2 Ω
E_{on}	18.2 mJ	24.5 mJ	31.4 mJ
di/dt $_{(20–80\%)}$	5.3 A/ns	3.8 A/ns	2.9 A/ns
$V_{SD.peak}$	552 V	552 V	555 V
E_{rr}	0.4 mJ	0.7 mJ	0.7 mJ

Figure 9 illustrates a waveform comparison between the DC−link loop inductance setups with optimized $R_{G(off)}$ during the SiC MOSFET Turn−off. To keep the V_{DS} overshoot level similar to the original 23 nH setup, a higher $R_{G(off)}$ was used for the higher loop inductance setups. As a result, a higher DC−link loop inductance setup shows a higher E_{off} with a slower dV/dt.

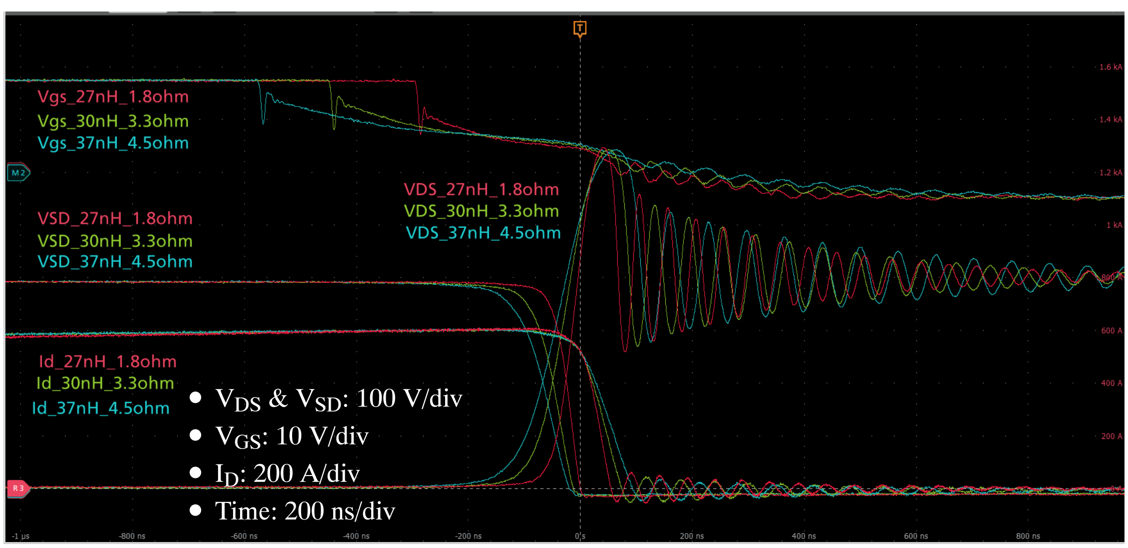
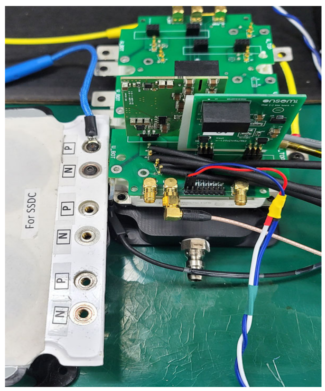
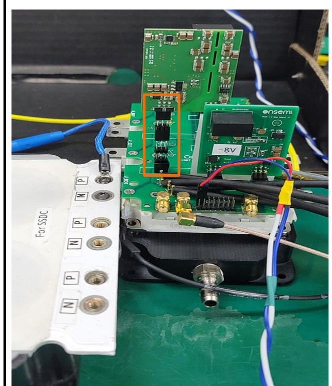
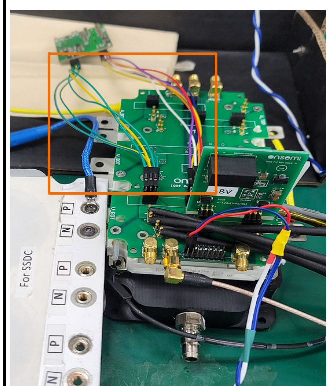


Figure 9. SiC MOSFET Turn−off Waveforms vs. DC−Link Loop Inductance with Optimized $R_{G(off)}$

Table 9. SiC MOSFET TURN−OFF CHARACTERISTICS VS. DC−LINK LOOP INDUCTANCE WITH OPTIMIZED $R_{G(OFF)}$

Test Case	23 nH	30 nH	37 nH
$R_{G(off)}$	1.8 Ω	3.3 Ω	4.5 Ω
E_{off}	15.3 mJ	24.8 mJ	32.9 mJ
dV/dt $_{(20–80\%)}$	8.5 V/ns	5.8 V/ns	4.4 V/ns
−di/dt $_{(80–20\%)}$	10.4 A/ns	7.3 A/ns	5.9 A/ns
$V_{DS.peak}$	647 V	645 V	645 V

Table 10. GATE LOOP INDUCTANCE TEST SETUP

Test Case (Loop Inductance)	Case 1	Case 2	Case 3
Test Configuration	 No additional element	 + additional socket (5 cm)	 + external wire (20 cm)

IGBT Switching Characteristics vs. Gate Loop Inductance (L_G)

Furthermore, the gate loop inductance influences the switching characteristics. A double pulse test was performed on the NVH950S75L4SPB module with the following conditions.

- DUT: FS4 750V 950A IGBT Module (NVH950S75L4SPB) Low side
- VDC = 400 V
- I_C = 600 A
- V_{GE} = +15/−8 V
- $R_{G(on)}$ = 4.0 Ω
- $R_{G(off)}$ = 12.0 Ω
- T_{vj} = 25°C

Table 10 shows three different test setups for the gate loop inductance vs. switching characteristics. The external socket or extended wires are added between the gate driver and module to simulate a higher loop inductance on the gate loop.

Figure 10 illustrates waveform comparison by different gate loop test setups during the IGBT turn−on, and summarized characteristics are described in Table 11 below. A longer gate loop test setup shows a lower E_{on} with faster di/dt. A gate loop inductance is mainly caused by gate loop length. The gate loop inductance can slow down the rising current at the beginning of the turn−on. When the gate voltage reaches the miller plateau, the loop inductance works as a current source. This current source can speed up the di/dt by sourcing more current to the gate. The impact on the turn−on characteristics by gate loop length is less significant than the DC−link loop. Meanwhile, a higher gate loop inductance can increase the overshoot of the gate voltage, which can lose controllability by R_G.

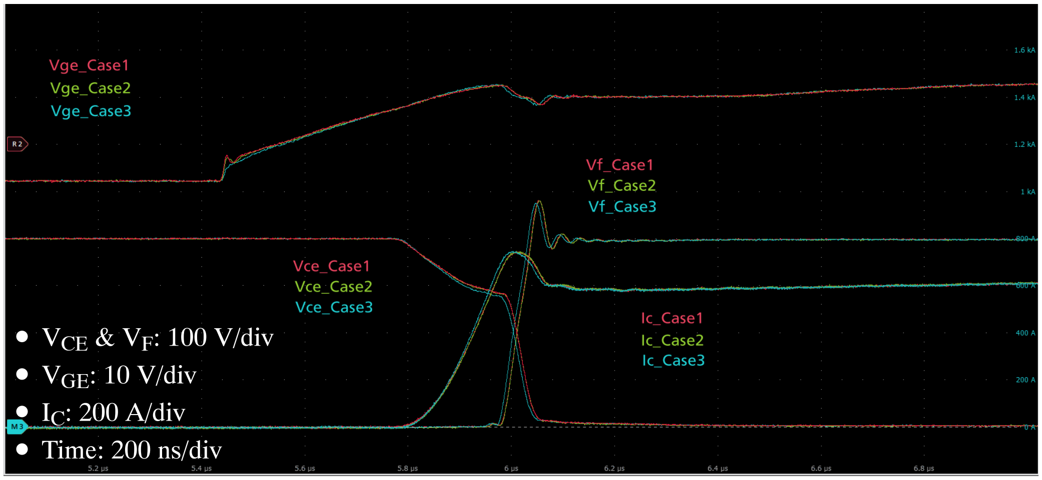


Figure 10. IGBT Turn−on Waveforms vs. Gate Loop Inductance (L_G)

Table 11. IGBT TURN−ON CHARACTERISTICS VS. GATE LOOP INDUCTANCE

Test Case	Case 1	Case 2	Case 3
E_{on}	22.6 mJ	22.2 mJ	21.6 mJ
di/dt $_{(20–80\%)}$	4.5 A/ns	4.6 A/ns	4.8 A/ns
$V_{F.peak}$	475 V	475 V	474 V
E_{rr}	3.0 mJ	3.4 mJ	3.7 mJ

Figure 11 illustrates a waveform comparison between different gate loop inductance setups during the IGBT turn−off event. Summarized characteristics are described in Table 12 below. The turn−off characteristics are less impact than the turn−on characteristics. At the beginning of the turn−off, the undershoot voltage is slightly different by gate loop inductance, but it cannot impact the turn−off characteristics. When gate voltage reaches the miller plateau, dV/dt and di/dt are slightly changed by undershoot but are quickly covered by gate sink current within a short transient.

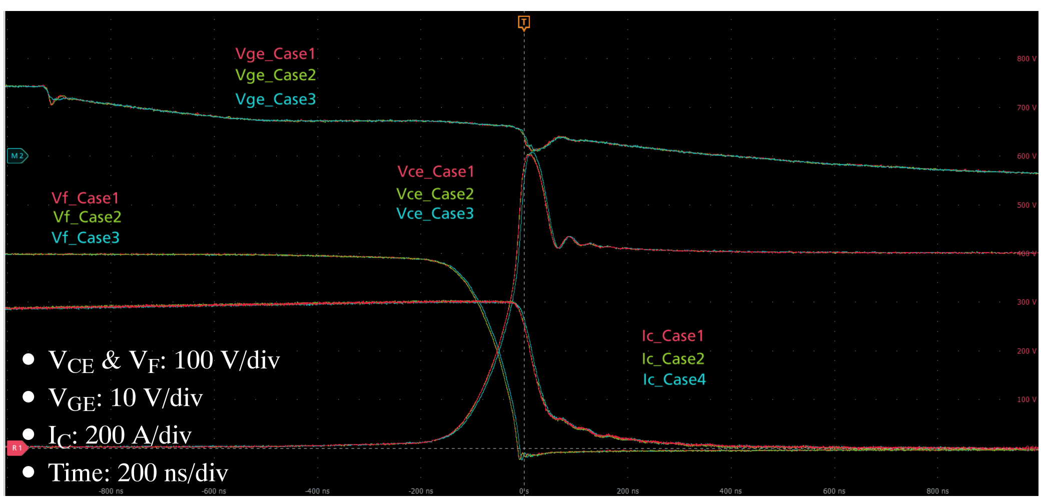


Figure 11. IGBT Turn−off Waveforms vs. Gate Loop Inductance (L_G)

Table 12. IGBT TURN−OFF CHARACTERISTICS VS. GATE LOOP INDUCTANCE (L_G)

Test Case	Case 1	Case 2	Case 3
E_{off}	31.5 mJ	31.2 mJ	31.2 mJ
dV/dt $_{(20−80\%)}$	5.0 V/ns	5.0 V/ns	5.1 V/ns
−di/dt $_{(85−55\%)}$	9.1 A/ns	9.1 A/ns	9.3 A/ns
$V_{CE.peak}$	602 V	604 V	608 V

SiC MOSFET Switching Characteristics vs. Gate Loop Inductance (L_G)

In this section, the impact of different gate loon inductances on the SiC MOSFET switching characteristics is analyzed. A double pulse test was performed on the NVXR17S90M2SPC module in the same test setup as Table 10 with the following conditions.

- DUT: NVXR17S90M2SPC Low side
- VDC = 400 V
- I_D = 600 A
- V_{GS} = +18/−5 V
- $R_{G(on)}$ = 3.9 Ω
- $R_{G(off)}$ = 1.8 Ω
- T_{vj} = 25°C

Figure 12 shows waveform comparison by different gate loop test setups during the SiC MOSFET turn−on, and summarized characteristics are described in Table 13 below. As in the IGBT case, a longer gate loop test setup shows a lower E_{on} and higher $V_{SD.peak}$ voltage by faster di/dt.

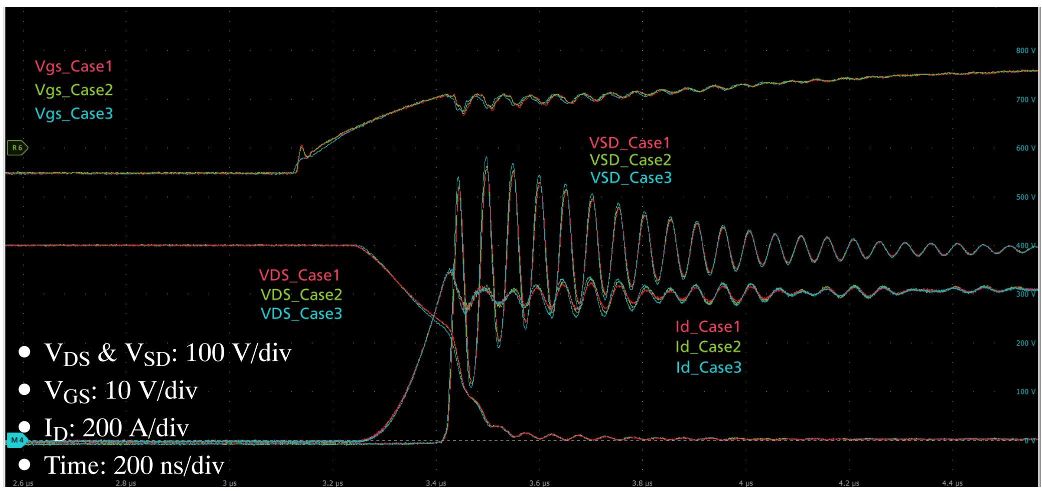


Figure 12. SiC MOSFET Turn−on Waveforms vs. Gate Loop Inductance (L_G)

Table 13. SiC MOSFET TURN−ON CHARACTERISTICS VS. GATE LOOP INDUCTANCE

Test Case	Case 1	Case 2	Case 3
E_{on}	16.3 mJ	16.2 mJ	15.3 mJ
di/dt $_{(20−80\%)}$	5.1 A/ns	5.1 A/ns	5.4 A/ns
$V_{SD.peak}$	558 V	563 V	581 V
E_{rr}	0.5 mJ	0.6 mJ	0.7 mJ

Figure 13. illustrates a waveform comparison between different gate loop inductance setups during the SiC MOSFET turn−off event. Summarized characteristics are described in Table 14 below. A higher gate loop inductance test setup shows a lower E_{off} with a faster di/dt even though a higher V_{DS} overshoot voltage. After tun−off, the I_D oscillation amplitude that could be an EMI noise source depends on the length of the gate loop.

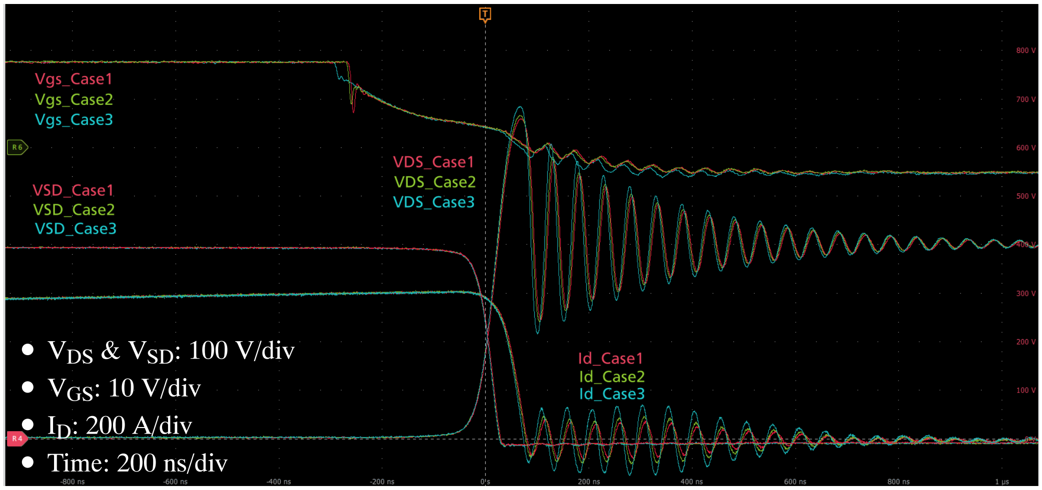


Figure 13. SiC MOSFET Turn−off Waveforms vs. Gate Loop Inductance (L_G)

Table 14. SiC MOSFET TURN−OFF CHARACTERISTICS VS. GATE LOOP INDUCTANCE

Test Case	Case 1	Case 2	Case 3
E_{off}	14.8 mJ	14.8 mJ	14.2 mJ
dV/dt $_{(20–80\%)}$	9.1 V/ns	9.2 V/ns	9.5 V/ns
−di/dt $_{(80–20\%)}$	10.3 A/ns	10.5 A/ns	11.8 A/ns
$V_{DS.peak}$	672 V	679 V	702 V

Summary

In this application note analyzes the impact of the inductance on the IGBT and SiC MOSFET module's switching characteristics.

A higher DC−link loop inductance setup brings lower E_{on} while higher E_{off} and E_{rr}. Furthermore, the overall result seems to be that a total switching loss gap between the 23 nH and 37 nH test setup is less than 2 mJ. Thus, it can easily misunderstand that the stray inductance does not have a big impact on the switching losses. However, to adhere to the RBSOA and EMC, adjusting the external gate resistance or the other parameters for the system performance is mandatory, although it loses di/dt controllability and switching losses. Figure 14 and Figure 15 illustrate an IGBT and SiC switching loss comparison result by DC−link loop inductance with/without the external R_G optimization. Before optimizing the external R_G, a higher DC−link loop inductance setup shows similar total switching losses, but after external R_G optimization for the system performance, the total loss is a 20% and 92% increase in each IGBT and SiC case when DC−link loop inductance changes from 23 nH to 37 nH.

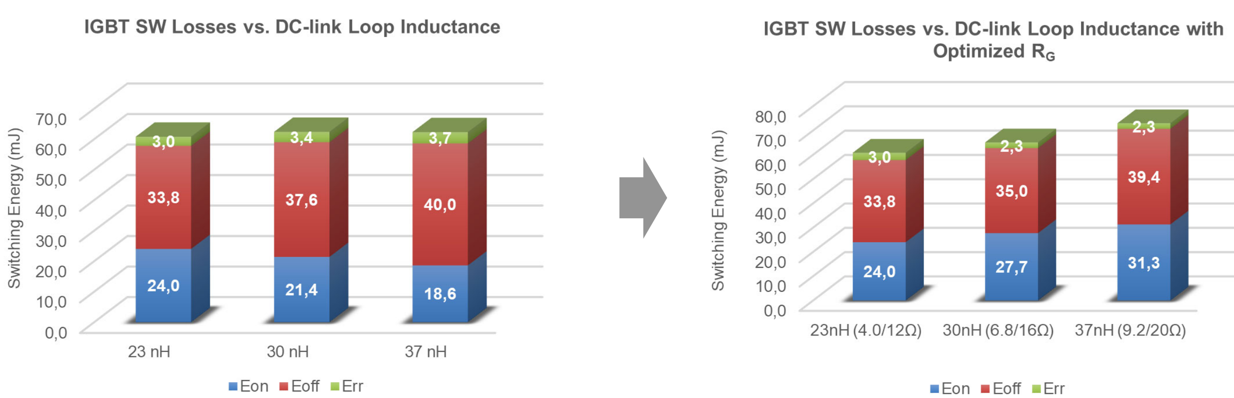


Figure 14. IGBT Total Losses Comparison

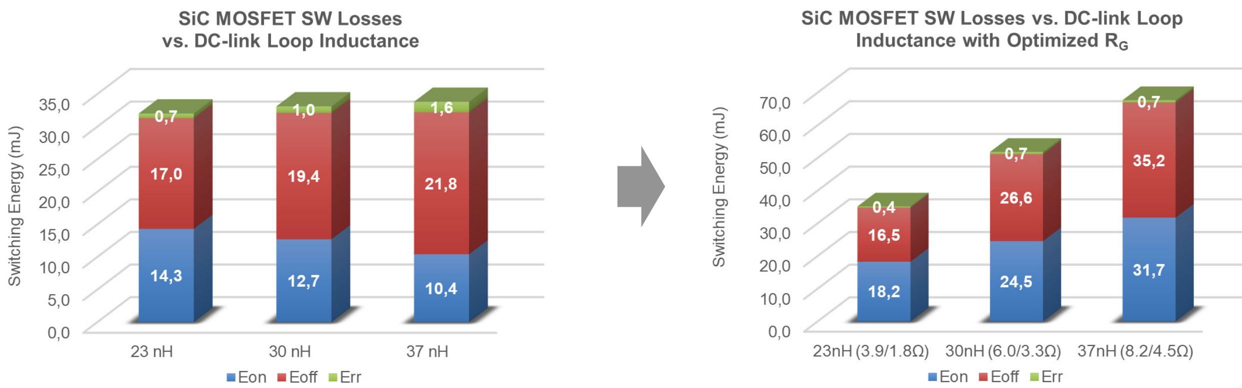


Figure 15. SiC MOSFET Total Switching Losses Comparison

A higher gate loop inductance setup brings a slightly faster turn−on transient by inductive effect after the miller plateau. And it is a less significant impact than the DC−link loop inductance from the switching loss point of view. However, because of the unwanted gate overshoot, a higher gate loop inductance setup will bring lower controllability to the gate. In terms of the short circuit event, this inductance can pull up the gate voltage, thus, it will have a shortened short circuit withstand time by the increased gate voltage. In addition, a longer gate loop has less electromagnetic noise immunity or interferes with the other circuitry because it can work as an antenna.

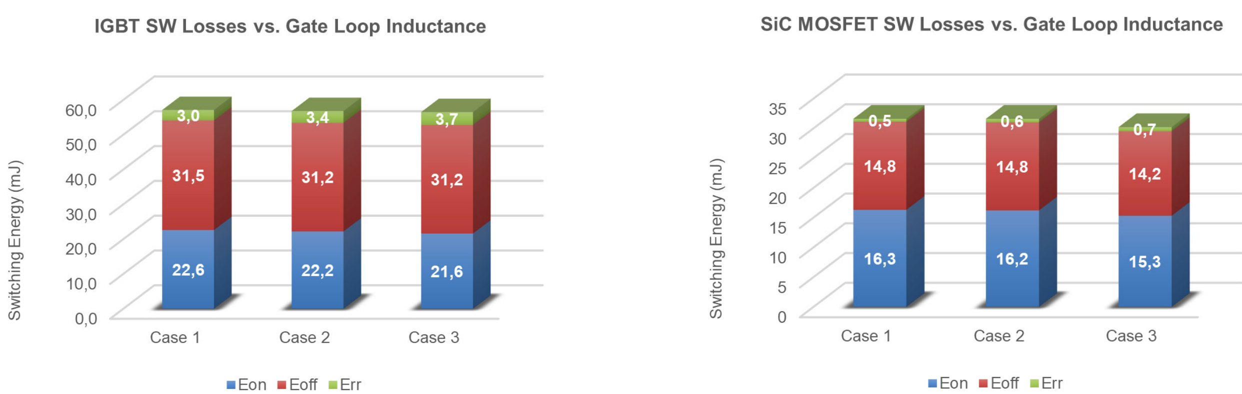


Figure 16. IGBT/SiC MOSFET Switching Losses vs. Gate Loop Inductance

In conclusion, minimizing DC−link and gate loop inductance is essential for the IGBT/SiC switching application to get lower switching losses with controllability and EMC.

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