Preferred Device

Darlington Complementary Silicon Power Transistors

This package is designed for general-purpose amplifier and low frequency switching applications.

Features

- High DC Current Gain $h_{FE} = 3500 \text{ (Typ)} @ I_C = 5.0 \text{ Adc}$
- Collector-Emitter Sustaining Voltage @ 100 mA V_{CEO(sus)} = 100 Vdc (Min)
- Monolithic Construction with Built-In Base-Emitter Shunt Resistors
- This is a Pb-Free Device*

MAXIMUM RATINGS (Note 1)

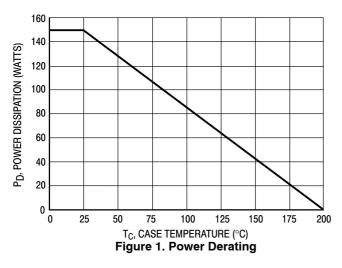
Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V _{CEO}	100	Vdc
Collector-Base Voltage	V _{CB}	100	Vdc
Emitter-Base Voltage	V_{EB}	5.0	Vdc
Collector Current – Continuous Peak	Ι _C	12 20	Adc
Base Current	Ι _Β	0.2	Adc
Total Power Dissipation @ $T_C = 25^{\circ}C$ Derate above $25^{\circ}C$	PD	150 0.857	W W/°C
Operating and Storage Temperature Range	T _J , T _{stg}	–65 to +200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	1.17	°C/W

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Indicates JEDEC Registered Data.

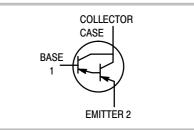


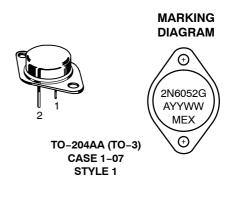


ON Semiconductor®

http://onsemi.com

12 AMPERE COMPLEMENTARY SILICON POWER TRANSISTOR 100 VOLTS, 150 WATTS





2N6052	=	Device Code
G	=	Pb-Free Package
Α	=	Location Code
YY	=	Year
WW	=	Work Week
MEX	=	Country of Orgin

ORDERING INFORMATION

Device	Package	Shipping
2N6052G	TO-3 (Pb-Free)	100 Units/Tray

Preferred devices are recommended choices for future use and best overall value.

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted) (Note 2)

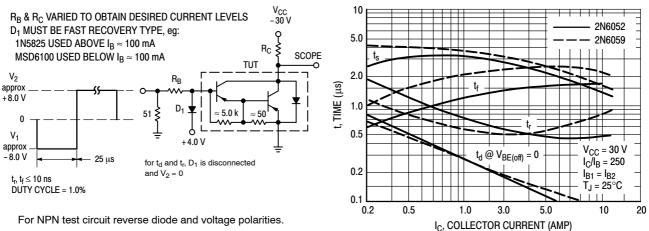
Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (Note 3)	$(I_{C} = 100 \text{ mAdc}, I_{B} = 0)$	V _{CEO(sus)}	100	-	Vdc
Collector Cutoff Current	$(V_{CE} = 50 \text{ Vdc}, I_B = 0)$	I _{CEO}	-	1.0	mAdc
$ Collector Cutoff Current \\ (V_{CE} = Rated V_{CEO}, V_{BE(off)} = 1.5 Vdc) \\ (V_{CE} = Rated V_{CEO}, V_{BE(off)} = 1.5 Vdc, T_C = 150^{\circ}C) $		I _{CEX}		0.5 5.0	mAdc
Emitter Cutoff Current	$(V_{BE} = 5.0 \text{ Vdc}, I_{C} = 0)$	I _{EBO}	-	2.0	mAdc

ON CHARACTERISTICS (Note 3)

DC Current Gain		h _{FE}			_
	$(I_{C} = 6.0 \text{ Adc}, V_{CE} = 3.0 \text{ Vdc})$ $(I_{C} = 12 \text{ Adc}, V_{CE} = 3.0 \text{ Vdc})$		750 100	18,000 -	
Collector-Emitter Saturation Voltage		V _{CE(sat)}			Vdc
	$(I_{C} = 6.0 \text{ Adc}, I_{B} = 24 \text{ mAdc})$ $(I_{C} = 12 \text{ Adc}, I_{B} = 120 \text{ mAdc})$	()	-	2.0 3.0	
Base-Emitter Saturation Voltage	$(I_C = 12 \text{ Adc}, I_B = 120 \text{ mAdc})$	V _{BE(sat)}	-	4.0	Vdc
Base-Emitter On Voltage	$(I_{C} = 6.0 \text{ Adc}, V_{CE} = 3.0 \text{ Vdc})$	V _{BE(on)}	-	2.8	Vdc
DYNAMIC CHARACTERISTICS		1	1	1	

$ \begin{array}{l} \mbox{Magnitude of Common Emitter Small-Signal Short Circuit Forward} \\ \mbox{Current Transfer Ratio} & (I_C = 5.0 \mbox{ Adc}, \mbox{ V}_{CE} = 3.0 \mbox{ Vdc}, \mbox{ f} = 1.0 \mbox{ MHz}) \end{array} $		h _{fe}	4.0	-	MHz
Output Capacitance	$(V_{CB} = 10 \text{ Vdc}, I_E = 0, f = 0.1 \text{ MHz})$	C _{ob}	-	500	pF
Small-Signal Current Gain	$(I_{C} = 5.0 \text{ Adc}, V_{CE} = 3.0 \text{ Vdc}, f = 1.0 \text{ kHz})$	h _{fe}	300	_	-

Indicates JEDEC Registered Data.
Pulse test: Pulse Width = 300 μs, Duty Cycle = 2.0%.



For NPN test circuit reverse diode and voltage polarities.



Figure 3. Switching Times

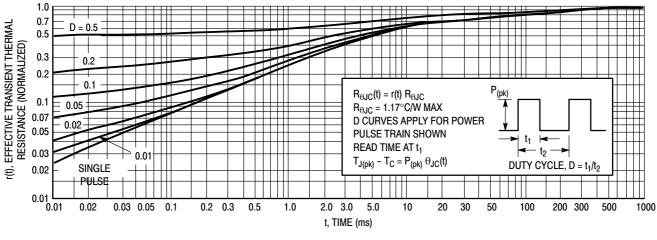


Figure 4. Thermal Response

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figures 5, and 6 is based on $T_{J(pk)} = 200^{\circ}C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 200^{\circ}C$; $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

T_C = 25°C

V_{CE} = 3.0 V

I_C = 5.0 A

200

500

1000

3000

2000

1000

500

200

100

50 30

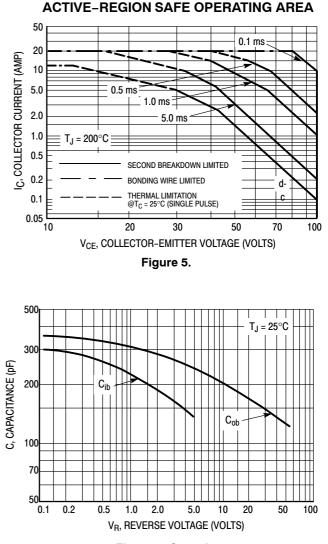
1.0

2.0

5.0

10 20

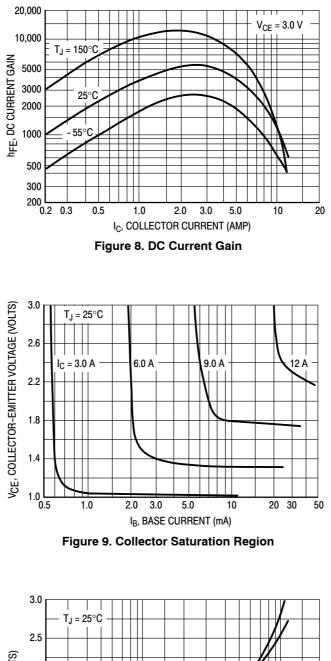
hfe, SMALL-SIGNAL CURRENT GAIN





50 100

Figure 7. Capacitance



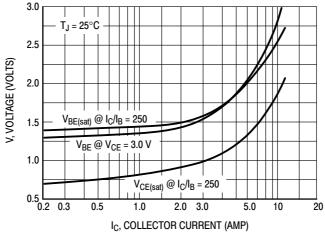


Figure 10. "On" Voltages

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TO-204 (TO-3) CASE 1-07 ISSUE Z DATE 10 MAR 2000 SCALE 1:1 NOTES: Δ 1. DIMENSIONING AND TOLERANCING PER ANSI ٠N Y14.5M. 1982. ¥ 2. CONTROLLING DIMENSION: INCH. 3. ALL RULES AND NOTES ASSOCIATED WITH REFERENCED TO-204AA OUTLINE SHALL APPLY. С E -T- SEATING PLANE MILLIMETERS Łκ INCHES → 🖛 D 2 PL MIN MAX MIN MAX DIM Α 1.550 REF 39.37 REF $| \oplus | \oslash 0.13 (0.005)$ \square T Q \square Y \square B
 -- 1.050
 -- 26.67

 0.250
 0.335
 6.35
 8.51

 D
 0.038
 0.043
 0.97

 E
 0.055
 0.070
 1.40
 1.09 1.40 1.77 -Y-1-> v G 0.430 BSC 10.92 BSC
 H
 0.215 BSC
 5.46 BSC

 K
 0.440
 0.480
 11.18
 12.19
 2**⊕** G ന് в 0.665 BSC 16.89 BSC L Ĥ
 N
 -- 0.830
 -- 21.08

 Q
 0.151
 0.165
 3.84
 4.19
 \oplus Å
 U
 1.187 BSC
 30.15 BSC

 V
 0.131
 0.188
 3.33
 4.77
 -Q-⊕ Ø 0.13 (0.005) M T Y M STYLE 3: PIN 1. GATE 2. SOURCE STYLE 5: PIN 1. CATHODE 2. EXTERNAL TRIP/DELAY STYLE 1: PIN 1. BASE STYLE 4: PIN 1. GROUND STYLE 2: PIN 1. BASE 2. COLLECTOR 2 FMITTER 2 INPUT CASE: COLLECTOR CASE: EMITTER CASE: DRAIN CASE: OUTPUT CASE: ANODE STYLE 6: STYLE 7: STYLE 8: STYLE 9: PIN 1. GATE 2. EMITTER PIN 1. ANODE 2. OPEN PIN 1. CATHODE #1 2. CATHODE #2 PIN 1. ANODE #1 2. ANODE #2

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CASE: ANODE

CASE: CATHODE

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CASE: COLLECTOR

CASE: CATHODE

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