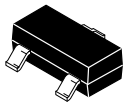
Field Effect Transistor - N-Channel, Enhancement Mode

2N7002K

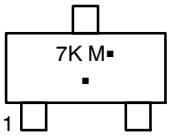


SOT−23 (TO−236)
CASE 318−08

Features

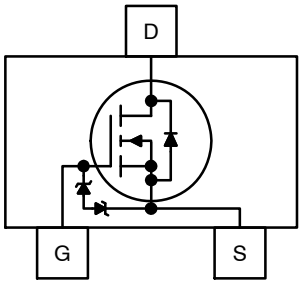
- Low On−Resistance
- Low Gate Threshold Voltage
- Low Input Capacitance
- Fast Switching Speed
- Low Input / Output Leakage
- Ultra−Small Surface Mount Package
- ESD HBM = 2000 V (Typical: 3000 V) as per JESD22 A114 and ESD CDM = 2000 V as per JESD22 C101
- This Device is Pb−Free, Halogen Free/BFR Free and is RoHS Compliant

MARKING DIAGRAM



7K = Specific Device Code
M = Date Code
▪ = Pb−Free Package
(Note: Microdot may be in either location)
*Date Code orientation may vary depending upon manufacturing location.

FUNCTIONAL SCHEMATIC



ORDERING INFORMATION

See detailed ordering and shipping information on page 4 of this data sheet.

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise specified)

Symbol	Parameter		Value	Unit
V_{DSS}	Drain−Source Voltage		60	V
V_{DGR}	Drain−Gate Voltage (R_{GS} ≤ 1.0 MΩ)		60	V
V_{GSS}	Gate−Source Voltage		±20	V
I_D	Drain Current	Continuous	300	mA
		Pulsed	800	
T_J	Operating Junction Temperature Range		−55 to +150	°C
T_{STG}	Storage Temperature Range		−55 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS (T_A = 25°C unless otherwise specified)

Symbol	Parameter	Value	Unit
P_D	Total Device Dissipation	350	mW
	Derate Above T_A = 25°C	2.8	mW/°C
$R_{\theta JA}$	Thermal Resistance, Junction−to−Ambient (Note 1)	350	°C/W

1. Device mounted on FR−4 PCB, 1 inch x 0.85 inch x 0.062 inch;Minimum land pad size.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Max	Unit
OFF CHARACTERISTICS (Note 2)					
BV_{DSS}	Drain−Source Breakdown Voltage	V_{GS} = 0 V, I_D = 10 μA	60	–	V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 60 V, V_{GS} = 0 V	–	1.0	μA
		V_{DS} = 60 V, V_{GS} = 0 V, T_J = 125°C	–	500	
I_{GSS}	Gate−Body Leakage	V_{GS} = ±20 V, V_{DS} = 0 V	–	±10	μA
ON CHARACTERISTICS (Note 2)					
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 μA	1.0	2.5	V
$R_{DS(ON)}$	Static Drain−Source On−Resistance	V_{GS} = 10 V, I_D = 0.5 A	–	2	Ω
		V_{GS} = 4.5 V, I_D = 200 mA	–	4	
$I_{D(ON)}$	On−State Drain Current	V_{GS} = 10 V, V_{DS} = 7.5 V	1.5	–	A
g_{FS}	Forward Transconductance	V_{DS} = 10 V, I_D = 0.2 A	200	–	mS
DYNAMIC CHARACTERISTICS					
C_{iss}	Input Capacitance	V_{DS} = 25 V, V_{GS}= 0 V, f = 1.0 MHz	–	50	pF
C_{oss}	Output Capacitance		–	15	pF
C_{rss}	Reverse Transfer Capacitance		–	6	pF
SWITCHING CHARACTERISTICS					
$t_{D(ON)}$	Turn−On Delay Time	V_{DD} = 30 V, I_{DSS} = 200 mA, R_G = 10 Ω, V_{GS} = 10 V	–	5	ns
$t_{D(OFF)}$	Turn−Off Delay Time		–	30	ns

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Short duration test pulse used to minimize self−heating effect.

TYPICAL PERFORMANCE CHARACTERISTICS

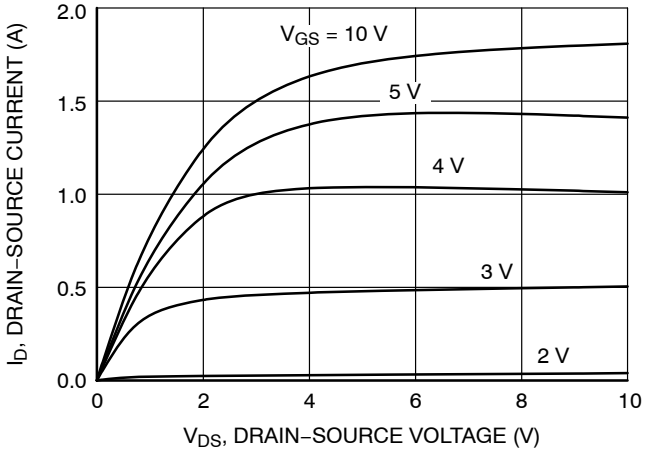


Figure 1. On−Region Characteristics

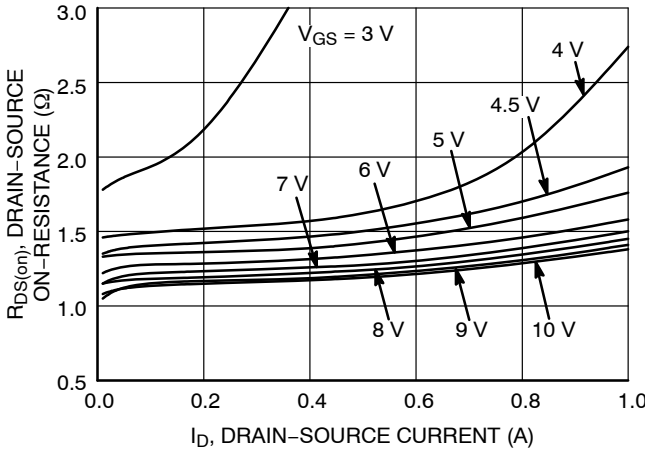


Figure 2. On−Resistance Variation with Gate Voltage and Drain Current

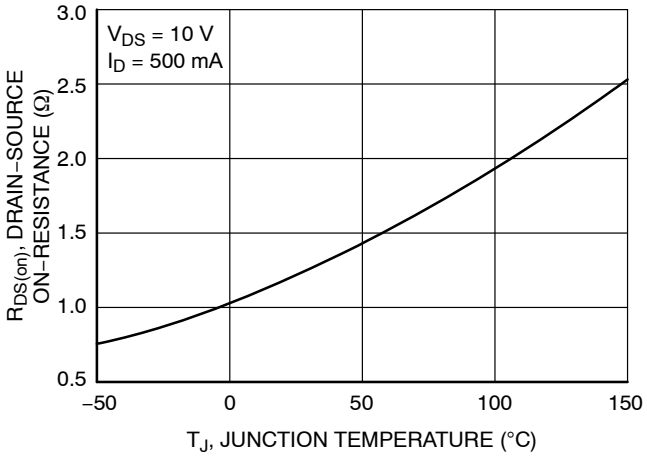


Figure 3. On−Resistance Variation with Temperature

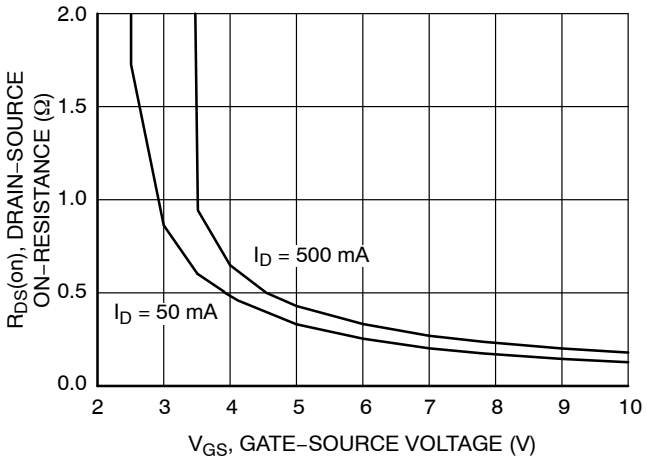


Figure 4. On−Resistance Variation with Gate−Source Voltage

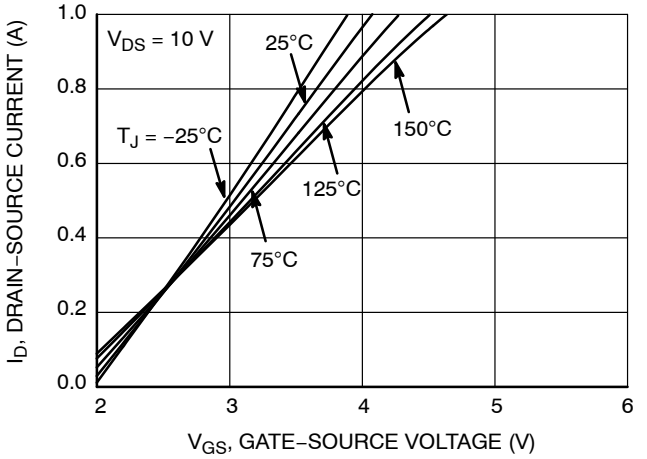


Figure 5. Transfer Characteristics

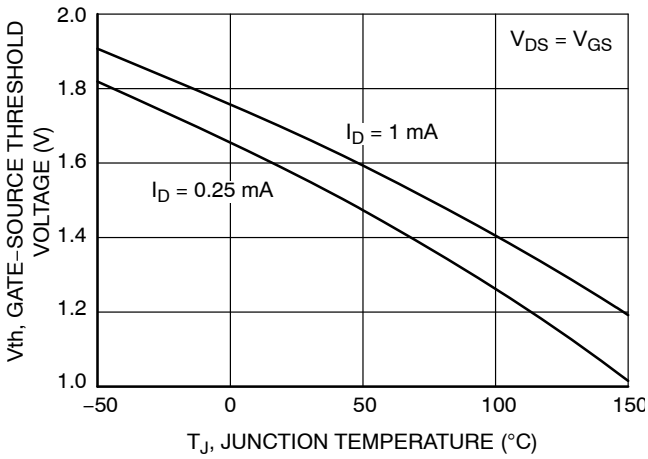


Figure 6. Gate Threshold Variation with Temperature

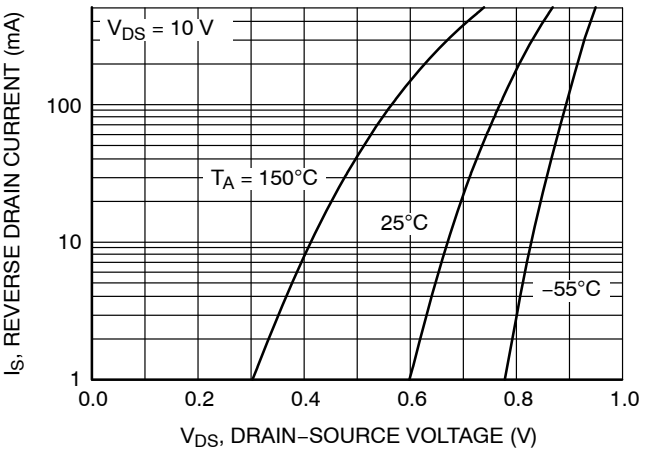


Figure 7. Reverse Drain Current Variation with Diode Forward Voltage and Temperature

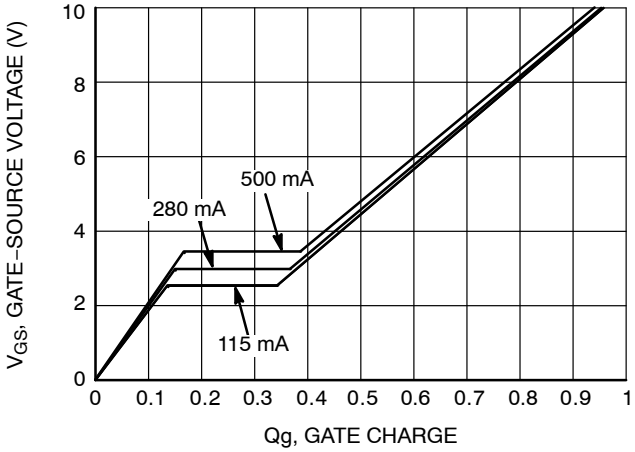


Figure 8. Gate Charge Characteristics

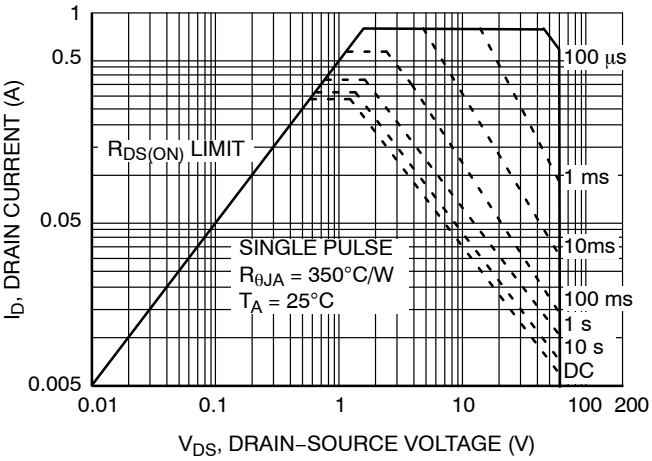


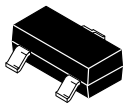
Figure 9. Maximum Safe Operating Area

ORDERING INFORMATION

Part Number	Top Mark	Package	Shipping†
2N7002K	7K	SOT−23 3L (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

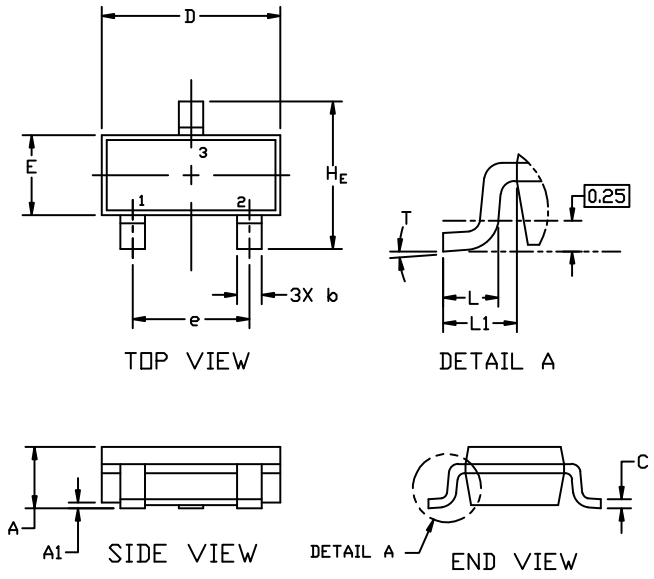
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS



SCALE 4:1

SOT−23 (TO−236)
CASE 318
ISSUE AT

DATE 01 MAR 2023

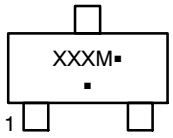


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M,1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF THE BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

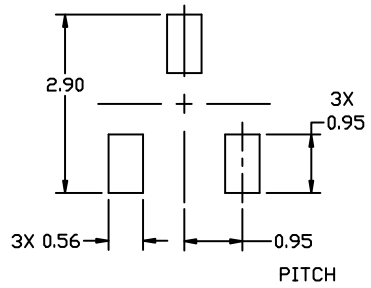
	MILLIMETERS			INCHES		
DIM	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.89	1.00	1.11	0.035	0.039	0.044
A1	0.01	0.06	0.10	0.000	0.002	0.004
b	0.37	0.44	0.50	0.015	0.017	0.020
c	0.08	0.14	0.20	0.003	0.006	0.008
D	2.80	2.90	3.04	0.110	0.114	0.120
E	1.20	1.30	1.40	0.047	0.051	0.055
e	1.78	1.90	2.04	0.070	0.075	0.080
L	0.30	0.43	0.55	0.012	0.017	0.022
L1	0.35	0.54	0.69	0.014	0.021	0.027
H_E	2.10	2.40	2.64	0.083	0.094	0.104
T	0°	---	10°	0°	---	10°

GENERIC MARKING DIAGRAM*



XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.



RECOMMENDED
MOUNTING FOOTPRINT

* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

STYLES ON PAGE 2

DOCUMENT NUMBER:	**98ASB42226B**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.	
DESCRIPTION:	**SOT−23 (TO−236)**		**PAGE 1 OF 2**

SOT−23 (TO−236)
CASE 318
ISSUE AT

DATE 01 MAR 2023

STYLE 1 THRU 5:
CANCELLED

STYLE 6:
PIN 1. BASE
2. EMITTER
3. COLLECTOR

STYLE 7:
PIN 1. EMITTER
2. BASE
3. COLLECTOR

STYLE 8:
PIN 1. ANODE
2. NO CONNECTION
3. CATHODE

STYLE 9:
PIN 1. ANODE
2. ANODE
3. CATHODE

STYLE 10:
PIN 1. DRAIN
2. SOURCE
3. GATE

STYLE 11:
PIN 1. ANODE
2. CATHODE
3. CATHODE−ANODE

STYLE 12:
PIN 1. CATHODE
2. CATHODE
3. ANODE

STYLE 13:
PIN 1. SOURCE
2. DRAIN
3. GATE

STYLE 14:
PIN 1. CATHODE
2. GATE
3. ANODE

STYLE 15:
PIN 1. GATE
2. CATHODE
3. ANODE

STYLE 16:
PIN 1. ANODE
2. CATHODE
3. CATHODE

STYLE 17:
PIN 1. NO CONNECTION
2. ANODE
3. CATHODE

STYLE 18:
PIN 1. NO CONNECTION
2. CATHODE
3. ANODE

STYLE 19:
PIN 1. CATHODE
2. ANODE
3. CATHODE−ANODE

STYLE 20:
PIN 1. CATHODE
2. ANODE
3. GATE

STYLE 21:
PIN 1. GATE
2. SOURCE
3. DRAIN

STYLE 22:
PIN 1. RETURN
2. OUTPUT
3. INPUT

STYLE 23:
PIN 1. ANODE
2. ANODE
3. CATHODE

STYLE 24:
PIN 1. GATE
2. DRAIN
3. SOURCE

STYLE 25:
PIN 1. ANODE
2. CATHODE
3. GATE

STYLE 26:
PIN 1. CATHODE
2. ANODE
3. NO CONNECTION

STYLE 27:
PIN 1. CATHODE
2. CATHODE
3. CATHODE

STYLE 28:
PIN 1. ANODE
2. ANODE
3. ANODE

ADDITIONAL INFORMATION

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