

MOSFET – N-Channel Enhancement Mode Field Effect Transistor

60 V, 0.28 A, 2 Ω

2N7002V/2N7002VA

Features

- Dual N-Channel MOSFET
- Low On-Resistance
- Low Gate Threshold Voltage
- Low Input Capacitance
- Fast Switching Speed
- Low Input/Output Leakage
- Ultra-Small Surface Mount Package
- This Device is Pb-Free, Halide Free and RoHS Compliant

MOSFET MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

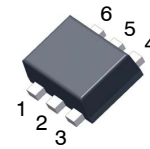
Symbol	Parameter		Ratings	Unit
V _{DSS}	Drain – Source Voltage		60	V
V _{DGR}	Gate – Gate Voltage (R _{GS} ≤ 1.0 MΩ)		60	V
V _{GSS}	Gate–Source Voltage	– Continuous	±20	V
		– Pulsed	±40	
I _D	Drain Current	– Continuous	280	mA
		– Pulsed	1.5	A
T _J , T _{STG}	Junction and Storage Temperature Range		–55 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Ratings	Unit
P _D	Total Device Dissipation	250	mW
	Derate Above T _A = 25°C	2.0	mW/°C
R _{θJA}	Thermal Resistance, Junction-to-Ambient (Note 1)	500	°C/W

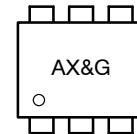
1. Device mounted on FR-4 PCB, 1 inch x 0.85 inch x 0.062 inch. Minimum land pad size.



SOT-563
CASE 419BH

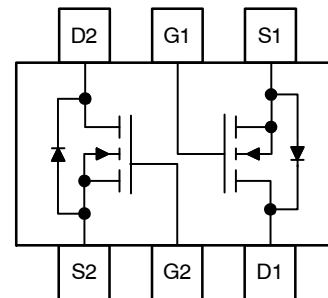
*Pin 1 and Pin 4 are exchangeable.

MARKING DIAGRAM

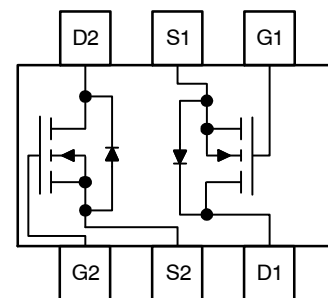


AX = Device Code (X = B or C)
&G = 1-Digit Weekly Date Code

PIN ASSIGNMENT



2N7002V



2N7002VA

ORDERING INFORMATION

See detailed ordering and shipping information on page 4 of this data sheet.

2N7002V/2N7002VA

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

BV_{DSS}	Drain to Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 10\text{ }\mu\text{A}$	60	78	–	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 60\text{ V}, V_{GS} = 0\text{ V}$	–	0.001	1.0	μA
		$V_{DS} = 60\text{ V}, V_{GS} = 0\text{ V}, T_J = 125^\circ$		7	500	
I_{GSS}	Gate–Body Leakage	$V_{GS} = \pm 20\text{ V}, V_{DS} = 0\text{ V}$	–	0.2	± 100	nA

ON CHARACTERISTICS (Note 2)

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	1.00	1.76	2.50	V
$R_{DS(on)}$	Static Drain–Source On–Resistance	$V_{GS} = 5\text{ V}, I_D = 0.05\text{ A}$	–	1.6	7.5	Ω
		$V_{GS} = 10\text{ V}, I_D = 0.5\text{ A}$	–	–	2.0	
		$V_{GS} = 10\text{ V}, I_D = 0.5\text{ A}, T_J = 125^\circ\text{C}$	–	2.53	13.5	
$I_{D(on)}$	On–State Drain Current	$V_{GS} = 10\text{ V}, V_{DS} = 7.5\text{ V}$	1.50	1.43	–	A
g_{FS}	Forward Transconductance	$V_{DS} = 10\text{ V}, I_D = 0.2\text{ A}$	80	356.5	–	mS

DYNAMIC CHARACTERISTICS

C_{iss}	Input Capacitance	$V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V}, f = 1.0\text{ MHz}$	–	37.8	50	pF
C_{oss}	Output Capacitance		–	12.4	25	pF
C_{rss}	Reverse Transfer Capacitance		–	6.5	7	pF

SWITCHING CHARACTERISTICS

$t_{d(on)}$	Turn–On Delay Time	$V_{DD} = 30\text{ V}, I_D = 0.2\text{ A}, V_{GEN} = 10\text{ V},$ $R_L = 150\text{ }\Omega, R_{GEN} = 25\text{ }\Omega$	–	5.85	20	ns
$t_{d(off)}$	Turn–Off Delay Time		–	12.5	20	ns

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Short duration test pulse used to minimize self–heating effect.

TYPICAL PERFORMANCE CHARACTERISTICS

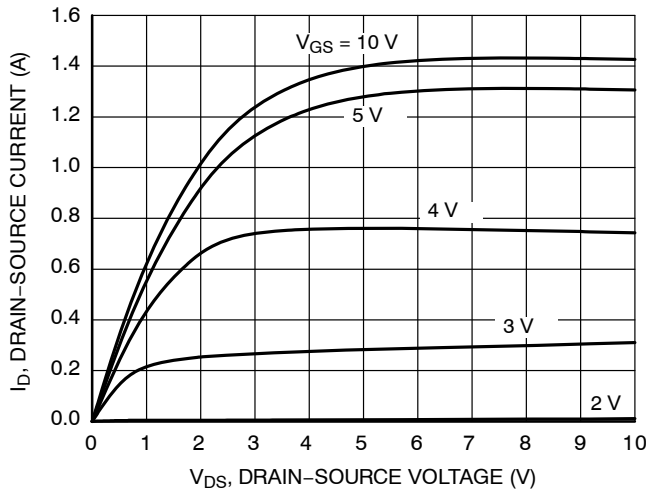


Figure 1. On - Region Characteristics

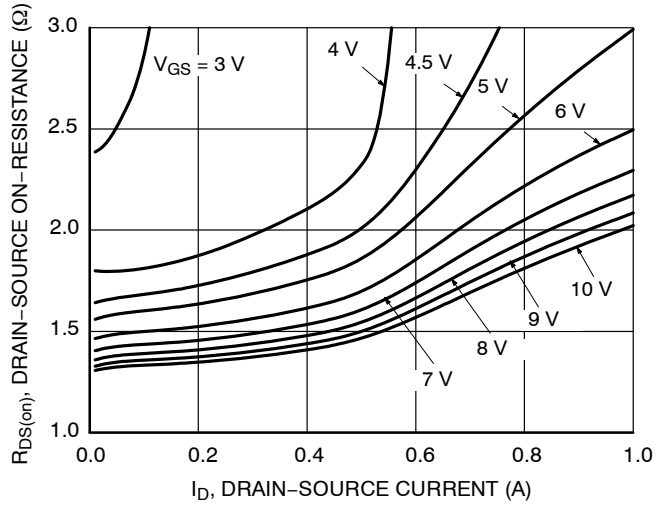


Figure 2. On-Resistance Variation with Gate Voltage and Drain Current

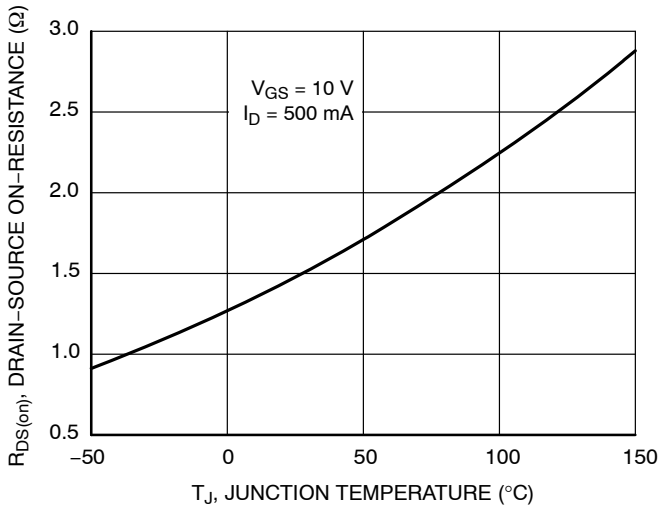


Figure 3. On-Resistance Variation with Temperature

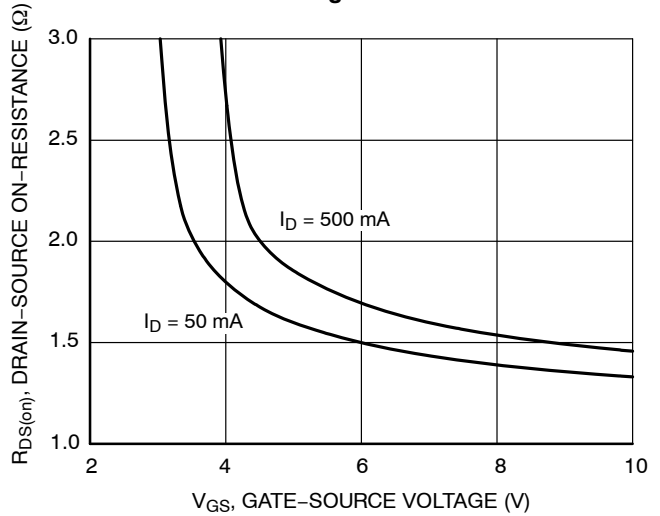


Figure 4. On-Resistance Variation with Gate-Source Voltage

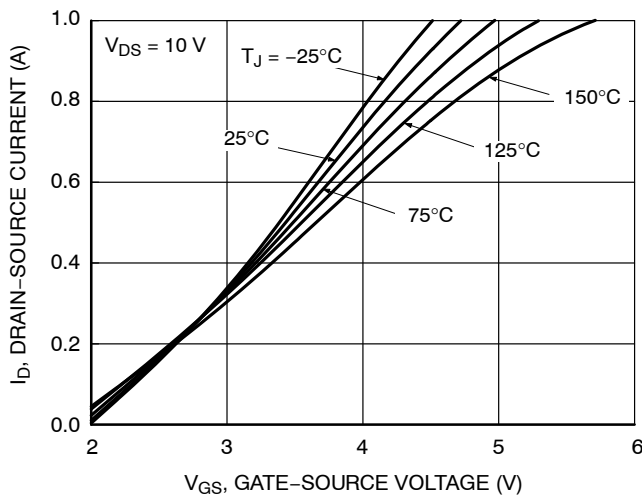


Figure 5. Transfer Characteristics

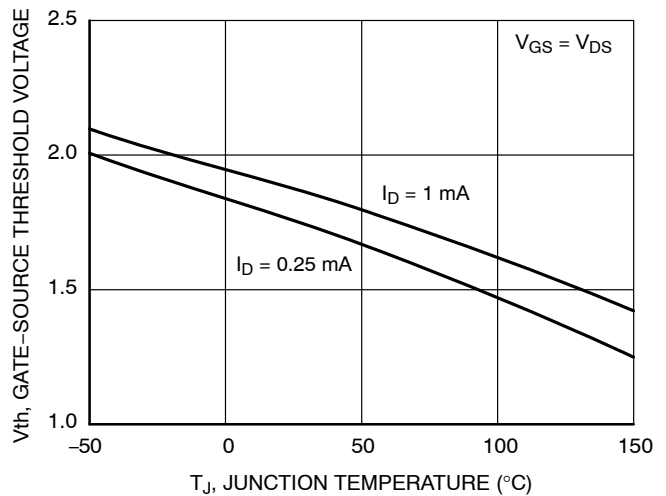


Figure 6. Gate Threshold Variation with Temperature

TYPICAL ELECTRICAL CHARACTERISTICS (continued)

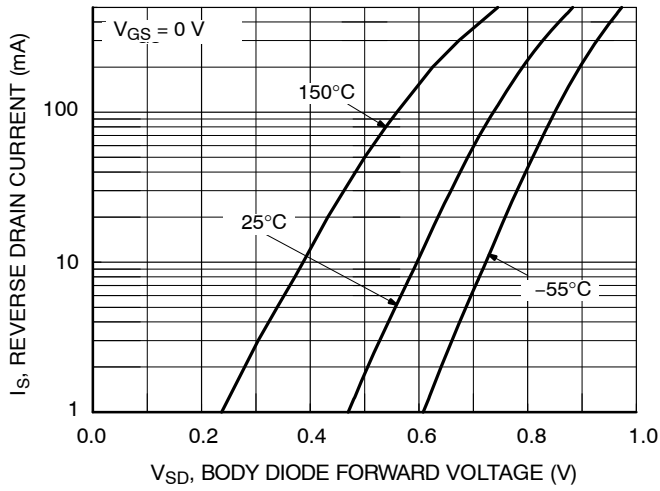


Figure 7. Reverse Drain Current Variation with Diode Forward Voltage and Temperature

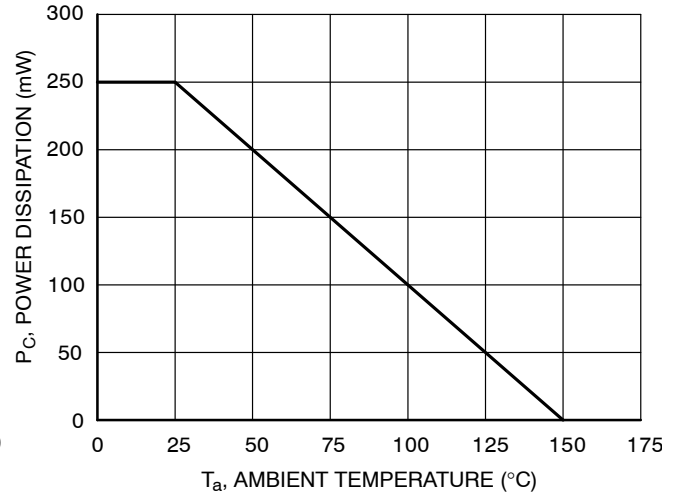


Figure 8. Power Derating

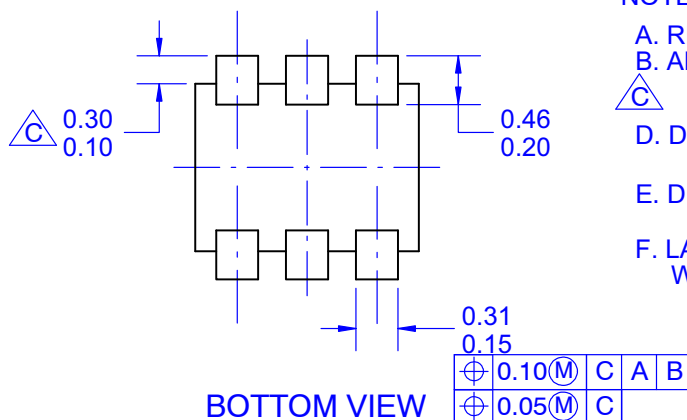
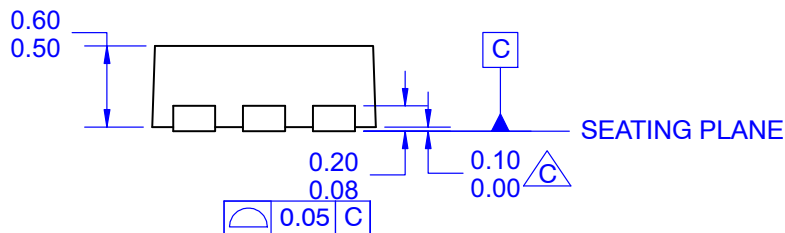
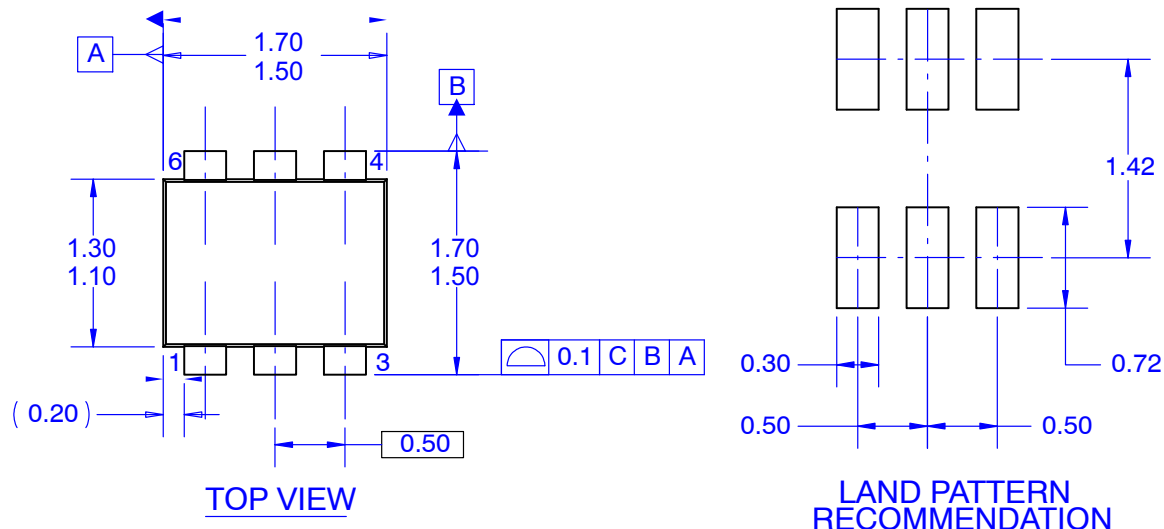
PACKAGE MARKING AND ORDERING INFORMATION

Device	Device Marking	Package	Shipping [†]
2N7002V	AB	SOT-563 (Pb-Free)	3000 / Tape & Reel
2N7002VA	AC	SOT-563 (Pb-Free)	3000 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

ON

DATE 31 AUG 2016



NOTES: UNLESS OTHERWISE SPECIFIED.

A. REFERENCE TO JEDEC MO293.

B. ALL DIMENSIONS ARE IN MILLIMETERS.


 DOES NOT COMPLY JEDEC STANDARD VALUE.

D. DIMENSIONS ARE EXCLUSIVE OF BURRS,
MOLD FLASH AND TIE BAR PROTRUSION.

E. DIMENSION AND TOLERANCE AS PER ASME Y14.5-2009.

F. LANDPATTERN RECOMMENDATION GENERATED WITH IPC LANDPATTERN GENERATOR

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