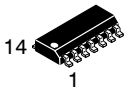
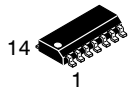
# Hex Inverter

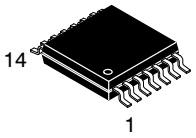
# 74AC04, 74ACT04




SOIC−14 NB
CASE 751A−03




SOIC14
CASE 751EF




TSSOP−14 WB
CASE 948G

### General Description

The AC/ACT04 contains six inverters.

### Features

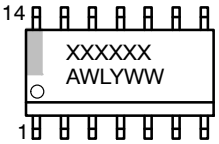
- $I_{CC}$ Reduced by 50% On 74AC Only
- Outputs Source/Sink 24 mA
- ACT04 has TTL−Compatible Inputs
- These are Pb−Free Devices

### ABSOLUTE MAXIMUM RATINGS

| Parameter | Symbol | Value | Unit |
|---|---|---|---|
| Supply Voltage | $V_{CC}$ | −0.5 to +6.5 | V |
| DC Input Diode Current<br>$V_I$ = −0.5 V<br>$V_I$ = $V_{CC}$ + 0.5 V | $I_{IK}$ | <br>−20<br>+20 | mA |
| DC Input Voltage | $V_I$ | −0.5 to<br>$V_{CC}$ + 0.5 | V |
| DC Output Diode Current<br>$V_O$ = −0.5 V<br>$V_O$ = $V_{CC}$ + 0.5 V | $I_{OK}$ | <br>−20<br>+20 | mA |
| DC Output Voltage | $V_O$ | −0.5 to<br>$V_{CC}$ + 0.5 | V |
| DC Output Source or Sink Current | $I_O$ | ±50 | mA |
| DC $V_{CC}$ or Ground Current per Output Pin | $I_{CC}$ or $I_{GND}$ | ±50 | mA |
| Storage Temperature Range | $T_{STG}$ | −65 to +150 | °C |
| Junction Temperature | $T_J$ | 140 | °C |

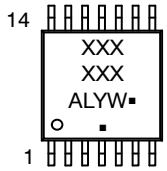
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

### MARKING DIAGRAM




| | |
|---|---|
| XXXXXX | = Specific Device Code |
| A | = Assembly Location |
| WL | = Wafer Lot |
| Y | = Year |
| WW | = Work Week |

### MARKING DIAGRAM




| | |
|---|---|
| XXXXXX | = Specific Device Code |
| A | = Assembly Location |
| L | = Wafer Lot |
| Y | = Year |
| W | = Work Week |
| ▪ | = Pb−Free Package |

(Note: Microdot may be in either location)

### ORDERING INFORMATION

See detailed ordering and shipping information on page 5 of this data sheet.

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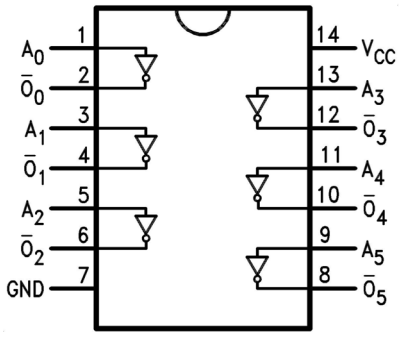


**Figure 1. Connection Diagram**

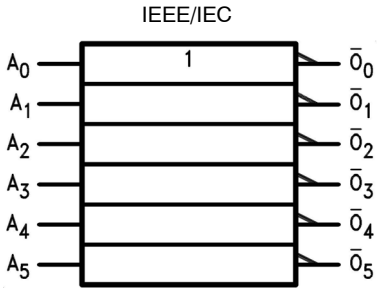


**Figure 2. Logic Symbol**

## PIN DESCRIPTION

| Pin | Description |
|---|---|
| $A_n$ | Inputs |
| $\overline{O}_n$ | Outputs |

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage<br>AC<br>ACT | <br>2.0<br>4.5 | <br>6.0<br>5.5 | V |
| $V_I$ | Input Voltage | 0 | $V_{CC}$ | V |
| $V_O$ | Output Voltage | 0 | $V_{CC}$ | V |
| $T_A$ | Operating Temperature | −40 | +85 | °C |
| $\Delta V / \Delta t$ | Minimum Input Edge Rate, AC Devices:<br>$V_{IN}$ from 30% to 70% of $V_{CC}$, $V_{CC}$ at 3.3 V, 4.5 V, 5.5 V | 125 | | mV/ns |
| $\Delta V / \Delta t$ | Minimum Input Edge Rate, ACT Devices:<br>$V_{IN}$ from 0.8 V to 2.0 V, $V_{CC}$ at 4.5 V, 5.5 V | 125 | | mV/ns |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.



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## DC ELECTRICAL CHARACTERISTICS FOR AC

| Symbol | Parameter | $V_{CC}$(V) | Conditions | $T_A$ = +25°C | $T_A$ = −40°C to +85°C | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Typ | Guaranteed Limits | | |
| $V_{IH}$ | Minimum HIGH Level Input Voltage | 3.0 | $V_{OUT}$ = 0.1 V or $V_{CC}$ − 0.1 V | 1.5 | 2.1 | 2.1 | V |
| | | 4.5 | | 2.25 | 3.15 | 3.15 | |
| | | 5.5 | | 2.75 | 3.85 | 3.85 | |
| $V_{IL}$ | Maximum LOW Level Input Voltage | 3.0 | $V_{OUT}$ = 0.1 V or $V_{CC}$ − 0.1 V | 1.5 | 0.9 | 0.9 | V |
| | | 4.5 | | 2.25 | 1.35 | 1.35 | |
| | | 5.5 | | 2.75 | 1.65 | 1.65 | |
| $V_{OH}$ | Minimum HIGH Level Output Voltage | 3.0 | $I_{OUT}$ = −50 μA | 2.99 | 2.9 | 2.9 | V |
| | | 4.5 | | 4.49 | 4.4 | 4.4 | |
| | | 5.5 | | 5.49 | 5.4 | 5.4 | |
| | | 3.0 | $V_{IN}$ = $V_{IL}$ or $V_{IH}$, $I_{OH}$ = −12 mA | – | 2.56 | 2.46 | |
| | | 4.5 | $I_{OH}$ = −24 mA | – | 3.86 | 3.76 | |
| | | 5.5 | $I_{OH}$ = −24 mA (Note 1) | – | 4.86 | 4.76 | |
| $V_{OL}$ | Maximum LOW Level Output Voltage | 3.0 | $I_{OUT}$ = 50 μA | 0.002 | 0.1 | 0.1 | V |
| | | 4.5 | | 0.001 | 0.1 | 0.1 | |
| | | 5.5 | | 0.001 | 0.1 | 0.1 | |
| | | 3.0 | $V_{IN}$ = $V_{IL}$ or $V_{IH}$, $I_{OL}$ = 12 mA | – | 0.36 | 0.44 | |
| | | 4.5 | $I_{OL}$ = 24 mA | – | 0.36 | 0.44 | |
| | | 5.5 | $I_{OL}$ = 24 mA (Note 1) | – | 0.36 | 0.44 | |
| $I_{IN}$ (Note 3) | Maximum Input Leakage Current | 5.5 | $V_I$ = $V_{CC}$, GND | – | ±0.1 | ±1.0 | μA |
| $I_{OLD}$ | Minimum Dynamic Output Current (Note 2) | 5.5 | $V_{OLD}$ = 1.65 V Max. | – | – | 75 | mA |
| $I_{OHD}$ | | 5.5 | $V_{OHD}$ = 3.85 V Min. | – | – | −75 | mA |
| $I_{CC}$ (Note 3) | Maximum Quiescent Supply Current | 5.5 | $V_{IN}$ = $V_{CC}$ or GND | – | 2.0 | 20.0 | μA |

1. All outputs loaded; thresholds on input associated with output under test.
2. Maximum test duration 2.0 ms, one output loaded at a time.
3. $I_{IN}$ and $I_{CC}$ at 3.0 V are guaranteed to be less than or equal to the respective limit at 5.5 V $V_{CC}$.



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## DC ELECTRICAL CHARACTERISTICS FOR ACT

| Symbol | Parameter | $V_{CC}$(V) | Conditions | $T_A$ = +25°C | $T_A$ = −40°C to +85°C | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Typ | Guaranteed Limits | | |
| $V_{IH}$ | Minimum HIGH Level Input Voltage | 4.5 | $V_{OUT}$ = 0.1 V or $V_{CC}$ − 0.1 V | 1.5 | 2.0 | 2.0 | V |
| | | 5.5 | | 1.5 | 2.0 | 2.0 | |
| $V_{IL}$ | Maximum LOW Level Input Voltage | 4.5 | $V_{OUT}$ = 0.1 V or $V_{CC}$ − 0.1 V | 1.5 | 0.8 | 0.8 | V |
| | | 5.5 | | 1.5 | 0.8 | 0.8 | |
| $V_{OH}$ | Minimum HIGH Level Output Voltage | 4.5 | $I_{OUT}$ = −50 μA | 4.49 | 4.4 | 4.4 | V |
| | | 5.5 | | 5.49 | 5.4 | 5.4 | |
| | | 4.5 | $V_{IN}$ = $V_{IL}$ or $V_{IH}$<br>$I_{OH}$ = −24 mA | – | 3.86 | 3.76 | |
| | | 5.5 | $I_{OH}$ = −24 mA (Note 4) | – | 4.86 | 4.76 | |
| $V_{OL}$ | Maximum LOW Level Output Voltage | 4.5 | $I_{OUT}$ = 50 μA | 0.001 | 0.1 | 0.1 | V |
| | | 5.5 | | 0.001 | 0.1 | 0.1 | |
| | | 4.5 | $V_{IN}$ = $V_{IL}$ or $V_{IH}$<br>$I_{OL}$ = 24 mA | – | 0.36 | 0.44 | |
| | | 5.5 | $I_{OL}$ = 24 mA (Note 4) | – | 0.36 | 0.44 | |
| $I_{IN}$ | Maximum Input Leakage Current | 5.5 | $V_I$ = $V_{CC}$, GND | – | ±0.1 | ±1.0 | μA |
| $I_{CCT}$ | Maximum $I_{CC}$/Input | 5.5 | $V_I$ = $V_{CC}$ − 2.1 V | 0.6 | – | 1.5 | mA |
| $I_{OLD}$ | Minimum Dynamic Output Current (Note 5) | 5.5 | $V_{OLD}$ = 1.65 V Max. | – | – | 75 | mA |
| $I_{OHD}$ | | 5.5 | $V_{OHD}$ = 3.85 V Min. | – | – | −75 | mA |
| $I_{CC}$ | Maximum Quiescent Supply Current | 5.5 | $V_{IN}$ = $V_{CC}$ or GND | – | 4.0 | 40.0 | μA |

4. All outputs loaded; thresholds on input associated with output under test.
5. Maximum test duration 2.0 ms, one output loaded at a time.



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## AC ELECTRICAL CHARACTERISTICS FOR AC

| Symbol | Parameter | $V_{CC}$(V) (Note 6) | $T_A$ = +25°C, $C_L$ = 50 pF | | | $T_A$ = −40°C to +85°C, $C_L$ = 50 pF | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Max | |
| $t_{PLH}$ | Propagation Delay | 3.3 | 1.5 | 4.5 | 9.0 | 1.0 | 10.0 | ns |
| | | 5.0 | 1.5 | 4.0 | 7.0 | 1.0 | 7.5 | |
| $t_{PHL}$ | Propagation Delay | 3.3 | 1.5 | 4.5 | 8.5 | 1.0 | 9.5 | ns |
| | | 5.0 | 1.5 | 3.5 | 6.5 | 1.0 | 7.0 | |

6. Voltage range 3.3 is 3.3 V + 0.3 V. Voltage range 5.0 is 5.0 V + 0.5 V.

## AC ELECTRICAL CHARACTERISTICS FOR ACT

| Symbol | Parameter | $V_{CC}$(V) (Note 7) | $T_A$ = +25°C, $C_L$ = 50 pF | | | $T_A$ = −40°C to +85°C, $C_L$ = 50 pF | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Max | |
| $t_{PLH}$ | Propagation Delay | 5.0 | 1.0 | 6.0 | 8.5 | 1.0 | 9.0 | ns |
| $t_{PLH}$ | Propagation Delay | 5.0 | 1.0 | 5.5 | 8.0 | 1.0 | 8.5 | ns |

7. Voltage range 5.0 is 5.0 V + 0.5 V.

## CAPACITANCE

| Symbol | Parameter | Conditions | Typ | Unit |
|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $V_{CC}$ = OPEN | 4.5 | pF |
| $V_{CC}$ | Power Dissipation Capacitance | $V_{CC}$ = 5.0 V | 30.0 | pF |

## ORDERING INFORMATION

| Order Number | Marking | Package | Shipping† |
|---|---|---|---|
| 74AC04SC | AC04G | SOIC−14 | 55 Units / Rail |
| 74AC04SCX | AC04G | SOIC−14 | 2500 / Tape & Reel |
| 74ACT04MTC | ACT<br>04 | TSSOP−14 | 96 Units / Rail |
| 74AC04MTCX | AC<br>04 | TSSOP−14 | 2500 / Tape & Reel |
| 74ACT04SC | ACT04G | SOIC−14 | 55 Units / Rail |
| 74ACT04SCX | ACT04G | SOIC−14 | 2500 / Tape & Reel |
| 74ACT04MTCX | ACT<br>04 | TSSOP−14 | 2500 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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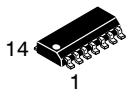
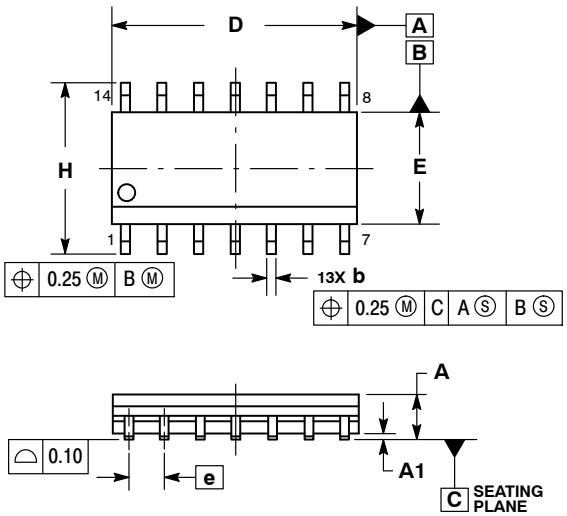
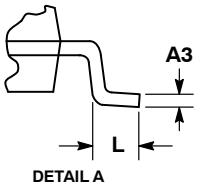


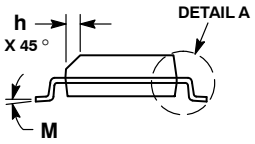

**SCALE 1:1**

**SOIC−14 NB**
CASE 751A−03
ISSUE L

DATE 03 FEB 2016



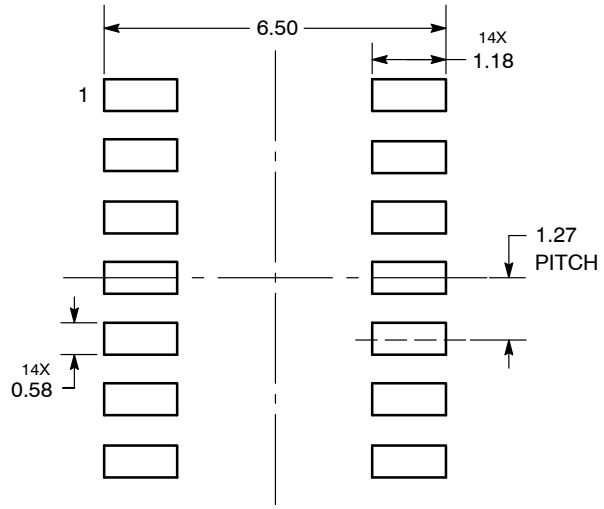




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 1.35 | 1.75 | 0.054 | 0.068 |
| A1 | 0.10 | 0.25 | 0.004 | 0.010 |
| A3 | 0.19 | 0.25 | 0.008 | 0.010 |
| b | 0.35 | 0.49 | 0.014 | 0.019 |
| D | 8.55 | 8.75 | 0.337 | 0.344 |
| E | 3.80 | 4.00 | 0.150 | 0.157 |
| e | 1.27 BSC | | 0.050 BSC | |
| H | 5.80 | 6.20 | 0.228 | 0.244 |
| h | 0.25 | 0.50 | 0.010 | 0.019 |
| L | 0.40 | 1.25 | 0.016 | 0.049 |
| M | 0 ° | 7 ° | 0 ° | 7 ° |

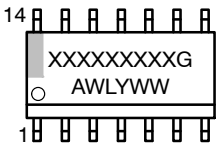
## SOLDERING FOOTPRINT*




DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

## GENERIC MARKING DIAGRAM*




XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

**STYLES ON PAGE 2**

| | | | |
|---|---|---|---|
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| **DESCRIPTION:** | **SOIC−14 NB** | | **PAGE 1 OF 2** |

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**SOIC−14**
CASE 751A−03
ISSUE L

DATE 03 FEB 2016

STYLE 1:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. NO CONNECTION
5. ANODE/CATHODE
6. NO CONNECTION
7. ANODE/CATHODE
8. ANODE/CATHODE
9. ANODE/CATHODE
10. NO CONNECTION
11. ANODE/CATHODE
12. ANODE/CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 2:
CANCELLED

STYLE 3:
PIN 1. NO CONNECTION
2. ANODE
3. ANODE
4. NO CONNECTION
5. ANODE
6. NO CONNECTION
7. ANODE
8. ANODE
9. ANODE
10. NO CONNECTION
11. ANODE
12. ANODE
13. NO CONNECTION
14. COMMON CATHODE

STYLE 4:
PIN 1. NO CONNECTION
2. CATHODE
3. CATHODE
4. NO CONNECTION
5. CATHODE
6. NO CONNECTION
7. CATHODE
8. CATHODE
9. CATHODE
10. NO CONNECTION
11. CATHODE
12. CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 5:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. ANODE/CATHODE
5. ANODE/CATHODE
6. NO CONNECTION
7. COMMON ANODE
8. COMMON CATHODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. ANODE/CATHODE
12. ANODE/CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 6:
PIN 1. CATHODE
2. CATHODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE
7. CATHODE
8. ANODE
9. ANODE
10. ANODE
11. ANODE
12. ANODE
13. ANODE
14. ANODE

STYLE 7:
PIN 1. ANODE/CATHODE
2. COMMON ANODE
3. COMMON CATHODE
4. ANODE/CATHODE
5. ANODE/CATHODE
6. ANODE/CATHODE
7. ANODE/CATHODE
8. ANODE/CATHODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. COMMON CATHODE
12. COMMON ANODE
13. ANODE/CATHODE
14. ANODE/CATHODE

STYLE 8:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. NO CONNECTION
5. ANODE/CATHODE
6. ANODE/CATHODE
7. COMMON ANODE
8. COMMON ANODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. NO CONNECTION
12. ANODE/CATHODE
13. ANODE/CATHODE
14. COMMON CATHODE




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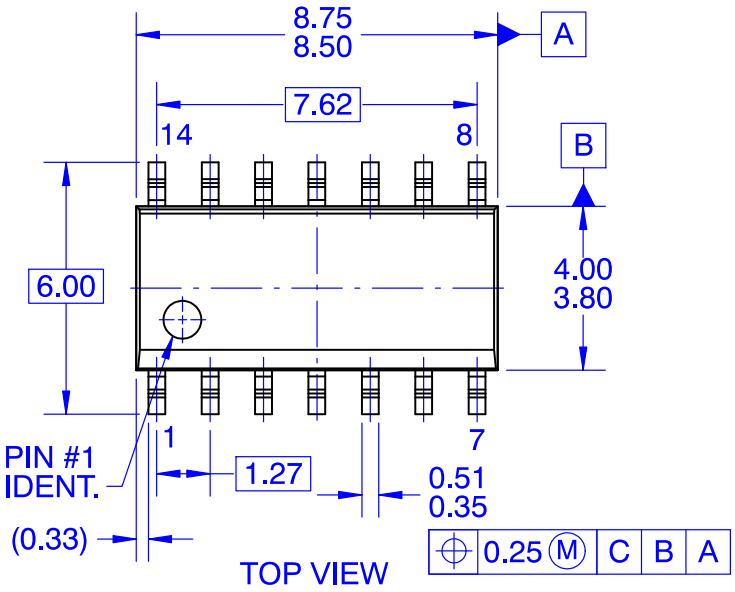
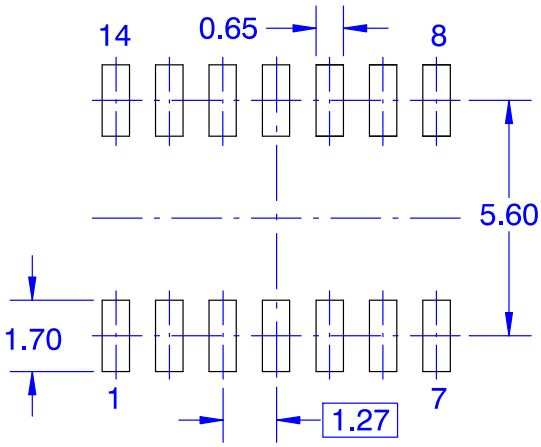
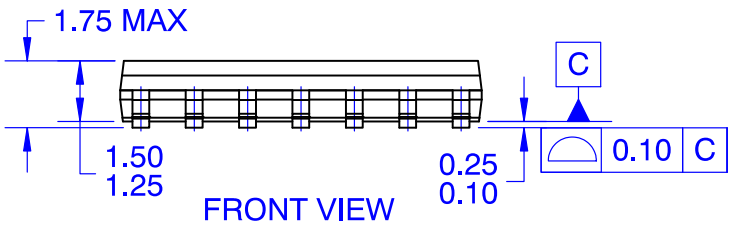


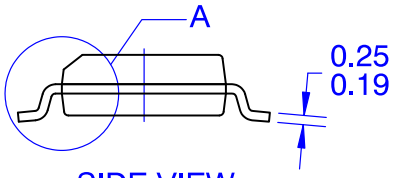

TOP VIEW




LAND PATTERN RECOMMENDATION

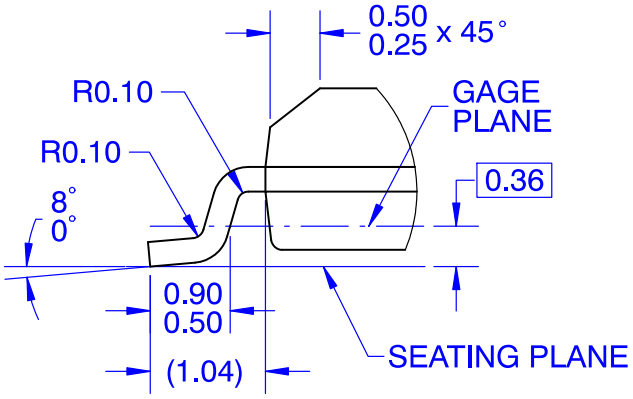



FRONT VIEW




SIDE VIEW

NOTES:
A. CONFORMS TO JEDEC MS−012, VARIATION AB, ISSUE C
B. ALL DIMENSIONS ARE IN MILLIMETERS
C. DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS
D. LAND PATTERN STANDARD: SOIC127P600X145−14M
E. CONFORMS TO ASME Y14.5M, 2009




DETAIL A
SCALE 16 : 1

| | | |
|---|---|---|
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| **DESCRIPTION:** | **SOIC14** | **PAGE 1 OF 1** |

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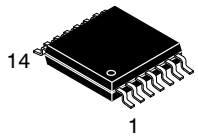
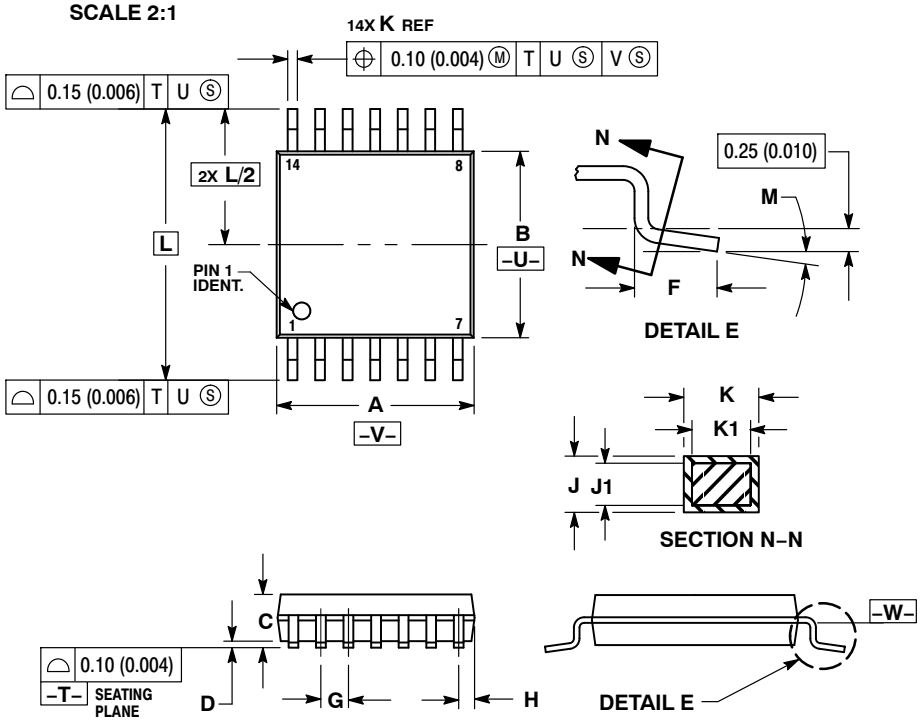



SCALE 2:1

**TSSOP−14 WB**
CASE 948G
ISSUE C

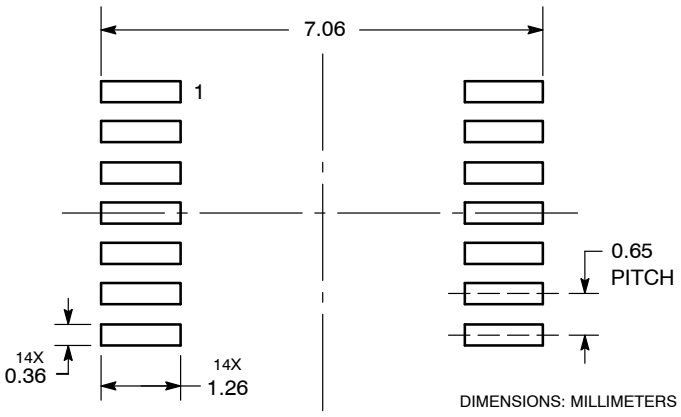
DATE 17 FEB 2016




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 4.90 | 5.10 | 0.193 | 0.200 |
| B | 4.30 | 4.50 | 0.169 | 0.177 |
| C | −−− | 1.20 | −−− | 0.047 |
| D | 0.05 | 0.15 | 0.002 | 0.006 |
| F | 0.50 | 0.75 | 0.020 | 0.030 |
| G | 0.65 BSC | | 0.026 BSC | |
| H | 0.50 | 0.60 | 0.020 | 0.024 |
| J | 0.09 | 0.20 | 0.004 | 0.008 |
| J1 | 0.09 | 0.16 | 0.004 | 0.006 |
| K | 0.19 | 0.30 | 0.007 | 0.012 |
| K1 | 0.19 | 0.25 | 0.007 | 0.010 |
| L | 6.40 BSC | | 0.252 BSC | |
| M | 0 ° | 8 ° | 0 ° | 8 ° |

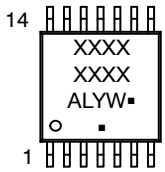
## RECOMMENDED SOLDERING FOOTPRINT*




DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

## GENERIC MARKING DIAGRAM*




| | |
|---|---|
| A | = Assembly Location |
| L | = Wafer Lot |
| Y | = Year |
| W | = Work Week |
| ▪ | = Pb−Free Package |

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

| | | |
|---|---|---|
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| **DESCRIPTION:** | **TSSOP−14 WB** | **PAGE 1 OF 1** |

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