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Low Voltage Quad Buffer with 5 V Tolerant Inputs and Outputs

74LCX125

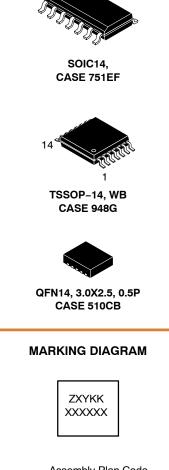
Description

The LCX125 contains four independent non-inverting buffers with 3–STATE outputs. The inputs tolerate Voltages up to 5.5 V Allowing the interface of 5 V Systems to 3 V Systems.

The 74LCX125 is fabricated with an advanced CMOS technology to achieve high Speed operation while Maintaining CMOS Low Power Dissipation.

Features

- 5 V Tolerant Inputs and Outputs
- 1.65 V–5.5 V V_{CC} Specifications Provided
- 6.0 ns t_{PD} max. (V_{CC} = 3.3 V), 10 μ A I_{CC} max.
- Power Down High Impedance Inputs and Outputs
- Supports Live Insertion/Withdrawal*
- ± 24 mA Output Drive (V_{CC} = 3.0 V)
- Latch-up Performance Exceeds JEDEC 78 Conditions
- ESD Performance:
 - ♦ Human body model > 2000 V
- Pb-Free DQFN Package
- These are Pb-Free Devices
- *To ensure the High–Impedance State During Power up or down, $\overline{\text{OE}}$ Should be tied to V_{CC} through a pull–up resistor: the minimum value of the resistor is determined by the current–sourcing capability of the driver.



Z	= Assembly Plan Code
XY	= Date Code (Year & Week)
KK	= Lot Run Traceability Code
XXXXXX	= Specific Device Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 7 of this data sheet.

Connection Diagrams

Pin Assignments for SOIC, SOP, and TSSOP

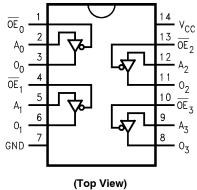
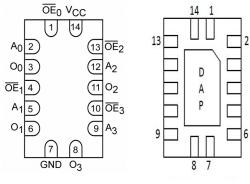


Figure 1.

Pad Assignments for DQFN



(Top Through View)

Figure 3.

(Bottom View)

Table 1. PIN DESCRIPTION

Pin Names	Description
A _n	Inputs
OE _n	Output Enable Inputs
O _n	Outputs
DAP	No Connect

NOTE: Die Attach Pad (DIE)



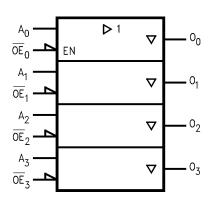


Figure 2. Logic Symbol

TRUTH	TABLE

Inp	Outputs	
OEn	A _n	O _n
L	L	L
L	н	Н
Н	Х	Z

H = HIGH Voltage Level L = HIGH Voltage Level Z = HIGH Impedance

L = HIGH Volta Z = HIGH Impe X = Immaterial

MAXIMUM RATINGS

Symbol	Parameter	Value	Unit	
V _{CC}	DC Supply Voltage		-0.5 to +6.5	V
VI	DC Input Voltage (Note 1)		–0.5 to +6.5	V
Vo	DC Output Voltage (Note 1)	Active-Mode (High or Low State) Tri-State Mode Power-Down Mode (V _{CC} = 0 V)	-0.5 to V _{CC} + 0.5 -0.5 to +6.5 -0.5 to +6.5	V
I _{IK}	DC Input Diode Current	V _I < GND	-50	mA
Ι _{ΟΚ}	DC Output Diode Current	V _O < GND	-50	mA
lo	DC Output Source/Sink Current		±50	mA
I _{CC} or I _{GND}	DC Supply Current per Supply Pin or Ground Pin		±100	mA
T _{STG}	Storage Temperature Range		-65 to +150	°C
ΤL	Lead Temperature, 1 mm from Case for 10 secs		260	°C
ТJ	Junction Temperature Under Bias		+150	°C
θ_{JA}	Thermal Resistance (Note 1)	SOIC-14 QFN14 TSSOP-14	116 130 150	°C/W
PD	Power Dissipation in Still Air at 125°C	SOIC-14 QFN14 TSSOP-14	1077 962 833	mW
MSL	Moisture Sensitivity		Level 1	-
F _R	Flammability Rating	Oxygen Index: 28 to 34	UL 94 V-0 @ 0.125 in	-
V_{ESD}	ESD Withstand Voltage (Note 3)	Human Body Model Charged Device Model	2000 N/A	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected. 1. I_O absolute maximum rating must be observed.

 Measured with minimum pad spacing on an FR4 board, using 76 mm-by-114 mm, 2-ounce copper trace no air flow per JESD51 – 7.
 HBM tested to EIA / JESD22-A114-A. CDM tested to JESD22-C101-A. JEDEC recommends that ESD qualification to EIA/JESD22-A115A (Machine Model) be discontinued.

RECOMMENDED OPERATING CONDITIONS

Symbol		Parameter				Unit
V _{CC}	Supply Voltage	Operating Data Retention Only	1.65 1.5	3.3 3.3	5.5 5.5	V
VI	Digital Input Voltage		0	_	5.5	V
Vo	Output Voltage	Active Mode (High or Low State) Tri-State Mode Power Down Mode (V _{CC} = 0 V)	0 0 0		V _{CC} 5.5 5.5	V
T _A	Operating Free-Air Temperature		-40	-	+125	°C
t _r , t _f	Input Rise or Fall Rate	$\label{eq:V_CC} \begin{array}{l} V_{CC} = 1.65 \; V \; to \; 1.95 \; V \\ V_{CC} = 2.3 \; V \; to \; 2.7 \; V \\ V_I \; \text{from 0.8 } V \; \text{to } 2.0 \; V, \; V_{CC} = 3.0 \; V \\ V_{CC} = 4.5 \; V \; \text{to } 5.5 \; V \end{array}$	0 0 0 0	- - -	20 20 10 5	nS/V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

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DC ELECTRICAL CHARACTERISTICS

				T _A = -40 °C	C to +85 °C	T _A = -40 °C	to +125 °C	
Symbol	Parameter	Conditions	V _{CC} (V)	Min	Мах	Min	Max	Unit
V _{IH}	HIGH Level Input Voltage		1.65 — 1.95	0.65 x V _{CC}	-	0.65 x V _{CC}	-	V
			2.3 – 2.7	1.7	-	1.7	-	
			3.0 - 3.6	2.0	-	2.0	-	
			4.5 – 5.5	0.70 x V _{CC}	-	0.70 x V _{CC}	-	
V _{IL}	LOW Level Input Voltage		1.65 — 1.95	-	0.35 x V _{CC}	-	0.35 x V _{CC}	V
			2.3 – 2.7	-	0.7	-	0.7	
			3.0 - 3.6	-	0.8	-	0.8	
			4.5 – 5.5	-	0.30 x V _{CC}	_	0.30 x V _{CC}	
V _{OH}	High-Level Output Voltage	$ \begin{array}{l} V_{I} = V_{IH} \mbox{ or } V_{IL} \\ I_{OH} = -100 \ \mu A \\ I_{OH} = -4 \ m A \\ I_{OH} = -8 \ m A \\ I_{OH} = -12 \ m A \\ I_{OH} = -12 \ m A \\ I_{OH} = -24 \ m A \\ I_{OH} = -24 \ m A \\ I_{OH} = -32 \ m A \\ I_{OH} = -32 \ m A \\ I_{OL} = 100 \ \mu A \\ I_{OL} = 4 \ m A \\ I_{OL} = 4 \ m A \\ I_{OL} = 8 \ m A \\ I_{OL} = 12 \ m A \\ I_{OL} = 16 \ m A \\ I_{OL} = 24 \ m A \end{array} $	1.65 to 5.5 1.65 2.3 2.7 3.0 3.0 4.5 1.65 to 5.5 1.65 2.3 2.7 3.0 3.0 3.0 4.5	V _{CC} - 0.1 1.29 1.8 2.2 2.4 2.2 3.7	- - - - - - 0.1 0.24 0.3 0.4 0.4 0.55	V _{CC} - 0.1 1.29 1.8 2.2 2.4 2.2 3.7	- - - - - 0.1 0.24 0.3 0.4 0.4 0.55	V
	3-State Output Leakage	I _{OL} = 32 mA	4.5 3.6	-	0.6 ±5.0	-	0.6 ±5.0	
I _{OZ}	Gurrent	$V_{I} = V_{IH} \text{ or } V_{IL},$ $V_{O} = 0 \text{ to } 5.5 \text{ V}$	3.0	_	±3.0	_	±3.0	μA
I	Input Leakage Current	$V_{I} = 0$ to 5.5 V	3.6	-	±5.0	-	±5.0	μA
I _{OFF}	Power Off Leakage Current	$V_{I} = 5.5 V \text{ or}$ $V_{O} = 5.5 V$	0	-	10	-	10	μA
I _{CC}	Quiescent Supply Current	$V_{I} = 5.5 \text{ V or GND}$	3.6	-	10	-	10	μA
ΔI_{CC}	Increase in I _{CC} per Input	$V_{IH} = V_{CC} - 0.6 V$	2.3 to 3.6	-	500	_	500	μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

AC ELECTRICAL CHARACTERISTICS

				T _A = -40 °C	C to +85 °C	T _A = -40 °C	to +125 °C	
Symbol	Parameter	Test Condition	V _{CC} (V)	Min	Max	Min	Max	Unit
t _{PLH} , t _{PHL}	Propagation Delay, Input to Output	See Figures 4 and 5	1.65 to 1.95	-	11.0	-	11.0	ns
			2.3 to 2.7	-	7.2	-	7.2	
			2.7	-	6.5	-	6.5	
			3.0 to 3.6	-	6.0	-	6.0	
			4.5 to 5.5	-	4.7	-	4.7	

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AC ELECTRICAL CHARACTERISTICS

				T _A = -40 °C	C to +85 °C	T _A = -40 °C	c to +125 °C	
Symbol	Parameter	Test Condition	V _{CC} (V)	Min	Max	Min	Max	Unit
t _{PZH} , t _{PZL}	Output Enable Time	See Figures 4 and 5	1.65 to 1.95	-	11.3	_	11.3	ns
			2.3 to 2.7	-	9.1	-	9.1	
			2.7	-	8.0	_	8.0	
			3.0 to 3.6	-	7.0	-	7.0	
			4.5 to 5.5	-	6.0	-	6.0	
t _{PHZ} , t _{PLZ}	Output Disable Time	See Figures 4 and 5	1.65 to 1.95	-	9.0	_	9.0	ns
			2.3 to 2.7	-	7.2	-	7.2	
			2.7	-	7.0	-	7.0	
			3.0 to 3.6	-	6.0	-	6.0	
			4.5 to 5.5	-	5.0	-	5.0	
t _{OSHL} , t _{OSLH}	Output to Output Skew		1.65 to 1.95	_	_	_	-	ns
			2.3 to 2.7	-	-	-	-	
			2.7	-	-	_	-	
			3.0 to 3.6	-	1.0	-	1.0	
			4.5 to 5.5	-	-	-	-	

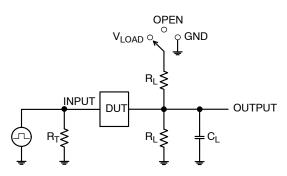
Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

DYNAMIC SWITCHING CHARACTERISTICS

		Vee		T _A = 25 °C	
Symbol	Parameter	V _{CC} (V)	Test Conditions	Тур	Unit
V _{OLP}	Quiet Output Dynamic Peak V _{OL}	3.3	C_L = 50 pF, V_{IH} = 3.3 V, V_{IL} = 0 V	0.8	V
		2.5	C_L = 30 pF, V_{IH} = 2.5 V, V_{IL} = 0 V	0.6	
V _{OLV}	Quiet Output Dynamic Peak V _{OL}	3.3	C_L = 50 pF, V_{IH} = 3.3 V, V_{IL} = 0 V	-0.8	V
		2.5	C_L = 30 pF, V_{IH} = 2.5 V, V_{IL} = 0 V	-0.6	

CAPACITANCE

Symbol	Parameter	Test Conditions	Тур	Unit
C _{IN}	Input Capacitance	V_{CC} = Open, V_I = 0 V or V_{CC}	7.0	pF
C _{OUT}	Output Capacitance	V_{CC} = 3.3 V, V_{I} = 0 V or V_{CC}	8.0	pF
C _{PD}	Power Dissipation Capacitance	V_{CC} = 3.3 V, V_{I} = 0 V or $V_{CC,}f$ = 10 MHz	25.0	pF



V....

Test	Switch Position
t _{PLH} / t _{PHL}	Open
t _{PLZ} / t _{PZL}	V _{LOAD}
t _{PHZ} / t _{PZH}	GND

 C_L includes probe and jig capacitance R_T is Z_{OUT} of pulse generator (typically 50 $\Omega)$ f = 1 MHz

10%

tрн

 t_{PLH}

t_r = 2.5 ns

INPUT

OUTPUT

OUTPUT

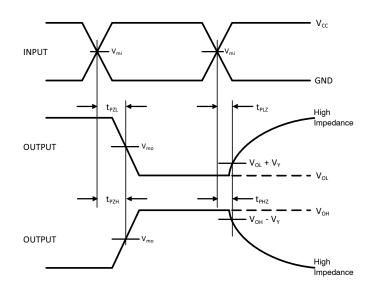


Figure	<u>م</u>	Test	Circuit
IIGUI		ICOL	Oncure

t_f = 2.5 ns

10%

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V_{ma}

t_{PLH}

 t_{PHL} Þ

Vcc

GND

V_{OH}

Vo

V_{OH}

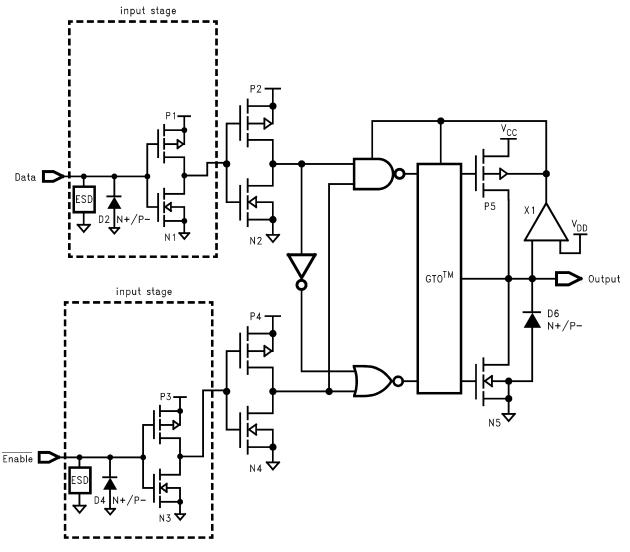
 V_{OL}

V _{CC} , V	R_{L}, Ω	C _L , pF	V _{LOAD}	V _m , V	V _Y , V
1.65 to 1.95	500	30	$2 \times V_{CC}$	V _{CC} /2	0.15
2.3 to 2.7	500	30	$2 \times V_{CC}$	V _{CC} /2	0.15
2.7	500	50	6 V	1.5	0.3
3.0 to 3.6	500	50	6 V	1.5	0.3
4.5 to 5.5	500	50	$2 \times V_{CC}$	V _{CC} /2	0.3

Figure 5. Switching Waveforms

74LCX125

SCHEMATIC DIAGRAM (GENERIC FOR LCX FAMILY)





ORDERING INFORMATION

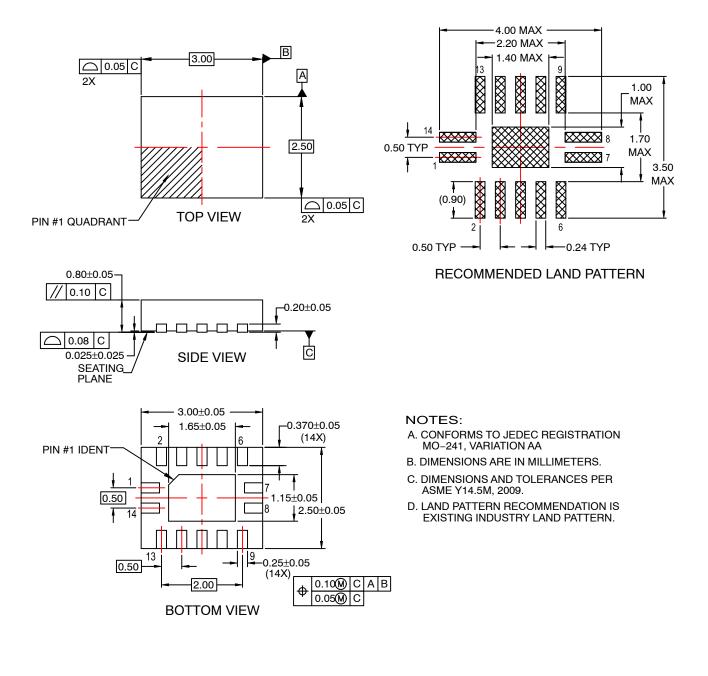
Product Number	Package	Shipping †	
74LCX125MTCX	TSSOP-14 WB (Pb-Free/Halide Free)	2500 / Tape and Reel	
74LCX125BQX (Note 5)	QFN-14 (Pb-Free/Halide Free)	3000 / Tape and Reel	
74LCX125MTC	TSSOP-14 WB (Pb-Free/Halide Free)	2350 Units / Tube	

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, <u>BRD8011/D</u>.
5. DQFN package available in Tape and Reel only.



QFN14 3.0x2.5, 0.5P CASE 510CB ISSUE O

DATE 31 AUG 2016



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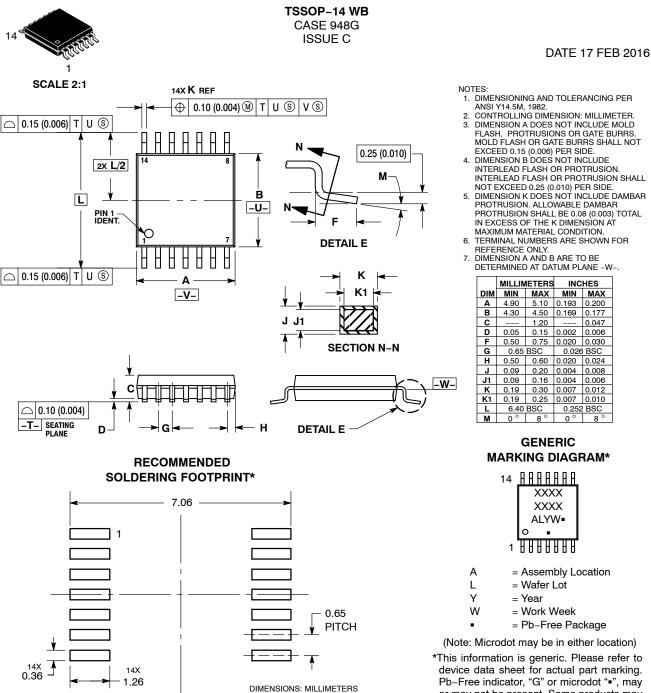
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SOIC14 CASE 751EF **ISSUE O** DATE 30 SEP 2016 8.75 Α 8.50 0.65 7.62 14 8 14 8 В ₽ ╞ 4.00 6.00 5.60 3.80 Ħ = ╞ = Ħ 1.70 7 **PIN #1** 7 1.27 1 0.51 IDENT. 1.270.35 (0.33) - \oplus 0.25 (M) С В Α LAND PATTERN RECOMMENDATION TOP VIEW 1.75 MAX 0.25 0.19 0.10 С 1.50 0.25 1.25 0.10 SIDE VIEW FRONT VIEW NOTES: A. CONFORMS TO JEDEC MS-012, VARIATION AB, ISSUE C **B. ALL DIMENSIONS ARE IN MILLIMETERS** 0.50 0.25 × 45° C. DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS R0.10 GAGE D. LAND PATTERN STANDARD: PLANE SOIC127P600X145-14M E. CONFORMS TO ASME Y14.5M, 2009 R0.10 0.36 8° 0° 0.90 0.50 SEATING PLANE (1.04)**DETAIL A** SCALE 16:1

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*For additional information on our Pb-Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

- FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT
- INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL

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