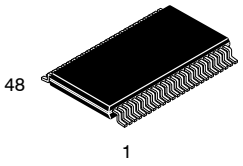
Low-Voltage 16-Bit Bidirectional Transceiver with 5 V Tolerant Inputs and Outputs

74LCX16245



TSSOP48 12.5x6.1
CASE 948BQ

General Description

The LCX16245 contains sixteen non-inverting bidirectional buffers with 3-STATE outputs and is intended for bus oriented applications. The device is designed for low voltage (2.5 V or 3.3 V) V_{CC} applications with capability of interfacing to a 5 V signal environment. The device is byte controlled. Each byte has separate control inputs which could be shorted together for full 16-bit operation. The $\overline{T/R}$ inputs determine the direction of data flow through the device. The $\overline{OE}$ inputs disable both the A and B ports by placing them in a high impedance state.

The LCX16245 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

Features

- 5 V Tolerant Inputs and Outputs
- 1.65 V – 5.5 V V_{CC} Specifications Provided
- 4.5 ns t_{PD} max (V_{CC} = 3.3 V), 20 μA I_{CC} max
- Power-off High Impedance Inputs and Outputs
- Supports Live Insertion and Withdrawal*
- ±24 mA Output Drive (V_{CC} = 3.0 V)
- Uses Patented Noise/EMI Reduction Circuitry
- Latch-up Performance Exceeds 100 mA
- ESD Performance:
  - Human Body Model >2000 V
- These Devices are Pb-Free, Halide Free and are RoHS Compliant

*To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pull-up resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

MARKING DIAGRAM

XXXXXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 7 of this data sheet.

LOGIC SYMBOL

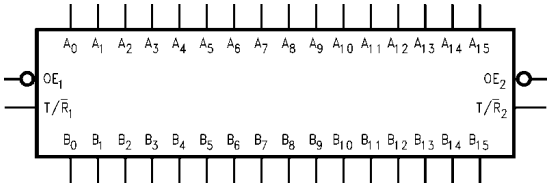


Figure 1. Logic Symbol

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CONNECTION DIAGRAM

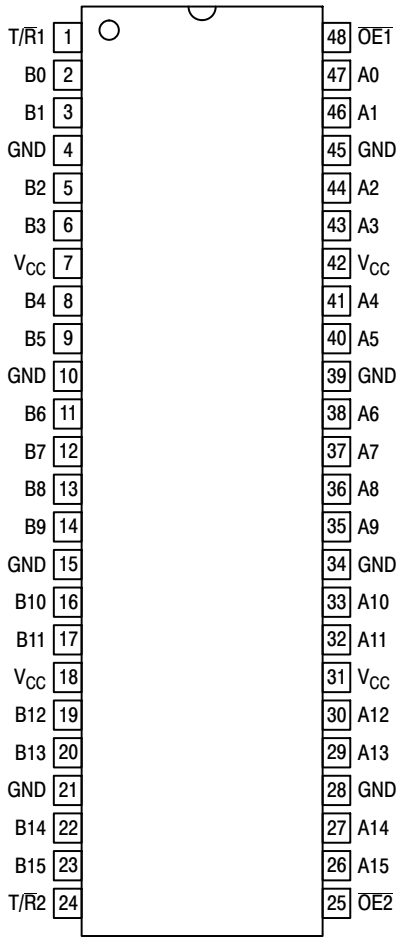


Figure 2. Pin Assignment

Table 1. PIN DESCRIPTIONS

Pin Names	Descriptions
$\overline{OE}_n$	Output Enable Inputs
$T/\overline{R}_n$	Transmit/Receive Inputs
A_0–A_{15}	Side A Inputs or 3-State Outputs
B_0–B_{15}	Side B Inputs or 3-State Outputs
NC	No Connect

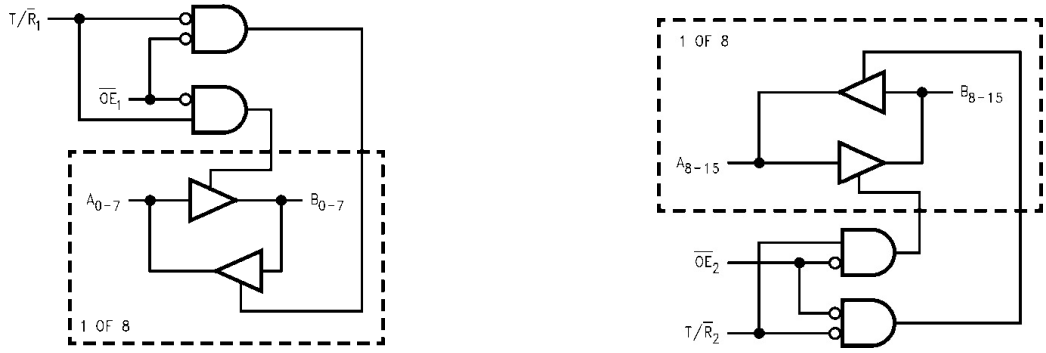
Table 2. TRUTH TABLES

Inputs		Outputs
$\overline{OE}_1$	$T/\overline{R}_1$	
L	L	Bus B_0–B_7 Data to Bus A_0–A_7
L	H	Bus A_0–A_7 Data to Bus B_0–B_7
H	X	HIGH Z State on A_0–A_7, B_0–B_7

Inputs		Outputs
$\overline{OE}_2$	$T/\overline{R}_2$	
L	L	Bus B_8–B_{15} Data to Bus A_8–A_{15}
L	H	Bus A_8–A_{15} Data to Bus B_8–B_{15}
H	X	HIGH Z State on A_8–$A1_5$, B_8–B_{15}

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

LOGIC DIAGRAMS



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Figure 3. Logic Diagram

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MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_{CC}	DC Supply Voltage		–0.5 to +6.5	V
V_{IN}	DC Input Voltage (Note 1)		–0.5 to +6.5	V
V_{OUT}	DC Output Voltage (Note 1)	Active-Mode (High or Low State) Tri-State Mode Power-Down Mode (V_{CC} = 0 V)	–0.5 to V_{CC} + 0.5 –0.5 to +6.5 –0.5 to +6.5	V
I_{IK}	DC Input Diode Current	V_{IN} < GND	–50	mA
I_{OK}	DC Output Diode Current	V_{OUT} < GND	–50	mA
I_O	DC Output Source/Sink Current		±50	mA
I_{CC}	DC Supply Current per Supply Pin		±100	mA
I_{GND}	DC Supply Current per Ground Pin		±100	mA
T_{STG}	Storage Temperature Range		–65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 secs		260	°C
T_J	Junction Temperature Under Bias		+150	°C
θ_{JA}	Thermal Resistance (Note 2)		71	°C/W
P_D	Power Dissipation in Still Air		1765	mW
MSL	Moisture Sensitivity		Level 1	–
F_R	Flammability Rating	Oxygen Index: 28 to 34	UL 94 V-0 @ 0.125 in	–
V_{ESD}	ESD Withstand Voltage (Note 3)	Human Body Model Charged Device Model	>2000 N/A	V

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. I_O absolute maximum rating must be observed.
2. Measured with minimum pad spacing on an FR4 board, using 76 mm-by-114 mm, 2-ounce copper trace no air flow per JESD51-7.
3. HBM tested to EIA / JESD22-A114-A. CDM tested to JESD22-C101-A. JEDEC recommends that ESD qualification to EIA/JESD22-A115A (Machine Model) be discontinued.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Typ	Max	Unit
V_{CC}	Supply Voltage	Operating Data Retention Only	1.65 1.5	2.5, 3.3 2.5, 3.3	5.5 5.5	V
V_{IN}	Digital Input Voltage		0	–	5.5	V
V_{OUT}	Output Voltage	Active Mode (High or Low State) Tri-State Mode Power Down Mode (V_{CC} = 0 V)	0 0 0	– – –	V_{CC} 5.5 5.5	V
T_A	Operating Free-Air Temperature		–40	–	+125	°C
t_r, t_f	Input Rise or Fall Rate	V_{CC} = 1.65 V to 1.95 V V_{CC} = 2.3 V to 2.7 V V_{IN} from 0.8 V to 2.0 V, V_{CC} = 3.0 V V_{CC} = 4.5 V to 5.5 V	0 0 0 0	– – – –	20 20 10 5	ns/V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

4. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

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DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	V_{CC} (V)	T_A = −40 °C to +85 °C		T_A = −55 °C to +125 °C		Unit
				Min	Max	Min	Max	
V_{IH}	High-Level Input Voltage		1.65 to 1.95	0.65 x V_{CC}	–	0.65 x V_{CC}	–	V
			2.3 to 2.7	1.7	–	1.7	–	
			2.7 to 3.6	2.0	–	2.0	–	
			4.5 to 5.5	0.7 x V_{CC}	–	0.7 x V_{CC}	–	
V_{IL}	Low-Level Input Voltage		1.65 to 1.95	–	0.35 x V_{CC}	–	0.35 x V_{CC}	V
			2.3 to 2.7	–	0.7	–	0.7	
			2.7 to 3.6	–	0.8	–	0.8	
			4.5 to 5.5	–	0.3 x V_{CC}	–	0.3 x V_{CC}	
V_{OH}	High-Level Output Voltage	V_I = V_{IH} or V_{IL}						V
		I_{OH} = −100 μA	1.65 to 5.5	V_{CC} − 0.1	–	V_{CC} − 0.1	–	
		I_{OH} = −4 mA	1.65	1.2	–	1.2	–	
		I_{OH} = −8 mA	2.3	1.8	–	1.8	–	
		I_{OH} = −12 mA	2.7	2.2	–	2.2	–	
		I_{OH} = −16 mA	3.0	2.4	–	2.4	–	
		I_{OH} = −24 mA	3.0	2.2	–	2.2	–	
		I_{OH} = −32 mA	4.5	3.8	–	3.8	–	
V_{OL}	Low-Level Output Voltage	V_I = V_{IH} or V_{IL}						V
		I_{OH} = −100 μA	1.65 to 5.5	–	0.1	–	0.1	
		I_{OH} = −4 mA	1.65	–	0.45	–	0.45	
		I_{OH} = −8 mA	2.3	–	0.6	–	0.6	
		I_{OH} = −12 mA	2.7	–	0.4	–	0.4	
		I_{OH} = −16 mA	3.0	–	0.4	–	0.4	
		I_{OH} = −24 mA	3.0	–	0.55	–	0.55	
		I_{OH} = −32 mA	4.5	–	0.6	–	0.6	
I_I	Input Leakage Current	V_I = 0 to 5.5 V	2.3 to 3.6	–	±5.0	–	±5.0	μA
I_{OZ}	3-State Output Leakage Current	V_I = V_{IH} or V_{IL}, V_O = 0 V to 5.5 V	2.3 to 3.6	–	±5.0	–	±5.0	μA
I_{OFF}	Power Off Leakage Current	V_I = 5.5 V or V_O = 5.5 V	0	–	10	–	10	μA
I_{CC}	Quiescent Supply Current	V_I = 5.5 V or GND	2.3 to 3.6	–	10	–	10	μA
ΔI_{CC}	Increase in I_{CC} per Input	V_{IH} = V_{CC} − 0.6 V	2.3 to 3.6	–	500	–	500	μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

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AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Condition	V_{CC} (V)	T_A = −40 °C to +85 °C		T_A = −55 °C to +125 °C		Unit
				Min	Max	Min	Max	
t_{PLH}, t_{PHL}	Propagation Delay, D to O	See Figures 4 and 5	1.65 to 1.95	–	8.5	–	8.5	ns
			2.3 to 2.7	–	5.4	–	5.4	
			2.7	–	5.2	–	5.2	
			3.0 to 3.6	–	4.5	–	4.5	
			4.5 to 5.5	–	4.0	–	4.0	
t_{PZH}, t_{PZL}	Output Enable Time, $\overline{OE}$ to O	See Figures 4 and 5	1.65 to 1.95	–	10.5	–	10.5	ns
			2.3 to 2.7	–	8.5	–	8.5	
			2.7	–	7.2	–	7.2	
			3.0 to 3.6	–	6.5	–	6.5	
			4.5 to 5.5	–	5.5	–	5.5	
t_{PHZ}, t_{PLZ}	Output Disable Time, $\overline{OE}$ to O	See Figures 4 and 5	1.65 to 1.95	–	9.7	–	9.7	ns
			2.3 to 2.7	–	7.7	–	7.7	
			2.7	–	6.9	–	6.9	
			3.0 to 3.6	–	6.4	–	6.4	
			4.5 to 5.5	–	5.4	–	5.4	
t_{OSHL}, t_{OSLH}	Output to Output Skew, (Note 5)		1.65 to 1.95	–	–	–	–	ns
			2.3 to 2.7	–	–	–	–	
			2.7	–	–	–	–	
			3.0 to 3.6	–	1.0	–	1.0	
t_{OSHL}, t_{OSLH}	Output to Output Skew, (Note 5)		4.5 to 5.5	–	–	–	–	ns

5. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the dynamic operating current consumption without load. Average operating current can be obtained by the equation $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}$. C_{PD} is used to determine the no-load dynamic power consumption: $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.

DYNAMIC SWITCHING CHARACTERISTICS

Symbol	Characteristic	Condition	V_{CC} (V)	T_A = +25 °C	Units
				Typical	
V_{OLP}	Quiet Output Dynamic Peak V_{OL}	C_L = 50 pF, V_{IH} = 3.3 V, V_{IL} = 0 V C_L = 30 pF, V_{IH} = 2.5 V, V_{IL} = 0 V	3.3 2.5	0.8 0.6	V V
V_{OLV}	Quiet Output Dynamic Valley V_{OL}	C_L = 50 pF, V_{IH} = 3.3 V, V_{IL} = 0 V C_L = 30 pF, V_{IH} = 2.5 V, V_{IL} = 0 V	3.3 2.5	−0.8 −0.6	V V

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Condition	Typical	Units
C_{IN}	Input Capacitance	V_{CC} = Open, V_I = 0 V or V_{CC}	7	pF
$C_{I/O}$	Input/Output Capacitance	V_{CC} = 3.3 V, V_I = 0 V or V_{CC}	8	pF
C_{PD}	Power Dissipation Capacitance	V_{CC} = 3.3 V, V_I = 0 V or V_{CC}, f = 10 MHz	20	pF

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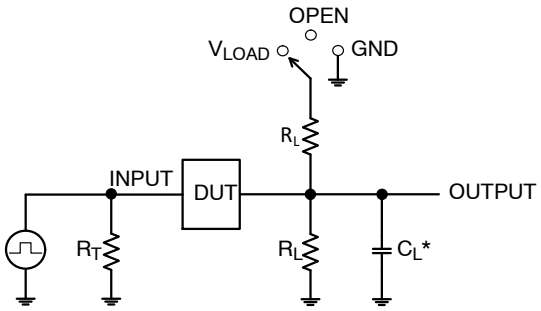
AC LOADING AND WAVEFORMS

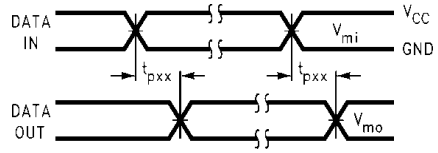


$C_{L\ =}$ includes probe and jig capacitance
$R_T = Z_{OUT}$ of pulse generator (typically 50 Ω)
f = 1 MHz

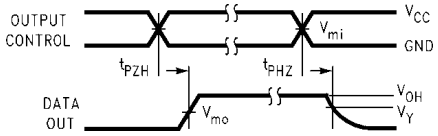
Figure 4. Test Circuit

Table 3. TEST CIRCUIT TABLE

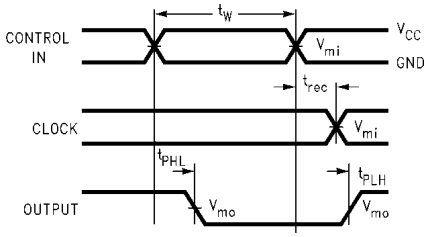
Test	Switch
t_{PLH}, t_{PHL}	Open
t_{PLZ}, t_{PZL}	V_{LOAD}
t_{PHZ}, t_{PZH}	GND



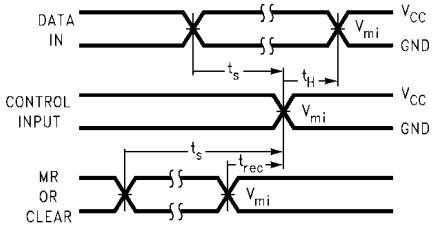
WAVEFORM FOR INVERTING AND NON-INVERTING FUNCTIONS



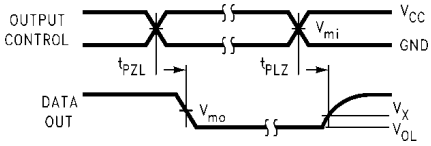
3–STATE OUTPUT HIGH ENABLE AND DISABLE TIMES FOR LOGIC



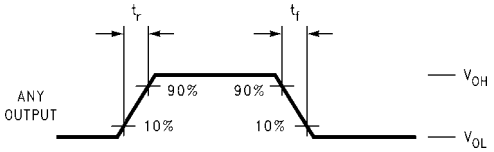
PROPAGATION DELAY. PULSE WIDTH AND T_{rec} WAVEFORMS



SETUP TIME, HOLD TIME AND RECOVERY TIME FOR LOGIC



3–STATE OUTPUT LOW ENABLE AND DISABLE TIMES FOR LOGIC



T_{rise} AND T_{fall}

Figure 5. Waveforms
(Input Characteristics; f =1 MHz, $t_r = t_f$ = 3 ns)

Table 4. SWITCHING WAVEFORMS TABLE

V_{CC}, V	R_L, Ω	C_L, pF	V_{LOAD}	V_{mi}, V	V_{mo}, V	V_Y, V
1.65 to 1.95	500	30	2 x V_{CC}	V_{CC}/2	V_{CC}/2	0.15
2.3 to 2.7	500	30	2 x V_{CC}	V_{CC}/2	V_{CC}/2	0.15
2.7	500	50	6 V	1.5	1.5	0.3
3.0 to 3.6	500	50	6 V	1.5	1.5	0.3
4.5 to 4.5	500	50	2 x V_{CC}	V_{CC}/2	V_{CC}/2	0.3

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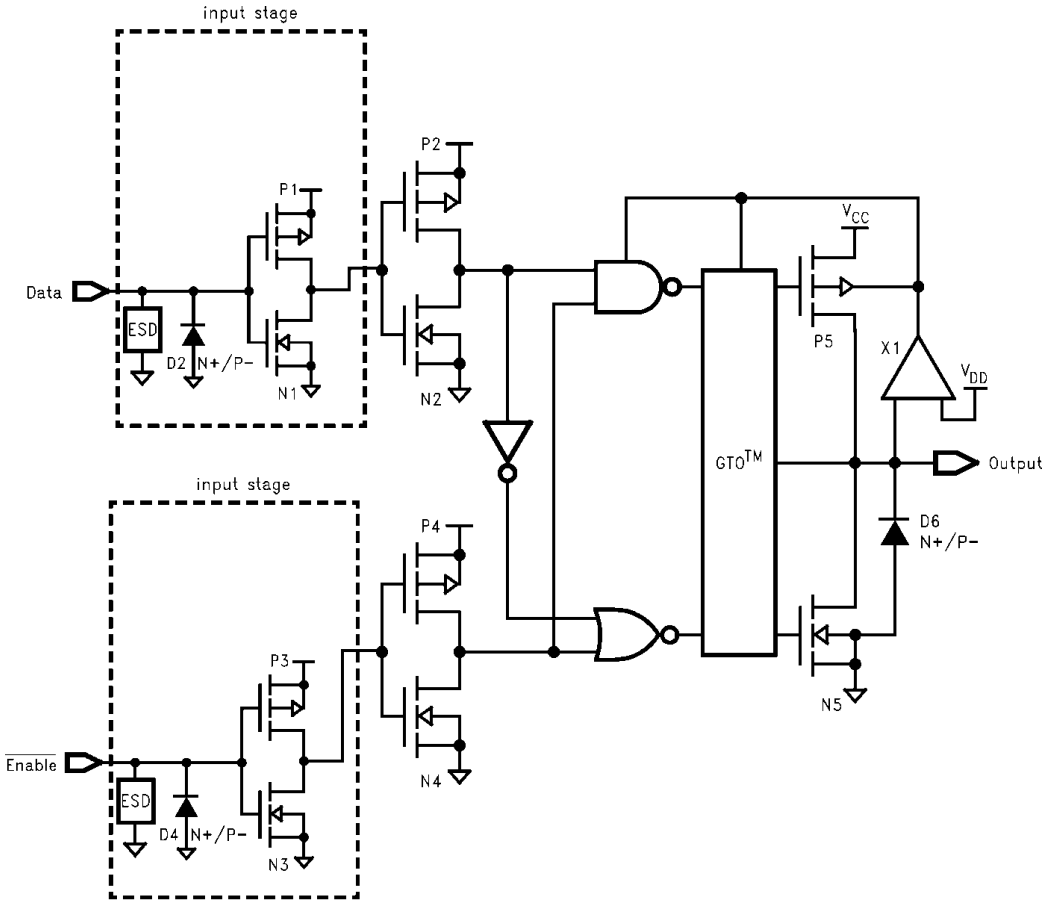

Figure 6. Schematic Diagram (Generic for LCX Family)

ORDERING INFORMATION

Device	Marking	Package	Shipping†
74LCX16245MTDX	LCX16245G	TSSOP-48	2500 Units / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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REVISION HISTORY

Revision	Description of Changes	Date
1	Converted the Data Sheet to **onsem**i format with the updates in Ordering Information Table, Recommended Operating Table, Maximum Rating Table.	9/16/2025

This document has undergone updates prior to the inclusion of this revision history table. The changes tracked here only reflect updates made on the noted approval dates.

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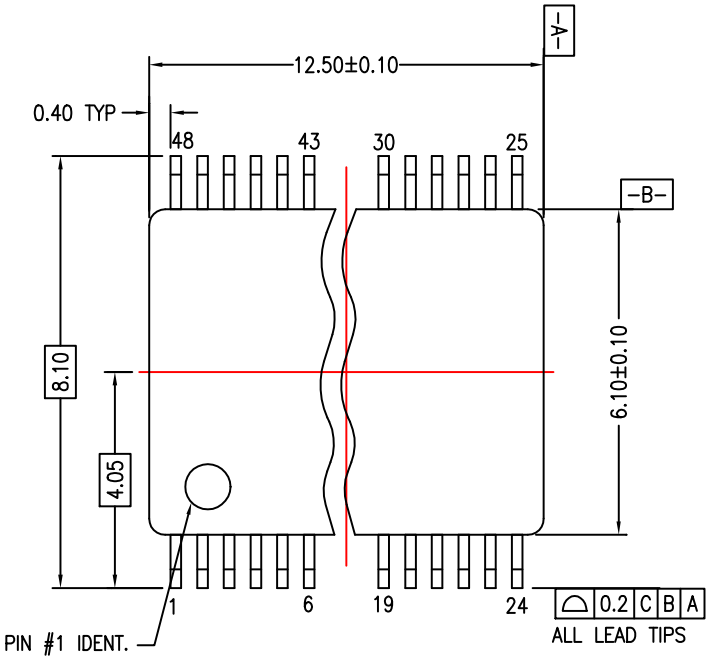
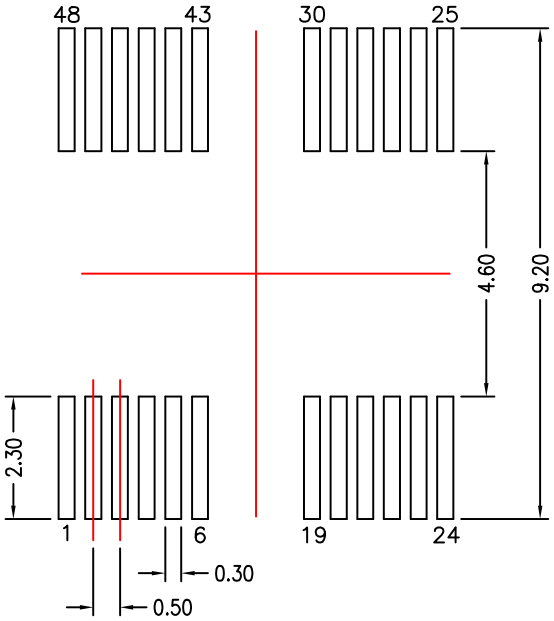
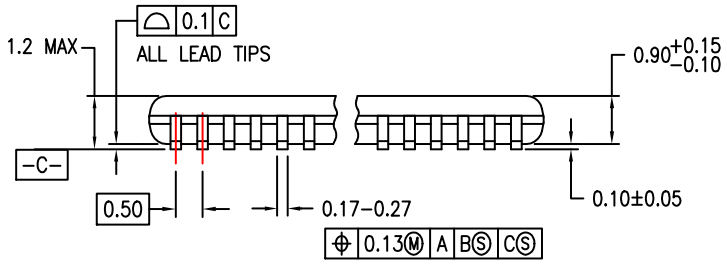
TSSOP48 12.5x6.1
CASE 948BQ
ISSUE O

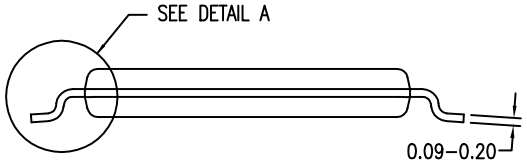
DATE 30 SEP 2016

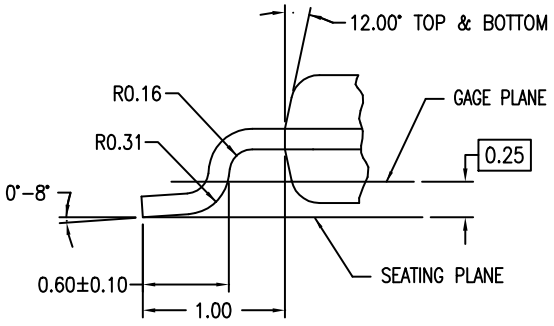




LAND PATTERN RECOMMENDATION







DETAIL A

DIMENSIONS ARE IN MILLIMETERS

NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO−153, VARIATION ED, DATE 4/97.
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

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DESCRIPTION:	**TSSOP48 12.5X6.1**		**PAGE 1 OF 1**

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