Low-Voltage Bidirectional Transceiver with 5 V Tolerant Inputs and Outputs

74LCX245

The LCX245 contains eight non−inverting bidirectional buffers with 3−STATE outputs and is intended for bus oriented applications. The device is designed for low voltage (2.5 V and 3.3 V) V_{CC} applications with capability of interfacing to a 5 V signal environment. The T/$\overline{R}$ input determines the direction of data flow through the device. The $\overline{OE}$ input disables both the A and B ports by placing them in a high impedance state.

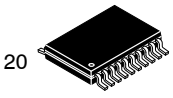
The LCX245 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

Features

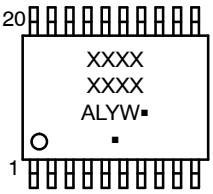
- 5 V Tolerant Inputs and Outputs
- 1.65 V to 5.5 V V_{CC} Specifications Provided
- 7.0 ns t_{PD} Max. (V_{CC} = 3.3 V), 10 mA I_{CC} Max
- Power Down High Impedance Inputs and Outputs
- Supports Live Insertion/Withdrawal (Note 1)
- ±24 mA Output Drive (V_{CC} = 3.0 V)
- Implements Proprietary Noise/EMI Reduction Circuitry
- Latch−up Performance Exceeds 100 mA
- ESD Performance:
  - Human Body Model > 2000 V
- Leadless DQFN Package
- This is a Pb−Free Device

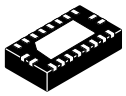
NOTE:

1. To ensure the high−impedance state during power up or down, $\overline{OE}$ should be tied to V_{CC} through a pull−up resistor: the minimum value or the resistor is determined by the current−sourcing capability of the driver.

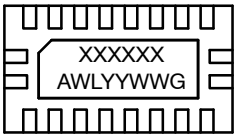


TSSOP−20
DT SUFFIX
CASE 948AQ





WQFN20, 4.5x2.5, 0.5P
MN SUFFIX
CASE 510CD



MARKING DIAGRAMS

XXXXXXXX	= Specific Device Code
A	= Assembly Location
L, WL	= Wafer Lot
Y, YY	= Year
W, WW	= Work Week
G or ▪	= Pb−Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 7 of this data sheet.

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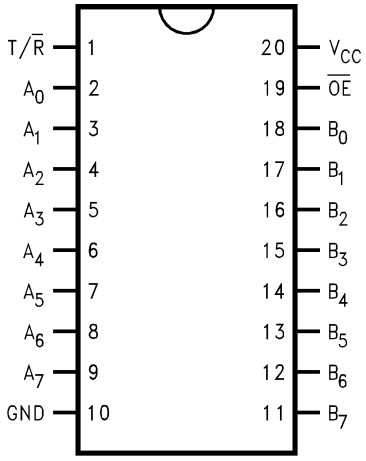

Figure 1. Connection Diagram
(Pin Assignment for SOIC, SOP, SSOP, and TSSSOP)

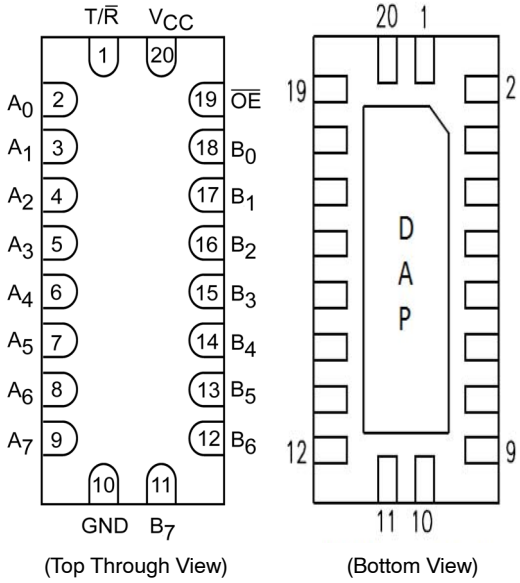

Figure 2. Connection Diagram
(Pin Assignment for DQFN)

PIN DESCRIPTION

Pin Names	Description
$\overline{OE}$	Output Enable Input
T/$\overline{R}$	Transmit/Receive Input
A_0–A_7	Side A Inputs or 3–STATE Outputs
B_0–B_7	Side B Inputs or 3–STATE Outputs
DAP	No Connect

NOTE: DAP (Die Attach Pad)

TRUTH TABLE

INPUTS		Outputs
$\overline{OE}$	T/$\overline{R}$	
L	L	Bus B_0 – B_7 Data to Bus A_0 – A_7
L	H	Bus A_0 – A_7 Data to Bus B_0 – B_7
H	X	HIGH Z State on A_0 – A_7, B_0 – B_7 (Note 2)

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

NOTE:
2. Unused bus terminals during HIGH Z State must be held HIGH or LOW.

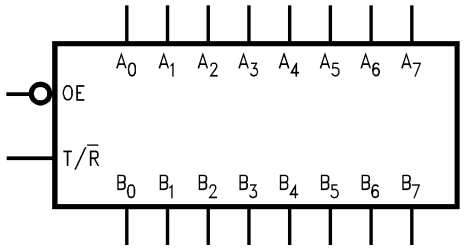

Figure 3. Logic Symbol

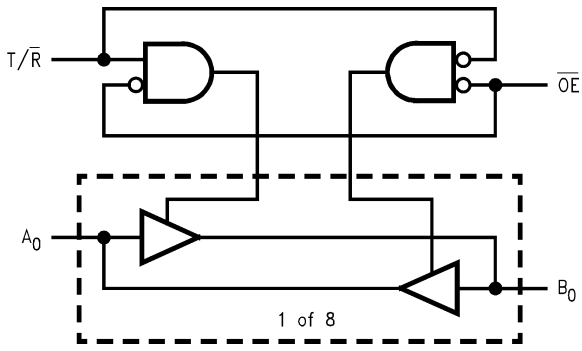

Figure 4. Logic Diagram

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ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Condition	Value	Unit
V_{CC}	DC Supply Voltage		−0.5 to +6.5	V
V_I	DC Input Voltage (Note 1)		−0.5 to +6.5	V
V_O	DC Output Voltage (Note 1)	Active−Mode (High or Low State)	−0.5 to V_{CC} + 0.5	V
		Tri−State Mode	−0.5 to +6.5	
		Power−Down Mode (V_{CC} = 0 V)	−0.5 to +6.5	
I_{IK}	DC Input Diode Current	V_{IN} < GND	−50	mA
I_{OK}	DC Output Diode Current	V_{OUT} < GND	−50	mA
I_O	DC Output Source/Sink Current		±50	mA
I_{CC} or I_{GND}	DC Supply Current per Supply Pin or Ground Pin		±100	mA
T_{STG}	Storage Temperature Range		−65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 secs		260	°C
T_J	Junction Temperature under Bias		+150	°C
θ_{JA}	Thermal Resistance (Note 2)	WQFN20	99	°C/W
		TSSOP−20	150	
P_D	Power Dissipation in Still Air	WQFN20	1256	mW
		TSSOP−20	833	
MSL	Moisture Sensitivity		Level 1	−
F_R	Flammability Rating	Oxygen Index: 28 to 34	UL 94 V−0 @ 0.125 in	−
V_{ESD}	ESD Withstand Voltage (Note 3)	Human Body Model	2000	V
		Charged Device Model	N/A	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. I_O absolute maximum rating must be observed.
2. Measured with minimum pad spacing on an FR4 board, using 76 mm−by−114 mm, 2−ounce copper trace no air flow per JESD51−7.
3. HBM tested to EIA / JESD22−A114−A. CDM tested to JESD22−C101−A.

RECOMMENDED OPERATING CONDITIONS (Note 4)

Symbol	Parameter		Min	Max	Unit
V_{CC}	Supply Voltage	Operating	1.65	5.5	V
		Data Retention Only	1.5	5.5	
V_I	Digital Input Voltage		0	5.5	V
V_O	Output Voltage	Active−Mode (High or Low State)	0	V_{CC}	V
		Tri−State Mode	0	5.5	
		Power−Down Mode (V_{CC} = 0 V)	0	5.5	
T_A	Operating Free−Air Temperature		−40	+125	°C
t_r, t_f	Input Rise or Fall Rate	V_{CC} = 1.65 V to 1.95 V	0	20	ns/V
		V_{CC} = 2.3 V to 2.7 V	0	20	
		V_{IN} from 0.8 V to 2.0 V, V_{CC} = 3.0 V	0	10	
		V_{CC} = 4.5 V to 5.5 V	0	5	

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

4. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

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DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	V_{CC} (V)	T_A = −40°C to +85°C		T_A = −40°C to +125°C		Unit
				Min	Max	Min	Max	
V_{IH}	High−Level Input Voltage		1.65 to 1.95	$0.65 \times V_{CC}$		$0.65 \times V_{CC}$		V
			2.3 to 2.7	1.7		1.7		
			2.7 to 3.6	2.0		2.0		
			4.5 to 5.5	$0.7 \times V_{CC}$		$0.7 \times V_{CC}$		
V_{IL}	Low−Level Input Voltage		1.65 to 1.95		$0.35 \times V_{CC}$		$0.35 \times V_{CC}$	V
			2.3 to 2.7		0.7		0.7	
			2.7 to 3.6		0.8		0.8	
			4.5 to 5.5		$0.3 \times V_{CC}$		$0.3 \times V_{CC}$	
V_{OH}	High−Level Output Voltage	$V_I = V_{IH}$ or V_{IL}						V
		I_{OH} = −100 μA	1.65 to 5.5	$V_{CC} - 0.1$	–	$V_{CC} - 0.1$	–	
		I_{OH} = −4 mA	1.65	1.2	–	1.2	–	
		I_{OH} = −8 mA	2.3	1.8	–	1.8	–	
		I_{OH} = −12 mA	2.7	2.2	–	2.2	–	
		I_{OH} = −16 mA	3.0	2.4	–	2.4	–	
		I_{OH} = −24 mA	3.0	2.2	–	2.2	–	
		I_{OH} = −32 mA	4.5	3.8	–	3.8	–	
V_{OL}	Low−Level Output Voltage	$V_I = V_{IH}$ or V_{IL}						V
		I_{OL} = 100 μA	1.65 to 5.5	–	0.1	–	0.1	
		I_{OL} = 4 mA	1.65	–	0.45	–	0.45	
		I_{OL} = 8 mA	2.3	–	0.6	–	0.6	
		I_{OL} = 12 mA	2.7	–	0.4	–	0.4	
		I_{OL} = 16 mA	3.0	–	0.4	–	0.4	
		I_{OL} = 24 mA	3.0	–	0.55	–	0.55	
		I_{OL} = 32 mA	4.5	–	0.6	–	0.6	
I_I	Input Leakage Current	V_I = 0 to 5.5 V	1.65 to 5.5	–	±5.0	–	±5.0	μA
I_{OZ}	3−State Output Leakage Current	$V_I = V_{IH}$ or V_{IL}, V_O = 0 V to 5.5 V	1.65 to 5.5	–	±5.0	–	±5.0	μA
I_{OFF}	Power Off Leakage Current	V_I = 5.5 V or V_O = 5.5 V	0	–	10	–	10	μA
I_{CC}	Quiescent Supply Current	V_I = 5.5 V or GND	1.65 to 5.5	–	10	–	10	μA
ΔI_{CC}	Increase in I_{CC} per Input	$V_{IH} = V_{CC} - 0.6$ V	2.3 to 3.6	–	500	–	500	μA

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AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} (V)	T_A = −40°C to +85°C		T_A = −40°C to +125°C		Unit
				Min	Max	Min	Max	
t_{PLH}, t_{PHL}	Propagation Delay, D to O	See Figures 5 and 6	1.65 to 1.95	–	10.3	–	10.3	ns
			2.3 to 2.7	–	8.4	–	8.4	
			2.7	–	8.0	–	8.0	
			3.0 to 3.6	–	7.0	–	7.0	
			4.5 to 5.5	–	5.0	–	5.0	
t_{PZH}, t_{PZL}	Output Enable Time, $\overline{OE}$ to O	See Figures 5 and 6	1.65 to 1.95	–	13.0	–	13.0	ns
			2.3 to 2.7	–	10.5	–	10.5	
			2.7	–	9.5	–	9.5	
			3.0 to 3.6	–	8.5	–	8.5	
			4.5 to 5.5	–	7.0	–	7.0	
t_{PHZ}, t_{PLZ}	Output Disable Time, $\overline{OE}$ to O	See Figures 5 and 6	1.65 to 1.95	–	11.0	–	11.0	ns
			2.3 to 2.7	–	9.0	–	9.0	
			2.7	–	8.5	–	8.5	
			3.0 to 3.6	–	7.5	–	7.5	
			4.5 to 5.5	–	6.0	–	6.0	
t_{OSHL}, t_{OSLH}	Output to Output Skew (Note 5)		1.65 to 1.95	–	–	–	–	ns
			2.3 to 2.7	–	–	–	–	
			2.7	–	–	–	–	
			3.0 to 3.6	–	1.0	–	1.0	
			5.0	–	–	–	–	

5. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH−to−LOW (t_{OSHL}) or LOW−to−HIGH (t_{OSLH}); parameter guaranteed by design.

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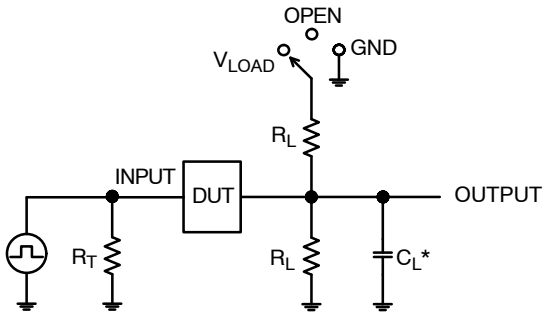
DYNAMIC SWITCHING CHARACTERISTICS

Symbol	Parameter	V_{CC} (V)	Condition	T_A = 25°C Typ	Unit
V_{OLP}	Quiet Output Dynamic Peak V_{OL}	3.3	C_L = 50 pF, V_{IH} = 3.3 V, V_{IL} = 0 V	0.8	V
		2.5	C_L = 30 pF, V_{IH} = 2.5 V, V_{IL} = 0 V	0.6	
V_{OLV}	Quiet Output Dynamic Peak V_{OL}	3.3	C_L = 50 pF, V_{IH} = 3.3 V, V_{IL} = 0 V	−0.8	V
		2.5	C_L = 30 pF, V_{IH} = 2.5 V, V_{IL} = 0 V	−0.6	

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Condition	Typical	Unit
C_{IN}	Input Capacitance	V_{CC} = Open, V_I = 0 V or V_{CC}	7.0	pF
C_{OUT}	Output Capacitance	V_{CC} = 3.3 V, V_I = 0 V or V_{CC}	8.0	pF
C_{PD}	Power Dissipation Capacitance	V_{CC} = 3.3 V, V_I = 0 V or V_{CC}, f = 10 MHz	25.0	pF



C_L includes probe and jig capacitance
R_T is Z_{OUT} of pulse generator (typically 50 Ω)
f = 1 MHz

Test	Switch Position
t_{PLH} / t_{PHL}	Open
t_{PLZ} / t_{PZL}	V_{LOAD}
t_{PHZ} / t_{PZH}	GND

Figure 5. Test Circuit

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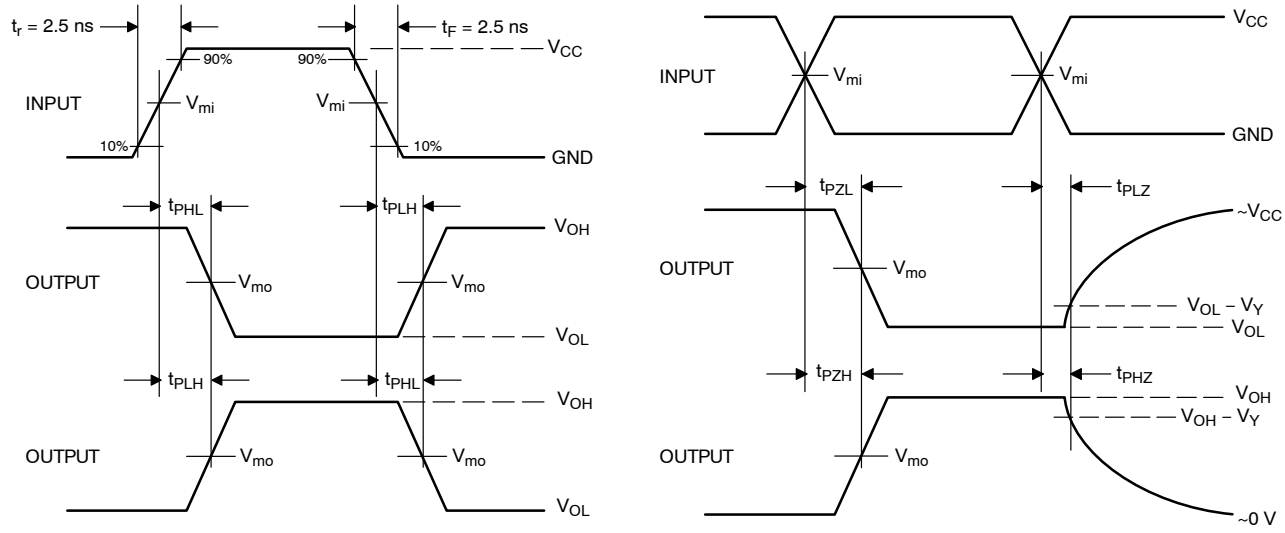

V_{CC}, V	R_L, Ω	C_L, pF	V_{LOAD}	V_{mi}, V	V_{mo}, V	V_Y, V
1.65 to 1.95	500	30	2 x V_{CC}	V_{CC}/2	V_{CC}/2	0.15
2.3 to 2.7	500	30	2 x V_{CC}	V_{CC}/2	V_{CC}/2	0.15
2.7	500	50	6 V	1.5	V_{CC}/2	0.3
3.0 to 3.6	500	50	6 V	1.5	V_{CC}/2	0.3
4.5 to 4.5	500	50	2 x V_{CC}	V_{CC}/2	V_{CC}/2	0.3

Figure 6. Switching Waveforms

ORDERING INFORMATION

Device	Marking	Package	Shipping†
74LCX245MTC	LCX 245	TSSOP−20	75 Units / Rail
74LCX245MTCX	LCX 245	TSSOP−20	2500 / Tape & Reel
74LCX245BQX	LCX245	WQFN20, 2.5x4.5	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*−Q Suffix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable.

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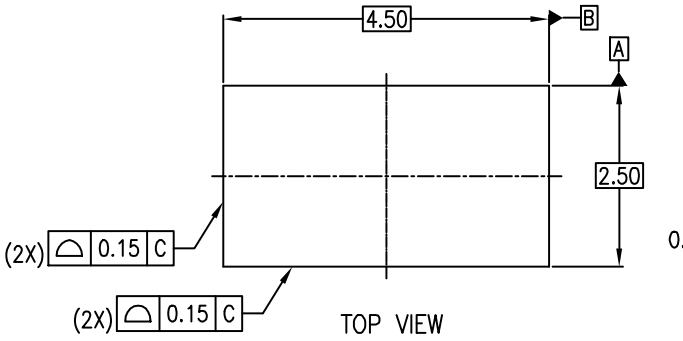
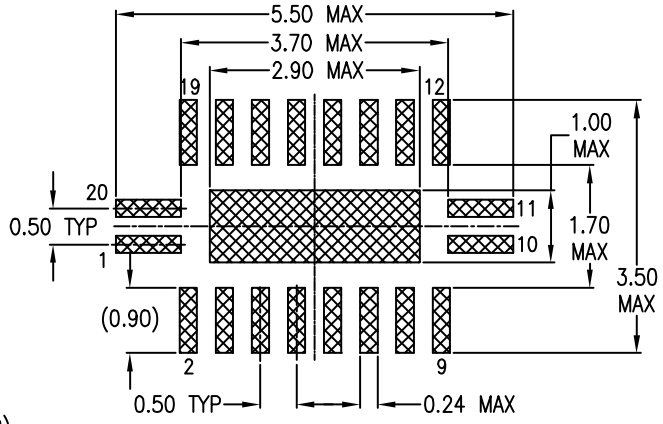
WQFN20 4.5x2.5, 0.5P
CASE 510CD
ISSUE O

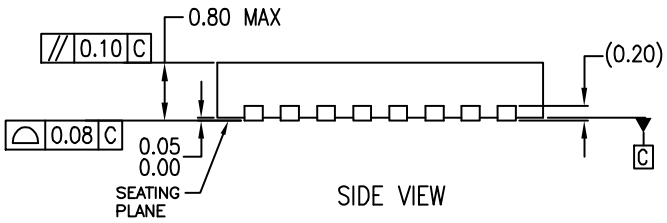
DATE 31 AUG 2016



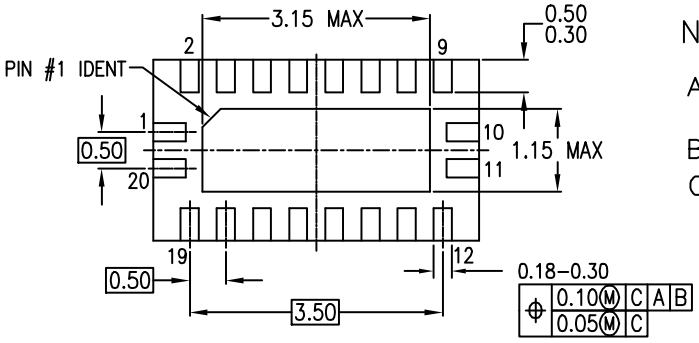
TOP VIEW



RECOMMENDED LAND PATTERN



SIDE VIEW



BOTTOM VIEW

NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO−241, VARIATION AC
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994

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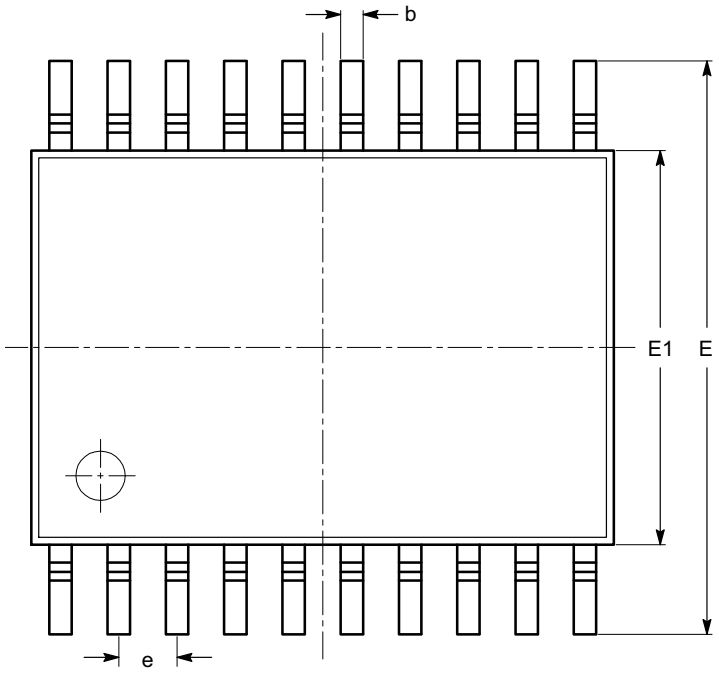
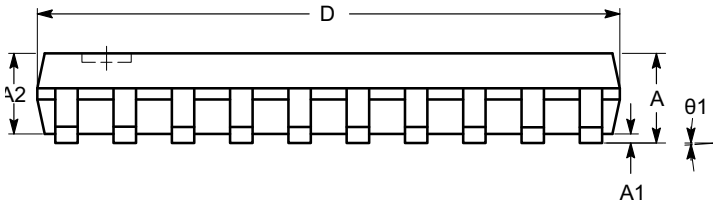
TSSOP20, 4.4x6.5
CASE 948AQ
ISSUE A

DATE 19 MAR 2009

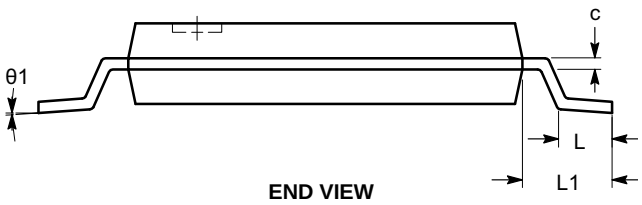


TOP VIEW

SYMBOL	MIN	NOM	MAX
A			1.20
A1	0.05		0.15
A2	0.80		1.05
b	0.19		0.30
c	0.09		0.20
D	6.40	6.50	6.60
E	6.30	6.40	6.50
E1	4.30	4.40	4.50
e		0.65 BSC	
L	0.45	0.60	0.75
L1		1.00 REF	
θ	0°		8°



SIDE VIEW



END VIEW

Notes:
(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC MO-153.

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DESCRIPTION:	TSSOP20, 4.4X6.5	PAGE 1 OF 1

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