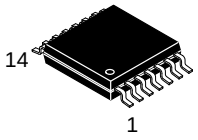
Low Voltage Quad 2-Input NAND Gate

74LVX00



TSSOP−14 WB
CASE 948G

General Description

The LVX00 contains four 2−input NAND gates. The inputs tolerate voltages up to 6.5 V allowing the interface of 5 V systems to 3 V systems.

Features

- Input Voltage Level Translation from 5 V to 3 V
- Ideal for Low Power/Low Noise 3.3 V Applications
- Guaranteed Simultaneous Switching Noise Level and Dynamic Threshold Performance

Logic Symbol

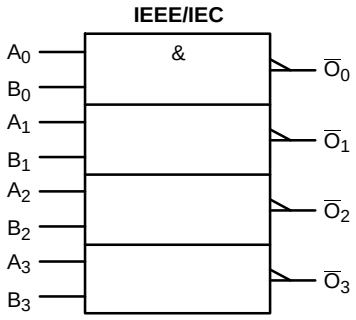
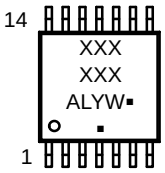


Figure 1. Logic Symbol

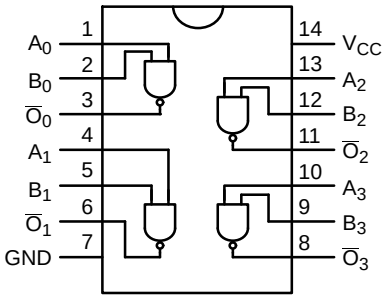
MARKING DIAGRAM



XXX	= Specific Device Code
A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week
▪	= Pb−Free Package

(Note: Microdot may be in either location)

CONNECTION DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Rating
V_{CC}	Supply Voltage		−0.5 V to +6.5 V
I_{IK}	DC Input Diode Current, V_I = −0.5 V		−20 mA
V_I	DC Input Voltage		−0.5 V to 6.5 V
I_{OK}	DC Output Diode Current	V_O = −0.5 V	−20 mA
		V_O = V_{CC} + 0.5 V	+20 mA
V_O	DC Output Voltage		−0.5 V to V_{CC} + 0.5 V
I_O	DC Output Source or Sink Current		±25 mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current		±50 mA
T_{STG}	Storage Temperature		−65°C to +150°C
P_D	Power Dissipation		833 mW

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

PIN DESCRIPTION

Pin Names	Description
A_n, B_n	Inputs
$\overline{O}_n$	Outputs

ORDERING INFORMATION

See detailed ordering and shipping information on page 3 of this data sheet.

RECOMMENDED OPERATING CONDITIONS (Note 1)

Symbol	Parameter	Rating
V_{CC}	Supply Voltage	2.0 V to 3.6 V
V_I	Input Voltage	0 V to 5.5 V
V_O	Output Voltage	0 V to V_{CC}
T_A	Operating Temperature	−40°C to +85°C
$\Delta t / \Delta V$	Input Rise and Fall Time	0 ns/V to 100 ns/V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

1. Unused inputs must be held HIGH or LOW. They may not float.

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	V_{CC} (V)	Conditions	T_A = +25°C			T_A = −40°C to +85°C		Unit
				Min	Typ	Max	Min	Max	
V_{IH}	HIGH Level Input Voltage	2.0		1.5	–	–	1.5	–	V
		3.0		2.0	–	–	2.0	–	
		3.6		2.4	–	–	2.4	–	
V_{IL}	LOW Level Input Voltage	2.0		–	–	0.5	–	0.5	V
		3.0		–	–	0.8	–	0.8	
		3.6		–	–	0.8	–	0.8	
V_{OH}	HIGH Level Output Voltage	2.0	$V_{IN} = V_{IL}$ or V_{IH}, $I_{OH} = -50$ μA	1.9	2.0	–	1.9	–	V
		3.0	$V_{IN} = V_{IL}$ or V_{IH}, $I_{OH} = -50$ μA	2.9	3.0	–	2.9	–	
			$V_{IN} = V_{IL}$ or V_{IH}, $I_{OH} = -4$ mA	2.58	–	–	2.48	–	
V_{OL}	LOW Level Output Voltage	2.0	$V_{IN} = V_{IL}$ or V_{IH}, $I_{OL} = 50$ μA	–	0.0	0.1	–	0.1	V
		3.0	$V_{IN} = V_{IL}$ or V_{IH}, $I_{OL} = 50$ μA	–	0.0	0.1	–	0.1	
			$V_{IN} = V_{IL}$ or V_{IH}, $I_{OL} = 4$mA	–	–	0.36	–	0.44	
I_{IN}	Input Leakage Current	3.6	V_{IN} = 5.5 V or GND	–	–	±0.1	–	±1.0	μA
I_{CC}	Quiescent Supply Current	3.6	$V_{IN} = V_{CC}$ or GND	–	–	2.0	–	20.0	μA

NOISE CHARACTERISTICS (Note 2)

Symbol	Parameter	V_{CC} (V)	C_L (pF)	T_A = 25°C		Unit
				Typ	Limit	
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	3.3	50	0.3	0.5	V
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	3.3	50	−0.3	−0.5	V
V_{IHD}	Minimum HIGH Level Dynamic Input Voltage	3.3	50	–	2.0	V
V_{ILD}	Maximum LOW Level Dynamic Input Voltage	3.3	50	–	0.8	V

2. Input $t_r = t_f$ = 3 ns

AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	V_{CC} (V)	C_L (pF)	T_A = 25°C			T_A = −40°C to +85°C		Unit
				Min	Typ	Max	Min	Max	
t_{PLH}, t_{PHL}	Propagation Delay Time	2.7	15	−	5.4	10.1	1.0	12.5	ns
			50	−	7.9	13.6	1.0	16.0	
		3.3 ±0.3	15	−	4.1	6.6	1.0	7.5	
			50	−	6.6	9.7	1.0	11.0	
t_{OSLH}, t_{OSHL}	Output to Output Skew (Note 3)	2.7	50	−	−	1.5	−	1.5	ns
		3.3		−	−	1.5	−	1.5	

3. Parameter guaranteed by design $t_{OSLH} = |t_{PLHm} - t_{PLHn}|$, $t_{OSHL} = |t_{PHLm} - t_{PHLn}|$

CAPACITANCE

Symbol	Parameter	T_A = 25°C			T_A = −40°C to +85°C		Unit
		Min	Typ	Max	Min	Max	
C_{IN}	Input Capacitance	−	4	10	−	10	pF
C_{PD}	Power Dissipation Capacitance (Note)	−	19	−	−	−	pF

4. CPD is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation:

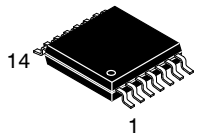
$$I_{CC(opr.)} = \frac{C_{PD} \times V_{CC} \times f_{IN} \times I_{CC}}{4 \text{ (per Gate)}}$$

ORDERING INFORMATION

Device Order Number	Marking	Package	Shipping†
74LVX00MTCX	LVX 00	TSSOP−14 WB (Pb−Free, Halide Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

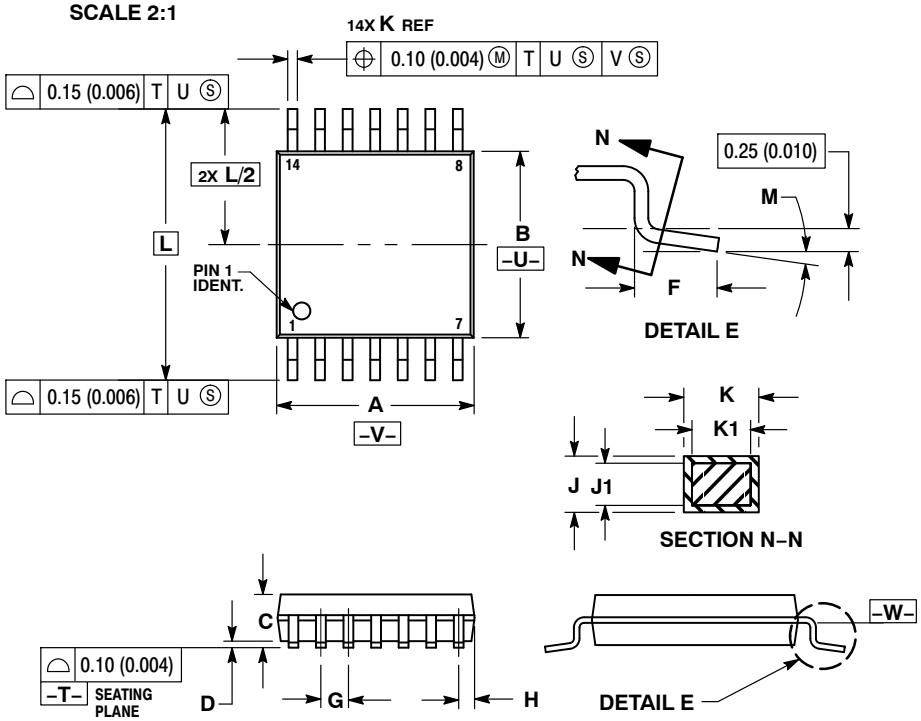
*−Q Suffix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable.



SCALE 2:1

TSSOP−14 WB
CASE 948G
ISSUE C

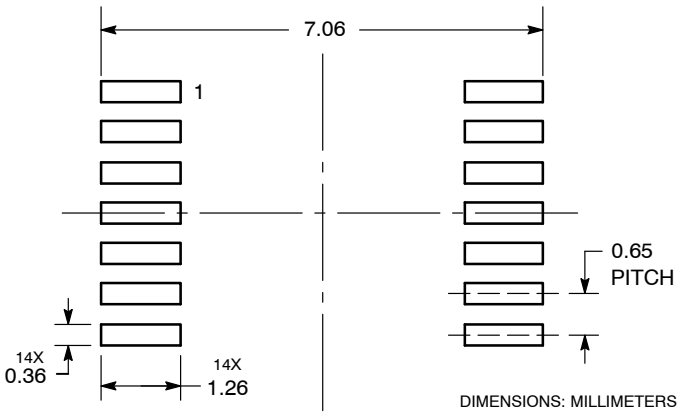
DATE 17 FEB 2016



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

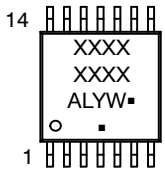
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	−−−	1.20	−−−	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.50	0.60	0.020	0.024
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0 °	8 °	0 °	8 °

RECOMMENDED SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week
▪	= Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	**TSSOP−14 WB**	**PAGE 1 OF 1**

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
Technical Library: www.onsemi.com/design/resources/technical−documentation
onsemi Website: www.onsemi.com

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