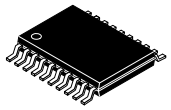
Low Voltage Octal Latch with 3-STATE Outputs

74LVX573



TSSOP20, 4.4x6.5
CASE 948AQ

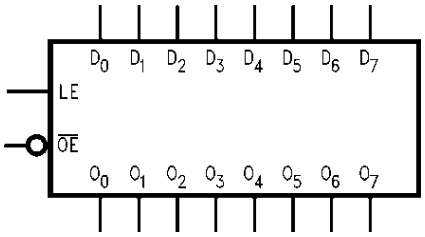
General Description

The LVX573 is a high-speed octal latch with buffered common Latch Enable (LE) and buffered common Output Enable ($\overline{OE}$) inputs. The LVX573 is functionally identical to the LVX373 but with inputs and outputs on opposite sides of the package. The inputs tolerate up to 5.5 V allowing interface of 5 V systems to 3 V systems.

Features

- Input Voltage Translation from 5 V to 3 V
- Ideal for Low Power / Low Noise 3.3 V Applications
- Guaranteed Simultaneous Switching Noise Level and Dynamic Threshold Performance
- This is a Pb-Free Device

Logic Symbol



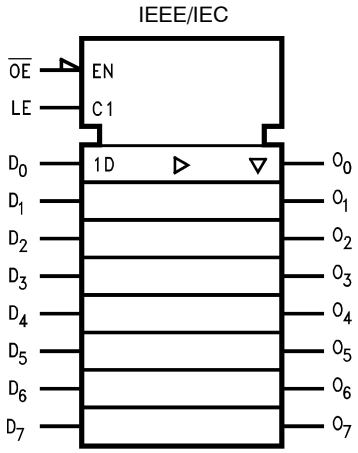
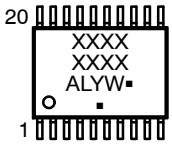


Figure 1. Logic Symbol

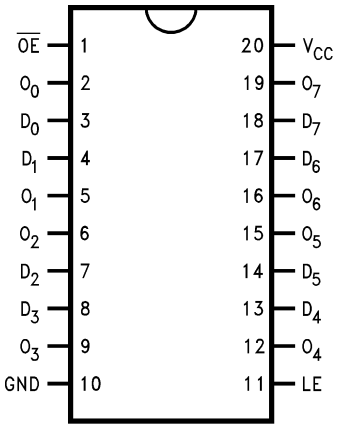
MARKING DIAGRAM



XXXXXX	= Specific Device Code
A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week
▪	= Pb-Free Package

(Note: Microdot may be in either location)

CONNECTION DIAGRAM



PIN DESCRIPTION

Pin Names	Description
D_0 – D_7	Data Inputs
LE	Latch Enable Input
$\overline{OE}$	Output Enable Input
O_0 – O_7	3-STATE Outputs

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 6 of this data sheet.

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Functional Description

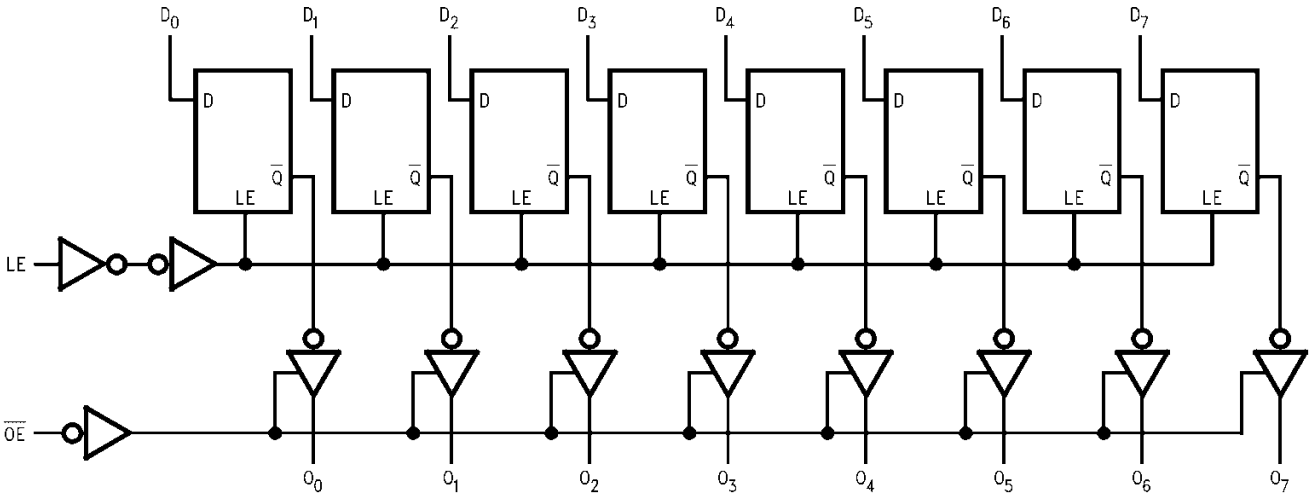
The LVX573 contains eight D-type latches. When the enable (LE) input is HIGH, data on the Dn inputs enters the latches. In this condition the latches are transparent, i.e., a latch output will change state each time its D input changes. When LE is LOW the latches store the informa-tion that was present on the D inputs a setup time preced-ing the HIGH-to-LOW transition of LE. The 3-STATE buffers are controlled by the Output Enable ($\overline{OE}$) input. When $\overline{OE}$ is LOW, the buffers are enabled. When $\overline{OE}$ is HIGH the buffers are in the high impedance mode but this does not interfere with entering new data into the latches.

TRUTH TABLE

Inputs			Outputs
$\overline{OE}$	LE	D	O_n
L	H	H	H
L	H	L	L
L	L	X	O_0
H	X	X	Z

H = HIGH Voltage
L = LOW Voltage
Z = High Impedance
X = Immaterial
O_0 = Previous O_0 before HIGH-to-LOW transition of Latch Enable

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Figure 2. Logic Diagram

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MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_{CC}	DC Supply Voltage		−0.5 to +6.5	V
V_{IN}	DC Input Voltage		−0.5 to +6.5	V
V_{OUT}	DC Output Voltage		−0.5 to V_{CC} + 0.5	V
I_{IN}	DC Input Current, per Pin		±20	mA
I_{OUT}	DC Output Current, per Pin		±25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins		±75	mA
I_{IK}	Input Clamp Current		−20	mA
I_{OK}	Output Clamp Current		±20	mA
T_{STG}	Storage Temperature Range		−65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds		260	°C
T_J	Junction Temperature Under Bias		+150	°C
θ_{JA}	Thermal Resistance (Note 2)	SOIC-20W	96	°C/W
		TSSOP-20	150	
P_D	Power Dissipation in Still Air at 25 °C	SOIC-20W	1302	mW
		TSSOP-20	833	
MSL	Moisture Sensitivity	SOIC-20W	Level 3	–
		All Other Packages	Level 1	
F_R	Flammability Rating	Oxygen Index: 28 to 34	UL 94 V−0 @ 0.573 in	–
V_{ESD}	ESD Withstand Voltage (Note 3)	Human Body Model	2000	V
		Charged Device Model	N/A	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Applicable to devices with outputs that may be tri-stated.
2. Measured with minimum pad spacing on an FR4 board, using 76 mm-by-114 mm, 2-ounce copper trace no air flow per JESD51-7.
3. HBM tested to EIA / JESD22-A114-A. CDM tested to JESD22-C101-A. JEDEC recommends that ESD qualification to EIA/JESD22-A115A (Machine Model) be discontinued.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage	2.0	3.6	V
V_{IN}	DC Input Voltage (Note 4)	0	5.5	V
V_{OUT}	DC Output Voltage (Note 4)	0	V_{CC}	V
T_A	Operating Temperature	−40	+85	°C
t_r, t_f	Input Rise or Fall Rate	0	100	ns/V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

4. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

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DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions		V_{CC}	T_A = 25 °C			T_A = −40 °C to +85 °C		Unit
					Min	Typ	Max	Min	Max	
V_{IH}	HIGH Level Input Voltage			2.0	1.5	–	–	1.5	–	V
				3.0	2.0	–	–	2.0	–	
				3.6	2.4	–	–	2.4	–	
V_{IL}	LOW Level Input Voltage			2.0	–	–	0.5	–	0.5	V
				3.0	–	–	0.8	–	0.8	
				3.6	–	–	0.8	–	0.8	
V_{OH}	HIGH Level Output Voltage	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −50 μA	2.0	1.9	2.0	–	1.9	–	V
			I_{OH} = −50 μA	3.0	2.9	3.0	–	2.9	–	
			I_{OH} = −4 mA	3.0	2.58	–	–	2.48	–	
V_{OL}	LOW Level Output Voltage	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 50 μA	2.0	–	0.0	0.1	–	0.1	V
			I_{OL} = 50 μA	3.0	–	0.0	0.1	–	0.1	
			I_{OL} = 4 mA	3.0	–	–	0.36	–	0.44	
I_{OZ}	3-STATE Output Off-State Current	V_{IN} = V_{IH} or V_{IL}; V_{OUT} = V_{CC} or GND		3.6	–	–	±0.25	–	±2.5	μA
I_{IN}	Input Leakage Current	V_{IN} = 5.5 V or GND		3.6	–	–	±0.1	–	±1.0	μA
I_{CC}	Quiescent Supply Current	V_{IN} = V_{CC} or GND		3.6	–	–	4.0	–	40.0	μA

NOISE CHARACTERISTICS (Note 5)

Symbol	Parameter	C_L (pF)	V_{CC} (V)	T_A = 25 °C		Unit
				Typ	Limits	
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	50	3.3	0.5	0.8	V
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	50	3.3	−0.5	−0.8	V
V_{IHD}	Minimum HIGH Level Dynamic Input Voltage	50	3.3	–	2.0	V
V_{ILD}	Maximum LOW Level Dynamic Input Voltage	50	3.3	–	0.8	V

5. (Input t_r = t_f = 3 ns)

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AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	V_{CC} (V)	T_A = 25 °C			T_A = −40 °C to +85 °C		Unit
				Min	Typ	Max	Min	Max	
t_{PLH}, t_{PHL}	Propagation Delay Time (D_n to O_n)	C_L = 15 pF	2.7	–	7.6	14.5	1.0	17.5	ns
		C_L = 50 pF		–	10.1	18.0	1.0	21.0	
		C_L = 15 pF	3.3 ±0.3	–	5.9	9.3	1.0	11.0	ns
		C_L = 50 pF		–	8.4	12.8	1.0	14.5	
t_{PLH}, t_{PHL}	Propagation Delay Time (LE to O_n)	C_L = 15 pF	2.7	–	8.2	15.6	1.0	18.5	ns
		C_L = 50 pF		–	10.7	19.1	1.0	22.0	
		C_L = 15 pF	3.3 ±0.3	–	6.4	10.1	1.0	12.0	
		C_L = 50 pF		–	8.9	13.6	1.0	15.5	
t_{PZL}, t_{PZH}	3-STATE Output Enable Time	C_L = 15 pF, R_L = 1 kΩ	2.7	–	7.8	15.0	1.0	18.5	ns
		C_L = 50 pF R_L = 1 kΩ		–	10.3	18.5	1.0	22.0	
		C_L = 15 pF R_L = 1 kΩ	3.3 ±0.3	–	6.1	9.7	1.0	12.0	ns
		C_L = 50 pF R_L = 1 kΩ		–	8.6	13.2	1.0	15.5	
t_{PLZ}, t_{PHZ}	3-STATE Output Disable Time	C_L = 50 pF R_L = 1 kΩ	2.7	–	12.1	19.1	1.0	22.0	ns
		C_L = 50 pF R_L = 1 kΩ	3.3 ±0.3	–	10.1	13.6	1.0	15.5	
t_W	LE Pulse Width		2.7	6.5	–	–	7.5	–	ns
			3.3 ±0.3	5.0	–	–	5.0	–	
t_S	Setup Time (D_n to LE)		2.7	5.0	–	–	5.0	–	ns
			3.3 ±0.3	3.5	–	–	3.5	–	
t_H	Hold Time (D_n to LE)		2.7	1.5	–	–	1.5	–	ns
			3.3 ±0.3	1.5	–	–	1.5	–	
t_{OSLH}, t_{OSHL}	Output to Output Skew (Note 6)	C_L = 50 pF	2.7	–	–	1.5	–	1.5	ns
			2.3	–	–	1.5	–	1.5	

6. Parameter guaranteed by design. $t_{OSLH} = |t_{PLHm} - t_{PLHn}|$; $t_{OSHL} = |t_{PHLm} - t_{PHLn}|$

CAPACITANCE

Symbol	Parameter	T_A = 25 °C			T_A = −40 °C to +85 °C		Unit
		Min	Typ	Max	Min	Max	
C_{IN}	Input Capacitance	–	4	10	–	10	pF
C_{OUT}	Output Capacitance	–	6	–	–	–	pF
C_{PD}	Power Dissipation Capacitance (Note 7)	–	27	–	–	–	pF

7. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I_{CC} (opr.) = $C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC} / 8$ (per Latch).

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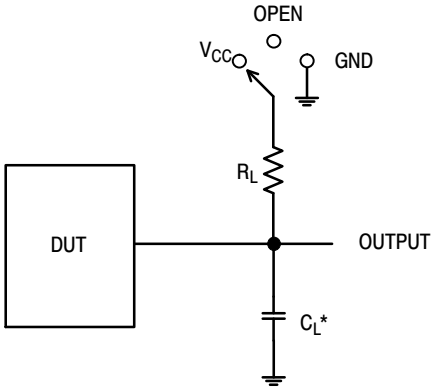
TEST CIRCUITS



Test	Switch Position	C_L	R_L
t_{PLH} / t_{PHL}	Open	See AC Characteristics Table	1 kΩ
t_{PLZ} / t_{PZL}	V_{CC}		
t_{PHZ} / t_{PZH}	GND		

*CL includes probe and jig capacitance
Input $t_R = t_F$ = 3 ns

Figure 3. AC Test Circuit

ORDERING INFORMATION

Device	Marking	Package	Shipping†
74LVX573MTCX	LVX 573	TSSOP-20	2500 Units / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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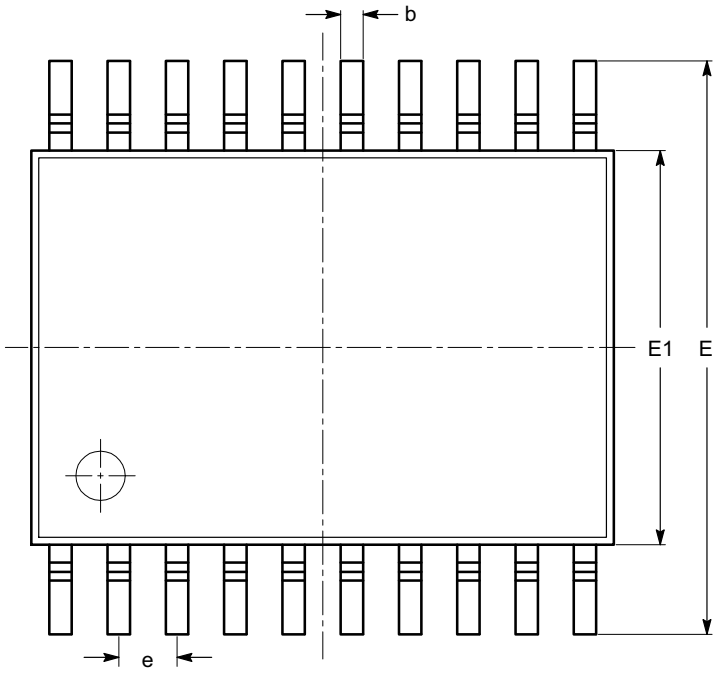
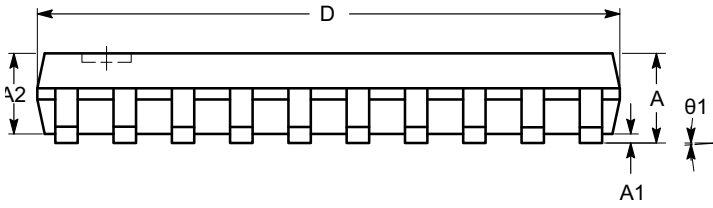
TSSOP20, 4.4x6.5
CASE 948AQ
ISSUE A

DATE 19 MAR 2009

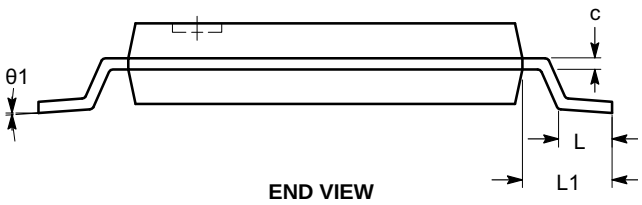


TOP VIEW

SYMBOL	MIN	NOM	MAX
A			1.20
A1	0.05		0.15
A2	0.80		1.05
b	0.19		0.30
c	0.09		0.20
D	6.40	6.50	6.60
E	6.30	6.40	6.50
E1	4.30	4.40	4.50
e		0.65 BSC	
L	0.45	0.60	0.75
L1		1.00 REF	
θ	0°		8°



SIDE VIEW



END VIEW

Notes:
(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC MO-153.

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