Remote Thermal Controller and Voltage Monitor

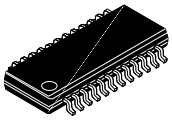
ADT7476A

The ADT7476A controller is a thermal monitor and multiple PWM fan controller for noise-sensitive or power-sensitive applications requiring active system cooling. The ADT7476A can drive a fan using either a low or high frequency drive signal and can monitor the temperature of up to two remote sensor diodes plus its own internal temperature. The part also measures and controls the speed of up to four fans, so the fans operate at the lowest possible speed for minimum acoustic noise.

The automatic fan speed control loop optimizes fan speed for a given temperature. The effectiveness of the system's thermal solution can be monitored using the $\overline{\text{THERM}}$ input. The ADT7476A also provides critical thermal protection to the system using the bidirectional $\overline{\text{THERM}}$ pin as an output to prevent system or component overheating.

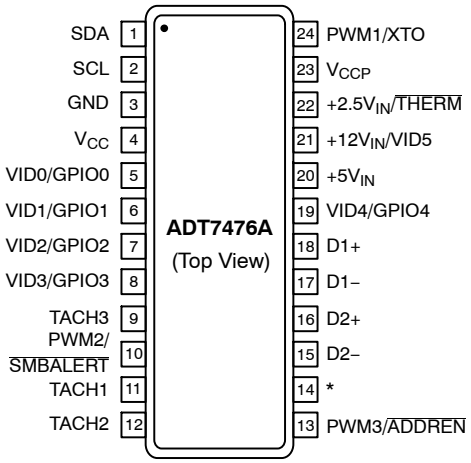
Features

- Monitors Up to Five Voltages
- Improved TACH and PWM Performance
- Controls and Monitors Up to Four Fans
- High and Low Frequency Fan Drive Signal
- One On-Chip and Two Remote Temperature Sensors
- Extended Temperature Measurement Range Up to 191°C
- Automatic Fan Speed Control Mode Controls System Cooling Based on Measured Temperature
- Enhanced Acoustic Mode Dramatically Reduces User Perception of Changing Fan Speeds
- Thermal Protection Feature via $\overline{\text{THERM}}$ Output
- Monitors Performance Impact of Intel® Pentium® 4 Processor
- Thermal Control Circuit via $\overline{\text{THERM}}$ Input
- 3-wire and 4-wire Fan Speed Measurement
- Limit Comparison of All Monitored Values
- 5.0 V Support on all TACH and PWM Channels
- Meets SMBus 2.0 Electrical Specifications
- This Device is Pb-Free, Halogen Free and is RoHS Compliant



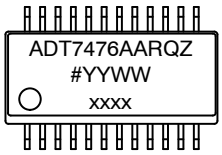
QSOP−24 NB
CASE 492B

PIN ASSIGNMENT



*TACH4/$\overline{\text{THERM}}$/$\overline{\text{SMBALERT}}$/GPIO6/$\overline{\text{ADDR SELECT}}$

MARKING DIAGRAMS



ADT7476AARQZ	= Specific Device Code
#	= Pb-Free Package
YYWW	= Date Code
xxxx	= Assembly Lot Code

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 68 of this data sheet.

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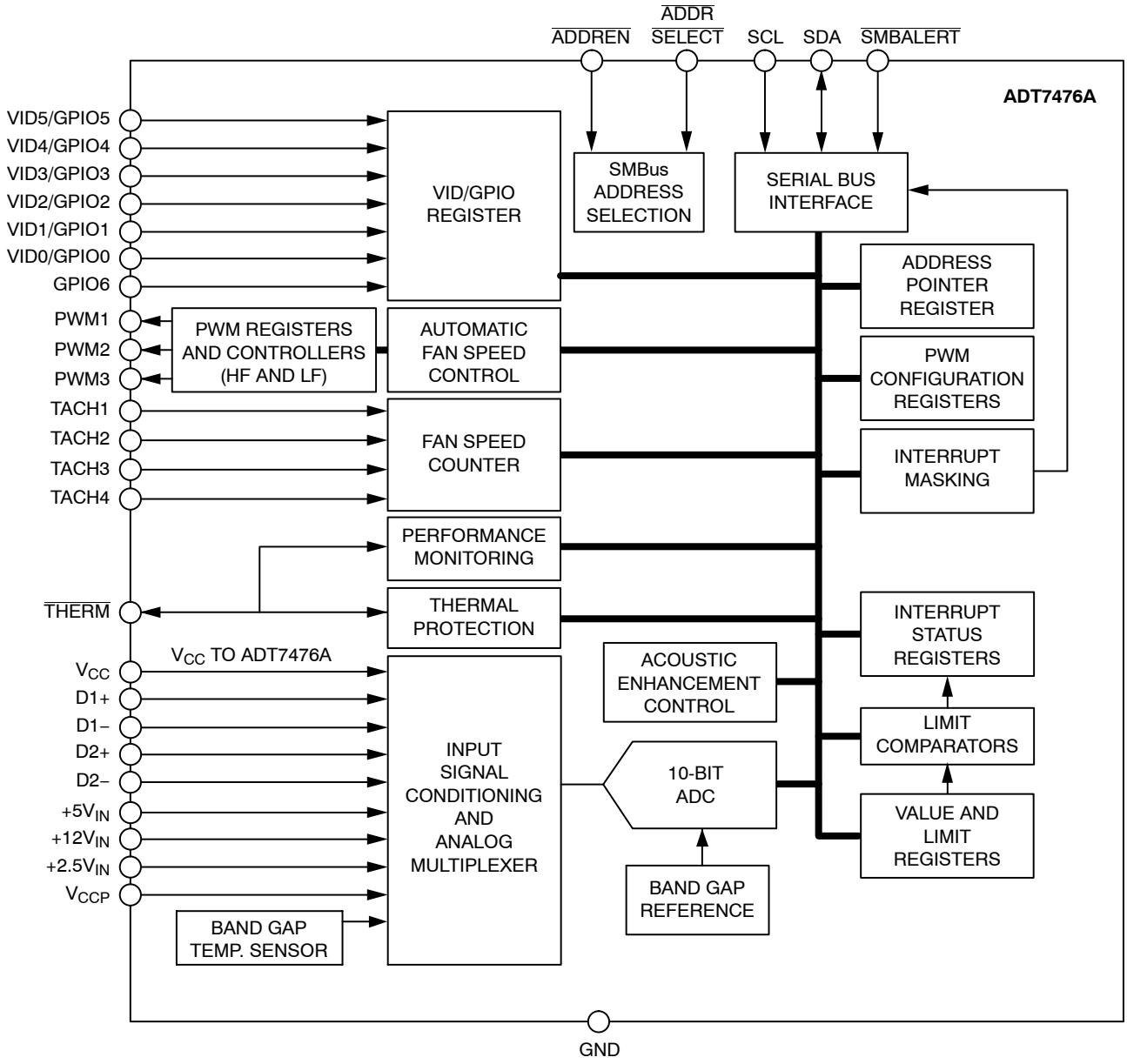


Figure 1. Functional Block Diagram

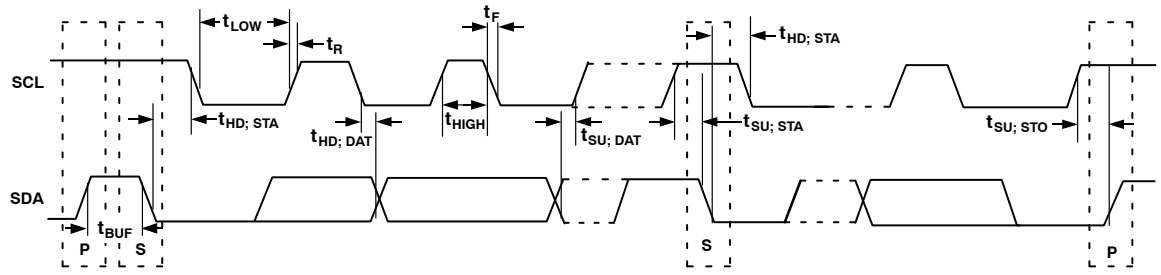


Figure 2. Serial Bus Timing Diagram

Table 1. ABSOLUTE MAXIMUM RATINGS

Parameter	Rating	Unit
Positive Supply Voltage (V_{CC})	3.6	V
Maximum Voltage on +12V_{IN} Pin	16	V
Maximum Voltage on +5.0V_{IN} Pin	6.25	V
Maximum Voltage on SDA, SCL, $\overline{\text{THERM}}$ (Pin 22) and GPIO1−5 Pins	3.6	V
Maximum Voltage on all Tach and PWM Pins	+5.5	V
Voltage on Remaining Input or Output Pins	−0.3 to +4.2	V
Input Current at Any Pin	±5	mA
Package Input Current	±20	mA
Maximum Junction Temperature ($T_{J\ MAX}$)	150	°C
Storage Temperature Range	−65 to +150	°C
Lead Temperature, Soldering IR Reflow Peak Temperature Pb-Free Peak Temperature Lead Temperature (Soldering, 10 sec)	 220 260 300	°C
ESD Rating	1,500	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

NOTE: This device is ESD sensitive. Use standard ESD precautions when handling.

Table 2. THERMAL CHARACTERISTICS (Note 1)

Package Type	θ_{JA}	θ_{JC}	Unit
24-lead QSOP	122	31.25	°C/W

1. $_{JA}$ is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 3. ELECTRICAL CHARACTERISTICS

($T_A = T_{MIN}$ to T_{MAX}, $V_{CC} = V_{MIN}$ to V_{MAX}, unless otherwise noted) (Note 1)

Parameter	Conditions	Min	Typ	Max	Unit
Power Supply					
Supply Voltage		3.0	3.3	3.6	V
Supply Current, I_{CC}	Interface Inactive, ADC Active		1.5	3.0	mA
Temperature-to-Digital Converter					
Local Sensor Accuracy Resolution	0°C ≤ T_A ≤ 85°C −40°C ≤ T_A ≤ 125°C	− − −	±0.5 − 0.25	±1.5 ±2.5 −	°C
Remote Diode Sensor Accuracy Resolution	0°C ≤ T_A ≤ 85°C −40°C ≤ T_A ≤ 125°C	− − −	±0.5 − 0.25	±1.5 ±2.5 −	°C
Remote Sensor Source Current	Low Level High Level	− −	11 180	− −	μA
Analog-to-Digital Converter (Including MUX and Attentuators)					
Total Unadjusted Error (TUE)	For 12 V Channel For All Other Channels	− −	− −	±2 ±1.5	%
Differential Non-Linearity (DNL)	8 Bits	−	−	±1	LSB
Power Supply Sensitivity		−	±0.1	−	%/V
Conversion Time Voltage Input Local Temperature Remote Temperature	Averaging Enabled	− − − −	 11 12 38	− − − −	ms
Total Monitoring Cycle Time	Averaging Enabled Averaging Disabled	− −	145 19	− −	ms
Input Resistance	For V_{CCP} Channel For All Other Channels	70 70	200 114	− −	kΩ

Table 3. ELECTRICAL CHARACTERISTICS (continued)
(T_A = T_{MIN} to T_{MAX}, V_{CC} = V_{MIN} to V_{MAX}, unless otherwise noted) (Note 1)

Parameter	Conditions	Min	Typ	Max	Unit
Fan RPM-to-Digital Converter					
Accuracy	0°C ≤ T_A ≤ 70°C −40°C ≤ T_A ≤ +120°C	– –	– –	±6 ±10	%
Full-Scale Count		–	–	65,535	
Nominal Input RPM	Fan Count = 0xBFFF Fan Count = 0x3FFF Fan Count = 0x0438 Fan Count = 0x021C	– – – –	109 329 5,000 10,000	– – – –	RPM
Open-Drain Digital Outputs, PWM1 TO PWM3, XTO					
Current Sink, I_{OL}		–	–	8.0	mA
Output Low Voltage, V_{OL}	I_{OUT} = −8.0 mA	–	–	0.4	V
High Level Output Current, I_{OH}	V_{OUT} = V_{CC}	–	0.1	20	μA
Open-Drain Serial Data Bus Output (SDA)					
Output Low Voltage, V_{OL}	I_{OUT} = −4.0 mA	–	–	0.4	V
High Level Output Current, I_{OH}	V_{OUT} = V_{CC}	–	0.1	1.0	μA
SMBus Digital Inputs (SCL, SDA) (Note 2)					
Input High Voltage, V_{IH}		2.0	–	–	V
Input Low Voltage, V_{IL}		–	–	0.8	V
Hysteresis		–	500	–	mV
Digital Input Logic Levels (TACH Inputs)					
Input High Voltage, V_{IH}	Maximum Input Voltage	2.0	–	5.5	V
Input Low Voltage, V_{IL}	Minimum Input Voltage	−0.3	–	0.8	V
Hysteresis		–	0.5	–	V p-p
Digital Input Logic Levels ($\overline{\text{THERM}}$) ADTL+					
Input High Voltage, V_{IH}		0.75 × V_{CCP}	–	–	V
Input Low Voltage, V_{IL}		–	–	0.8	V
Digital Input Current					
Input High Current, I_{IH}	V_{IN} = V_{CC}	–	±1	–	μA
Input Low Current, I_{IL}	V_{IN} = 0	–	±1	–	μA
Input Capacitance, C_{IN}		–	5.0	–	pF
Serial Bus Timing (See Figure 2)					
Clock Frequency, f_{SCLK}		10	–	100	kHz
Glitch Immunity, t_{SW}	@ 100 kHz	–	–	50	ns
Bus Free Time, t_{BUF}	@ 100 kHz	4.7	–	–	μs
SCL Low Time, t_{LOW}	@ 100 kHz	4.7	–	–	μs
SCL High Time, t_{HIGH}	@ 100 kHz	4.0	–	50	μs
SCL, SDA Rise Time, t_r	@ 100 kHz	–	–	1,000	ns
SCL, SDA Fall Time, t_f	@ 100 kHz	–	–	300	μs
Data Setup Time, $t_{SU;DAT}$	@ 100 kHz	250	–	–	ns
Detect Clock Low Timeout, $t_{TIMEOUT}$	Can be Optionally Disabled	15	–	35	ms

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. All voltages are measured with respect to GND, unless otherwise specified. Typical voltages are T_A = 25°C and represent a parametric norm. Logic inputs accept input high voltages up to V_{MAX}, even when the device is operating down to V_{MIN}. Timing specifications are tested at logic levels of V_{IL} = 0.8 V for a falling edge, and V_{IH} = 2.0 V for a rising edge.
2. SMBus timing specifications are guaranteed by design and are not production tested.

Table 4. PIN ASSIGNMENT

Pin No.	Mnemonic	Description
1	SDA	Digital I/O (Open Drain). SMBus bidirectional serial data. Requires SMBus pullup.
2	SCL	Digital Input (Open Drain). SMBus serial clock input. Requires SMBus pullup.
3	GND	Ground Pin.
4	V_{CC}	Power Supply. Powered by 3.3 V standby, if monitoring in low power states is required. V_{CC} is also monitored through this pin.
5	VID0/ GPIO0	Digital Input. Voltage supply readouts from CPU. This value is read into the VID/GPIO register (0x43). General-Purpose Open Drain Digital I/O.
6	VID1/ GPIO1	Digital Input. Voltage supply readouts from CPU. This value is read into the VID/GPIO register (0x43). General-Purpose Open Drain Digital I/O.
7	VID2/ GPIO2	Digital Input. Voltage supply readouts from CPU. This value is read into the VID/GPIO register (0x43). General-Purpose Open Drain Digital I/O.
8	VID3/ GPIO3	Digital Input. Voltage supply readouts from CPU. This value is read into the VID/GPIO register (0x43). General-Purpose Open Drain Digital I/O.
9	TACH3	Digital Input (Open Drain). Fan tachometer input to measure speed of Fan 3.
10	PWM2/ $\overline{\text{SMBALERT}}$	Digital Output (Open Drain). Requires 10 kΩ typical pullup. Pulse width modulated output to control Fan 2 speed. Can be configured as a high or low frequency drive. Digital Output (Open Drain). This pin can be reconfigured as an $\overline{\text{SMBALERT}}$ interrupt output to signal out-of-limit conditions.
11	TACH1	Digital Input (Open Drain). Fan tachometer input to measure speed of Fan 1.
12	TACH2	Digital Input (Open Drain). Fan tachometer input to measure speed of Fan 2.
13	PWM3 $\overline{\text{ADDREN}}$	Digital I/O (Open Drain). Pulse width modulated output to control the speed of Fan 3 and Fan 4. Requires 10 kΩ typical pullup. Can be configured as a high or low frequency drive. If pulled low on powerup, the ADT7476A enters address select mode, and the state of Pin 14 ($\overline{\text{ADDR SELECT}}$) determines the ADT7476A's slave address.
14	TACH4/	Digital Input (Open Drain). Fan tachometer input to measure speed of Fan 4.
	$\overline{\text{THERM}}$/ $\overline{\text{SMBALERT}}$/ GPIO6/ $\overline{\text{ADDR SELECT}}$	Alternatively, the pin can be reconfigured as a bidirectional $\overline{\text{THERM}}$ pin. Times and monitors assertions on the $\overline{\text{THERM}}$ input. For example, it can be connected to the $\overline{\text{PROCHOT}}$ output of Intel's Pentium® 4 processor or to the output of a trip point temperature sensor. Can be used as an output to signal overtemperature conditions. Digital Output (Open Drain). This pin can be reconfigured as an $\overline{\text{SMBALERT}}$ interrupt output to signal out-of-limit conditions. General-Purpose Open Drain Digital I/O. If in address select mode, the logic state of this pin defines the SMBus device address.
15	D2−	Cathode Connection to Second Thermal Diode.
16	D2+	Anode Connection to Second Thermal Diode.
17	D1−	Cathode Connection to First Thermal Diode.
18	D1+	Anode Connection to First Thermal Diode.
19	VID4/	Digital Input. Voltage supply readouts from CPU. This value is read into the VID/GPIO register (0x43).
	GPIO4	General-Purpose Open Drain Digital I/O.
20	+5.0 V_{IN}	Analog Input. Monitors 5.0 V power supply.
21	+12 V_{IN}/ VID5	Analog Input. Monitors 12 V power supply. Digital Input. Voltage supply readouts from CPU. This value is read into the VID/GPIO register (0x43).
22	+2.5 V_{IN}/ $\overline{\text{THERM}}$	Analog Input. Monitors 2.5 V supply, typically a chipset voltage. Alternatively, this pin can be reconfigured as a bidirectional/omnidirectional $\overline{\text{THERM}}$ pin. Can be used to time and monitor assertions on the $\overline{\text{THERM}}$ input. For example, can be connected to the $\overline{\text{PROCHOT}}$ output of Intel's Pentium® 4 processor or to the output of a trip point temperature sensor. Can be used as an output to signal overtemperature conditions.
23	V_{CCP}	Analog Input. Monitors processor core voltage (0 V to 3 V).
24	PWM1/ XTO	Digital Output (Open Drain). Pulse width modulated output to control the speed of Fan 1. Requires 10 kΩ typical pullup. Also functions as the output from the XOR tree in XOR test mode.

TYPICAL PERFORMANCE CHARACTERISTICS

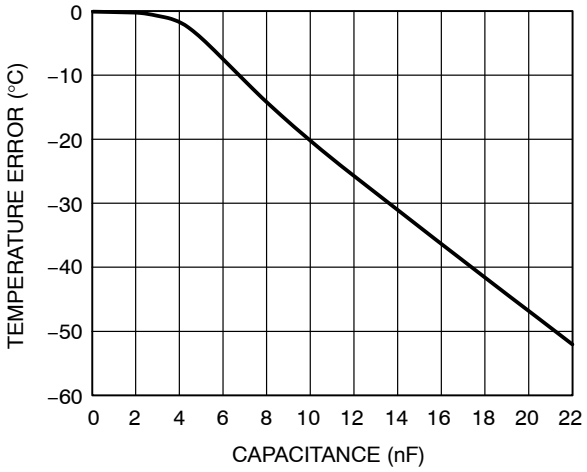


Figure 3. Temperature Error vs. Capacitance Between D+ and D−

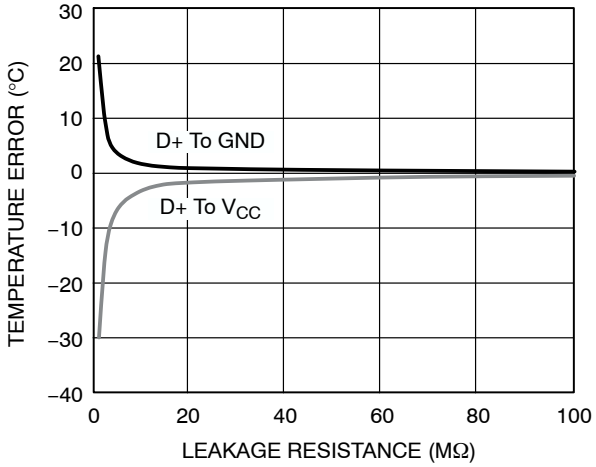


Figure 4. Remote Temperature Error vs. PCB Resistance

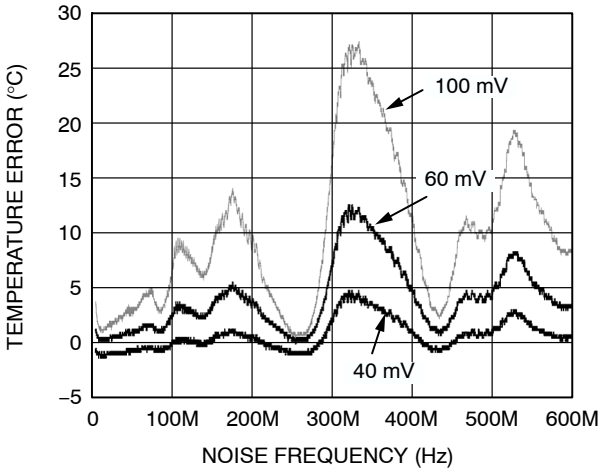


Figure 5. Remote Temperature Error vs. Common-Mode Noise Frequency

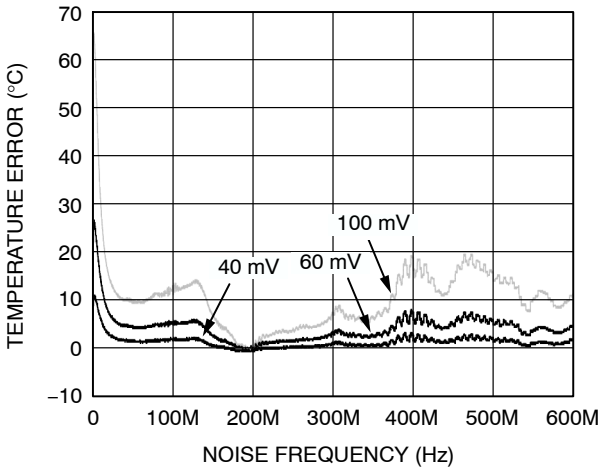


Figure 6. Remote Temperature Error vs. Differential-Mode Noise Frequency

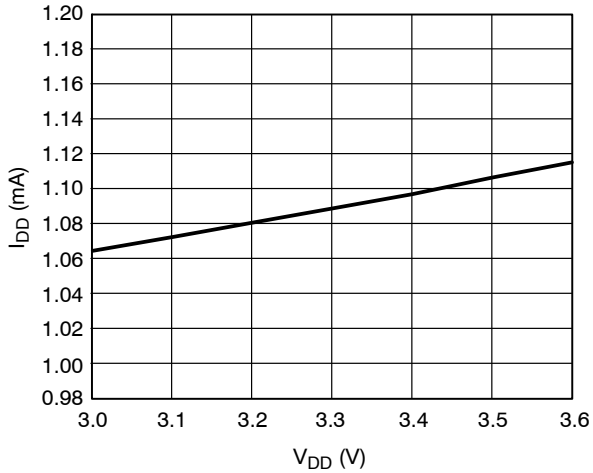


Figure 7. Normal I_{DD} vs. Power Supply

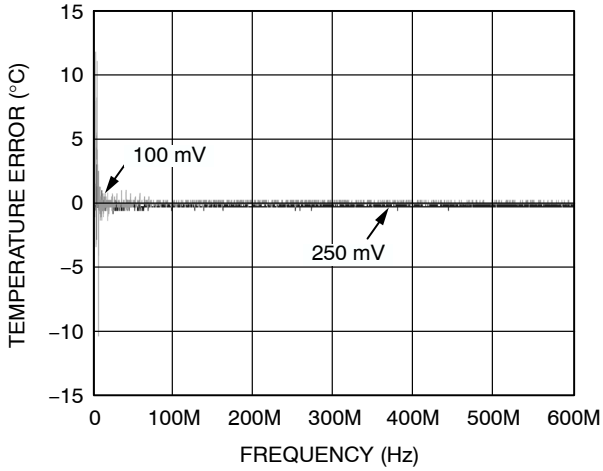


Figure 8. Internal Temperature Error vs. Power Supply Noise

TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

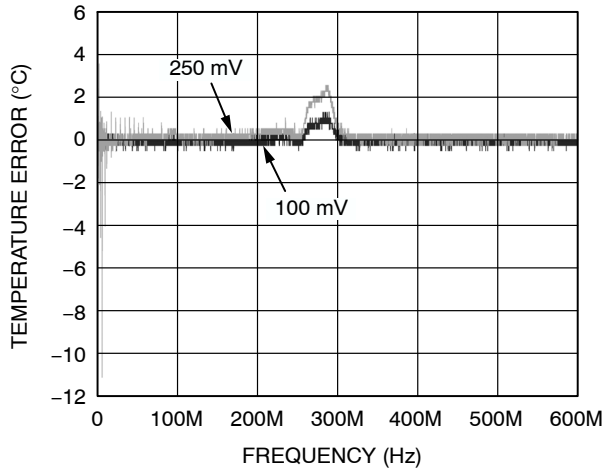


Figure 9. Remote Temperature Error vs. Power Supply Noise Frequency

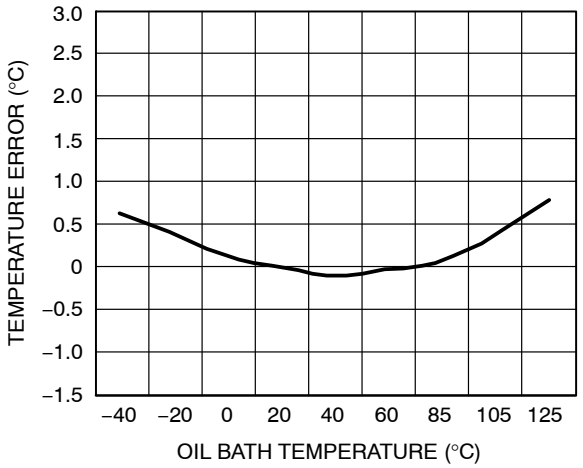


Figure 10. Internal Temperature Error vs. ADT7476A Temperature

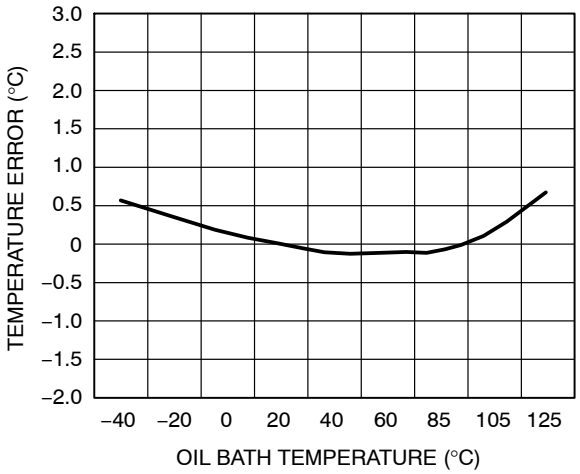


Figure 11. Remote Temperature Error vs. ADT7476A Temperature

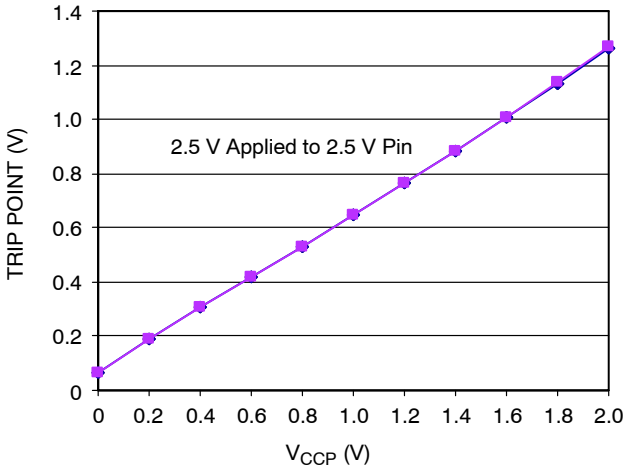


Figure 12. $\overline{\text{THERM}}$ Input Threshold vs. V_{CCP} Voltage

Product Description

The ADT7476A is a complete thermal monitor and multiple fan controller for any system requiring thermal monitoring and cooling. The device communicates with the system via a serial system management bus. The serial bus controller has a serial data line for reading and writing addresses and data (Pin 1), and an input line for the serial clock (Pin 2). All control and programming functions for the ADT7476A are performed over the serial bus. In addition, a pin can be reconfigured as an $\overline{\text{SMBALERT}}$ output to signal out-of-limit conditions.

Feature Comparisons Between ADT7476A and ADT7468

- Dynamic T_{MIN}, dynamic operating point, and associated registers are no longer available in the ADT7476A. The following related registers are gone:
  - Calibration Control 1 (0x36)
  - Calibration Control 2 (0x37)
  - Operating Point (0x33, 0x34, and 0x35)
- Previously (in the ADT7468), T_{RANGE} defined the slope of the automatic fan control algorithm. T_{RANGE} now defines a true temperature range (in the ADT7476A).
- Acoustic filtering is now assigned to temperature zones, not to fans. Available smoothing times have been increased for better acoustic performance.
- Temperature measurements are now made with two switching currents instead of three. SRC is not available in the ADT7476A.
- High frequency PWM can now be enabled/disabled on each PWM output individually.
- $\overline{\text{THERM}}$ can now be enabled/disabled on each temperature channel individually.
- The ADT7476A does not support full shutdown mode.
- The ADT7476A offers increased temperature accuracy on all temperature channels.
- The ADT7476A defaults to twos complement temperature measurement mode.
- Some pins have swapped/added functions.
- The powerup routine for the ADT7476A is simplified.
- The ADT7476A has a higher maximum input voltage TACH/PWM spec, supporting a wider range of fans.
- $V_{CORE_LOW_ENABLE}$ has been reallocated to Bit 7 of Configuration Register 1 (0x40).

Recommended Implementation

Configuring the ADT7476A as shown in Figure 13 allows the system designer to use the following features:

- Two PWM outputs for fan control of up to three fans (the front and rear chassis fans are connected in parallel).
- Three TACH fan speed measurement inputs.
- V_{CC} measured internally through Pin 4.
- CPU temperature measured using Remote 1 temperature channel.
- Remote temperature zone measured through Remote 2 temperature channel.
- Local temperature zone measured through the internal temperature channel.
- Bidirectional $\overline{\text{THERM}}$ pin. This feature allows Intel® Pentium® 4 $\overline{\text{PROCHOT}}$ monitoring and can function as an overtemperature $\overline{\text{THERM}}$ output. It can alternatively be programmed as an $\overline{\text{SMBALERT}}$ system interrupt output.

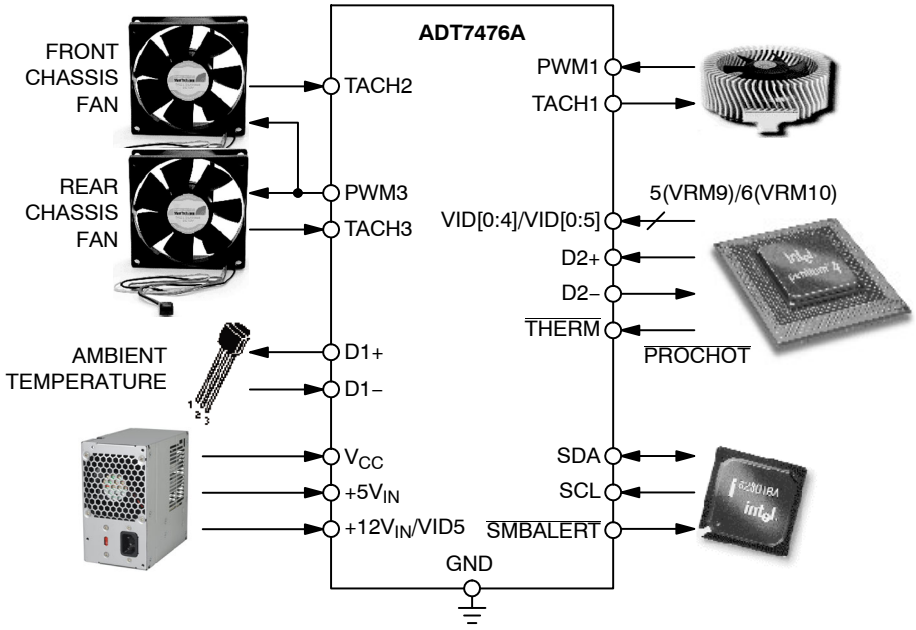


Figure 13. ADT7476A Configuration

Serial Bus Interface

Control of the ADT7476A is carried out using the serial system management bus (SMBus). The ADT7476A is connected to this bus as a slave device, under the control of a master controller. The ADT7476A has a 7-bit serial bus address. When the device is powered up with Pin 13 (PWM3/$\overline{\text{ADDREN}}$) high, the ADT7476A has a default SMBus address of 0101110 or 0x2E. The read/write bit must be added to get the 8-bit address. If more than one ADT7476A is to be used in a system, each ADT7476A is placed in $\overline{\text{ADDR SELECT}}$ mode by strapping Pin 13 low on powerup. The logic state of Pin 14 then determines the device's SMBus address. The logic of these pins is sampled on powerup.

The device address is sampled on powerup and latched on the first valid SMBus transaction, more precisely on the low-to-high transition at the beginning of the eighth SCL pulse, when the serial bus address byte matches the selected slave address. The selected slave address is chosen using the $\overline{\text{ADDREN}}$ pin/$\overline{\text{ADDR SELECT}}$ pin. Any attempted changes in the address have no effect after this.

Table 5. HARDWIRING THE ADT7476A SMBUS DEVICE ADDRESS

Pin 13 State	Pin 14 State	Address
0	Low (10 kΩ to GND)	0101100 (0x2C)
0	High (10 kΩ Pullup)	0101101 (0x2D)
1	Don't Care	0101110 (0x2E)

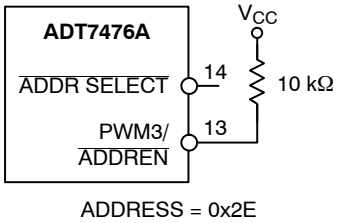


Figure 14. Default SMBus Address = 0x2E

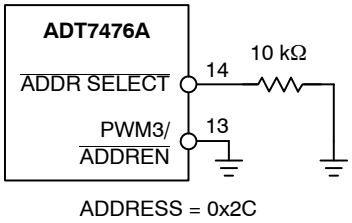


Figure 15. SMBus Address = 0x2C (Pin 14 = 0)

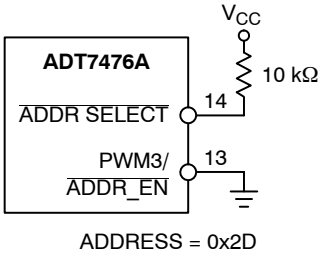
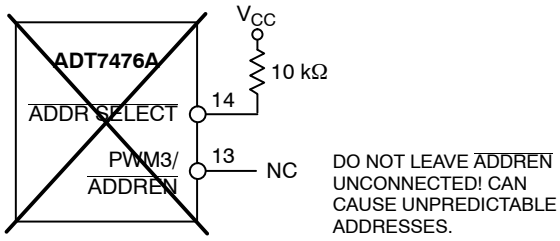


Figure 16. SMBus Address = 0x2D (Pin 14 = 1)



CARE SHOULD BE TAKEN TO ENSURE THAT PIN 13 (PWM3/$\overline{\text{ADDREN}}$) IS EITHER TIED HIGH OR LOW. LEAVING PIN 13 FLOATING COULD CAUSE THE ADT7476A TO POWER UP WITH AN UNEXPECTED ADDRESS.

NOTE THAT IF THE ADT7476A IS PLACED INTO $\overline{\text{ADDR SELECT}}$ MODE, PINS 13 AND 14 CANNOT BE USED AS THE ALTERNATE FUNCTIONS (PWM3, TACH4/$\overline{\text{THERM}}$) UNLESS THE CORRECT CIRCUIT IS MUXED IN AT THE CORRECT TIME OR DESIGNED TO HANDLE THESE DUAL FUNCTIONS.

Figure 17. Unpredictable SMBus Address if Pin 13 is Unconnected

The ability to make hardwired changes to the SMBus slave address allows the user to avoid conflicts with other devices sharing the same serial bus, for example, if more than one ADT7476A is used in a system.

The serial bus protocol operates as follows:

1. The master initiates data transfer by establishing a start condition, which is defined as a high-to-low transition on the serial data line SDA while the serial clock line SCL remains high. This indicates that an address/data stream follows. All slave peripherals connected to the serial bus respond to the start condition and shift in the next eight bits, consisting of a 7-bit address (MSB first), plus a R/$\overline{\text{W}}$ bit, which determine the direction of the data transfer, that is, whether data is written to or read from the slave device.
   The peripheral whose address corresponds to the transmitted address responds by pulling the data line low during the low period before the ninth clock pulse, known as the acknowledge bit. All other devices on the bus now remain idle while the selected device waits for data to be read from or written to it. If the R/$\overline{\text{W}}$ bit is a 0, the master writes to the slave device. If the R/$\overline{\text{W}}$ bit is a 1, the master reads from the slave device.
2. Data is sent over the serial bus in sequences of nine clock pulses, eight bits of data followed by an acknowledge bit from the slave device. Transitions on the data line must occur during the low period of the clock signal and remain stable during the high period. A low-to-high transition, when the clock is high, can be interpreted as a stop signal. The number of data bytes transmitted over the serial bus in a single read or write operation is limited only by what the master and slave devices can handle.
3. When all data bytes have been read or written, stop conditions are established. In write mode, the master pulls the data line high during the 10$^{\text{th}}$

clock pulse to assert a stop condition. In read mode, the master device overrides the acknowledge bit by pulling the data line high during the low period before the ninth clock pulse. This is known as no acknowledge. The master then takes the data line low during the low period before the 10^{th} clock pulse, and then high during the 10^{th} clock pulse to assert a stop condition.

Any number of bytes of data can be transferred over the serial bus in one operation. However, it is not possible to mix read and write in one operation because the type of operation is determined at the beginning and cannot subsequently be changed without starting a new operation. In the ADT7476A, write operations contain either one or two bytes, and read operations contain one byte.

To write data to one of the device data registers or read data from it, the address pointer register must be set so the correct data register is addressed. Then, data can be written into that register or read from it. The first byte of a write operation always contains an address stored in the address pointer register. If data is to be written to the device, then the write operation contains a second data byte that is written to the register selected by the address pointer register.

This write operation is illustrated in Figure 18. The device address is sent over the bus, and then R/$\overline{W}$ is set to 0. This is followed by two data bytes. The first data byte is the address of the internal data register to be written to, which is stored in the address pointer register. The second data byte is the data to be written to the internal data register.

When reading data from a register, there are two possibilities:

1. If the ADT7476A's address pointer register value is unknown, or not the desired value, then it must first be set to the correct value before data can be read from the desired data register. This is done by performing a write to the ADT7476A as before, but only the data byte containing the register address is sent, because no data is written to the register (see Figure 19).
   A read operation is then performed consisting of the serial bus address; R/$\overline{W}$ bit set to 1, followed by the data byte read from the data register (see Figure 20.)
2. If the address pointer register is already known to be at the desired address, data can be read from the corresponding data register without first writing to the address pointer register (see Figure 20).

It is possible to read a data byte from a data register without first writing to the address pointer register, if the address pointer register is already at the correct value. However, it is not possible to write data to a register without writing to the address pointer register, because the first data byte of a write is always written to the address pointer register.

In addition to supporting the send byte and receive byte protocols, the ADT7476A also supports the read byte protocol. See Intel's System Management Bus Specifications Revision 2 for more information.

If several read or write operations must be performed in succession, the master can send a repeat start condition instead of a stop condition to begin a new operation.

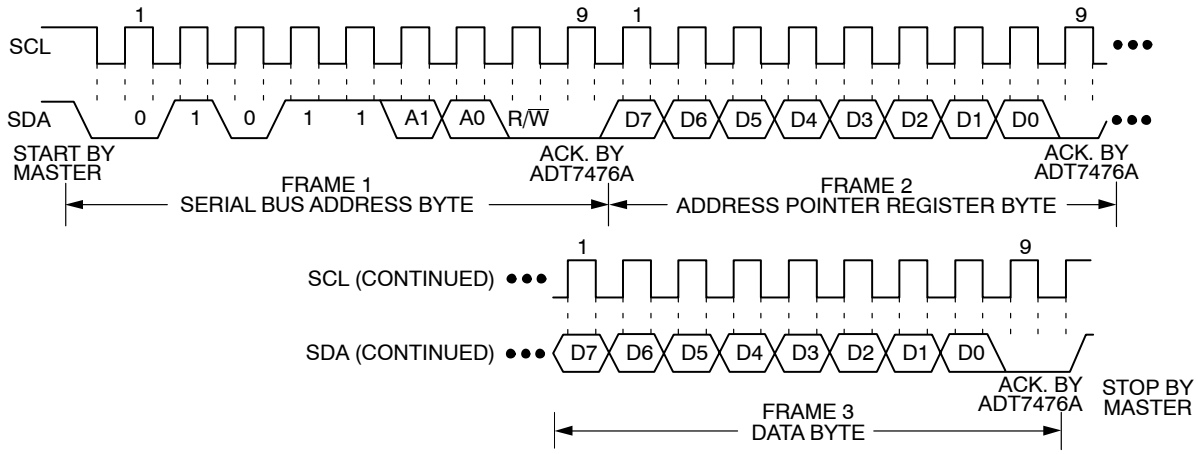


Figure 18. Writing a Register Address to the Address Pointer Register, then Writing Data to the Selected Register

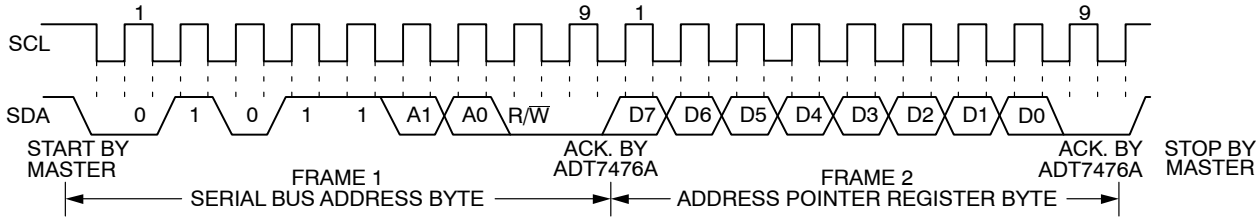


Figure 19. Writing to the Address Pointer Register Only

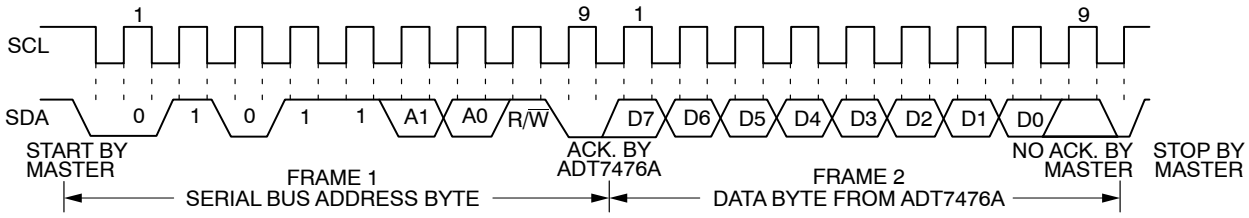


Figure 20. Reading Data from a Previously Selected Register

Write Operations

The SMBus specification defines several protocols for different types of read and write operations. The ones used in the ADT7476A are discussed below. The following abbreviations are used in the diagrams:

- S – START
- P – STOP
- R – READ
- $\overline{W}$– WRITE
- A – ACKNOWLEDGE
- $\overline{A}$ – NO ACKNOWLEDGE

The ADT7476A uses the following SMBus write protocols.

Send Byte

In this operation, the master device sends a single command byte to a slave device, as follows:

1. The master device asserts a start condition on SDA.
2. The master sends the 7-bit slave address followed by the write bit (low).
3. The addressed slave device asserts ACK on SDA.
4. The master sends a command code.
5. The slave asserts ACK on SDA.
6. The master asserts a stop condition on SDA, and the transaction ends.

For the ADT7476A, the send byte protocol is used to write a register address to RAM for a subsequent single-byte read from the same address. This operation is illustrated in Figure 21.

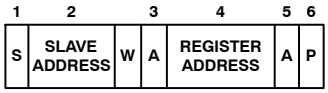


Figure 21. Setting a Register Address for Subsequent Read

If the master is required to read data from the register immediately after setting up the address, it can assert a repeat start condition immediately after the final ACK and carry out a single byte read without asserting an intermediate stop condition.

Write Byte

In this operation, the master device sends a command byte and one data byte to the slave device, as follows:

1. The master device asserts a start condition on SDA.
2. The master sends the 7-bit slave address followed by the write bit (low).
3. The addressed slave device asserts ACK on SDA.
4. The master sends a command code.
5. The slave asserts ACK on SDA.
6. The master sends a data byte.
7. The slave asserts ACK on SDA.
8. The master asserts a stop condition on SDA, and the transaction ends.

This operation is illustrated in Figure 22.

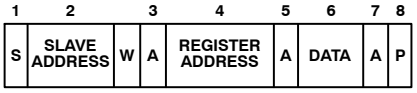


Figure 22. Single-byte Write to a Register

Read Operations

The ADT7476A uses the following SMBus read protocols.

Receive Byte

This operation is useful when repeatedly reading a single register. The register address is set up beforehand. In this operation, the master device receives a single byte from a slave device, as follows:

1. The master device asserts a start condition on SDA.
2. The master sends the 7-bit slave address followed by the read bit (high).
3. The addressed slave device asserts ACK on SDA.
4. The master receives a data byte.
5. The master asserts NO ACK on SDA.
6. The master asserts a stop condition on SDA, and the transaction ends.

In the ADT7476A, the receive byte protocol is used to read a single byte of data from a register whose address has previously been set by a send byte or write byte operation. This operation is illustrated in Figure 23.

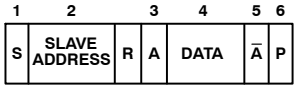


Figure 23. Single-byte Read from a Register

Alert Response Address

Alert response address (ARA) is a feature of SMBus devices, allowing an interrupting device to identify itself to the host when multiple devices exist on the same bus.

The $\overline{\text{SMBALERT}}$ output can be used as either an interrupt output or an $\overline{\text{SMBALERT}}$. One or more outputs can be connected to a common $\overline{\text{SMBALERT}}$ line connected to the master. If a device's $\overline{\text{SMBALERT}}$ line goes low, the following procedure occurs:

1. $\overline{\text{SMBALERT}}$ is pulled low.
2. The master initiates a read operation and sends the alert response address (ARA = 0001 100). This is a general call address that must not be used as a specific device address.
3. The device whose $\overline{\text{SMBALERT}}$ output is low responds to the alert response address, and the master reads its device address. The address of this device is now known and can be interrogated per usual.
4. If more than one device's $\overline{\text{SMBALERT}}$ output is low, the one with the lowest device address has priority in accordance with normal SMBus arbitration.
5. Once the ADT7476A responds to the alert response address, the master must read the status registers, and $\overline{\text{SMBALERT}}$ is cleared only if the error condition goes away.

SMBus Timeout

The ADT7476A includes an SMBus timeout feature. If there is no SMBus activity for 35 ms, the ADT7476A assumes the bus is locked and releases the bus. This prevents the device from locking or holding the SMBus expecting data. Some SMBus controllers cannot handle the SMBus timeout feature, so if necessary, it can be disabled.

Table 6. CONFIGURATION REGISTER 1 (REG. 0x40)

Bit	Description
[6] TODIS	0: SMBus Timeout Enabled (Default) 1: SMBus Timeout Disabled

Virus Protection

To prevent rogue programs or viruses from accessing critical ADT7476A register settings, the lock bit can be set. Setting Bit 1 of Configuration Register 1 (0x40) sets the lock bit and locks critical registers. In this mode, certain registers can no longer be written to until the ADT7476A is powered down and powered up again. For more information on which registers are locked see Table 49.

Voltage Measurement Input

The ADT7476A has four external voltage measurement channels. It can also measure its own supply voltage, V_{CC}. Pin 20 to Pin 23 can measure 5.0 V, 12 V, and 2.5 V supplies, and the processor core voltage V_{CCP} (0 V to 3 V input). The V_{CC} supply voltage measurement is carried out through the V_{CC} pin (Pin 4). The 2.5 V input can be used to monitor a chipset supply voltage in computer systems.

Analog-to-Digital Converter

All analog inputs are multiplexed into the on-chip, successive-approximation, analog-to-digital converter, which has a resolution of 10 bits. The basic input range is 0 V to 2.25 V, but the inputs have built-in attenuators to allow measurement of 2.5 V, 3.3 V, 5.0 V, 12 V, and the processor core voltage V_{CCP} without any external components. To allow the tolerance of these supply voltages, the ADC produces an output of 3/4 full scale (768 dec or 300 hex) for the nominal input voltage, giving it adequate headroom to cope with overvoltages.

Input Circuitry

The internal structure for the analog inputs is shown in Figure 24 The input circuit consists of an input protection diode, an attenuator, plus a capacitor to form a first-order low-pass filter that gives input immunity to high frequency noise.

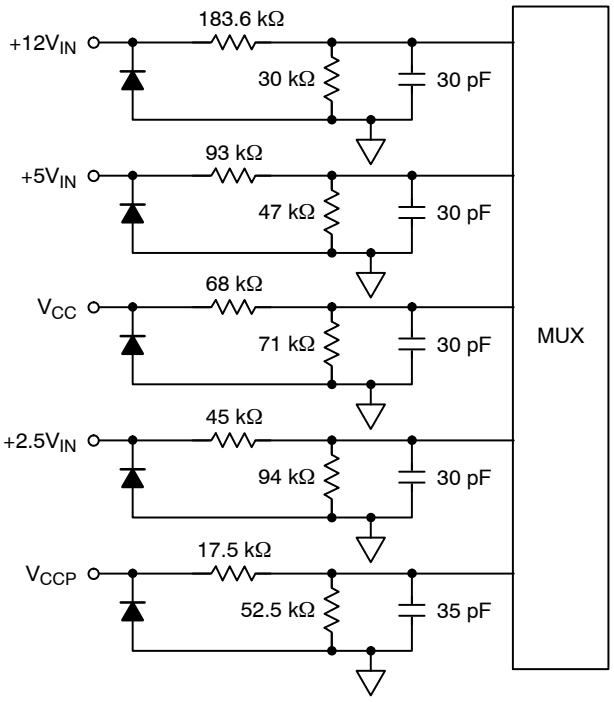


Figure 24. Structure of Analog Inputs

Table 7. VOLTAGE MEASUREMENT REGISTERS

Register	Description	Default
0x20	2.5 V Reading	0x00
0x21	V_{CCP} Reading	0x00
0x22	V_{CC} Reading	0x00
0x23	5.0 V Reading	0x00
0x24	12 V Reading	0x00

Voltage Limit Registers

Associated with each voltage measurement channel is a high and low limit register. Exceeding the programmed high or low limit causes the appropriate status bit to be set. Exceeding either limit can also generate $\overline{\text{SMBALERT}}$ interrupts.

Table 8. VOLTAGE LIMIT REGISTERS

Register	Description	Default
0x44	2.5 V Low Limit	0x00
0x45	2.5 V High Limit	0xFF
0x46	V_{CCP} Low Limit	0x00
0x47	V_{CCP} High Limit	0xFF
0x48	V_{CC} Low Limit	0x00
0x49	V_{CC} High Limit	0xFF
0x4A	5.0 V Low Limit	0x00
0x4B	5.0 V High Limit	0xFF
0x4C	12 V Low Limit	0x00
0x4D	12 V High Limit	0xFF

Table 13 shows the input ranges of the analog inputs and output codes of the 10-bit ADC.

When the ADC is running, it samples and converts a voltage input in 0.7 ms and averages 16 conversions to reduce noise; a measurement takes nominally 11 ms.

Extended Resolution Registers

Voltage measurements can be made with higher accuracy using the extended resolution registers (0x76 and 0x77). Whenever the extended resolution registers are read, the corresponding data in the voltage measurement registers (0x20 to 0x24) is locked until their data is read. That is, if extended resolution is required, then the extended resolution register must be read first, immediately followed by the appropriate voltage measurement register.

Additional ADC Functions for Voltage Measurements

A number of other functions are available on the ADT7476A to offer the system designer increased flexibility.

Turn-off Averaging

For each voltage/temperature measurement read from a value register, 16 readings have been made internally and the results averaged before being placed into the value register. When faster conversions are needed, setting Bit 4 of Configuration Register 2 (0x73) turns averaging off. This effectively gives a reading 16 times faster but the reading can be noisier. The default round robin cycle time takes 146.5 ms.

Table 9. CONVERSION TIME WITH AVERAGING DISABLED

Channel	Measurement Time (ms)
Voltage Channels	0.7
Remote Temperature 1	7
Remote Temperature 2	7
Local Temperature	1.3

When Bit 7 of Configuration Register 6 (0x10) is set, the default round robin cycle time increases to 240 ms.

Bypass All Voltage Input Attenuators

Setting Bit 5 of Configuration Register 2 (0x73) removes the attenuation circuitry from the 2.5 V, V_{CCP}, V_{CC}, 5.0 V, and 12 V inputs. This allows the user to directly connect external sensors or rescale the analog voltage measurement inputs for other applications. The input range of the ADC without the attenuators is 0 V to 2.25 V.

Bypass Individual Voltage Input Attenuators

Bits [7:4] of Configuration Register 4 (0x7D) can be used to bypass individual voltage channel attenuators.

Table 10. BYPASSING INDIVIDUAL VOLTAGE INPUT ATTENUATORS

Configuration Register 4 (0x7D)	
Bit No.	**Channel Attenuated**
[4]	Bypass 2.5 V Attenuator
[5]	Bypass V_{CCP} Attenuator
[6]	Bypass 5.0 V Attenuator
[7]	Bypass 12 V Attenuator

Table 11. CONFIGURATION REGISTER 2 (REG. 0x73)

Bit	Description
[4]	1: Averaging Off
[5]	1: Bypass Input Attenuators
[6]	1: Single-channel Convert Mode

TACH1 Minimum High Byte (0x55)

[7:5] Selects ADC channel for single-channel convert mode.

Single-channel ADC Conversion

While single-channel mode is intended as a test mode that can be used to increase sampling times for a specific channel, and therefore helps to analyze that channel's performance in greater detail, it can also have other applications.

Setting Bit 6 of Configuration Register 2 (0x73) places the ADT7476A into single-channel ADC conversion mode.

In this mode, the ADT7476A can only read a single voltage channel. The selected voltage input is read every 0.7 ms. The appropriate ADC channel is selected by writing to Bits [7:5] of the TACH1 minimum high byte register (0x55).

Table 12. PROGRAMMING SINGLE-CHANNEL ADC MODE

Bits [7:4], Register 0x55	**Channel Selected** (Note 1)
000	2.5 V
001	V_{CCP}
010	V_{CC}
011	5.0 V
100	12 V
101	Remote 1 Temperature
110	Local Temperature
111	Remote 2 Temperature

1. In the process of configuring single-channel ADC conversion mode, the TACH1 minimum high byte is also changed, possibly trading off TACH1 minimum high byte functionality with single-channel mode functionality.

Table 13. 10-BIT ADC OUTPUT CODE VS. V_{IN}

Input Voltage						ADC Output	
12 V_{IN}	5.0 V_{IN}	V_{CC} (3.3 V_{IN})	2.5 V_{IN}	V_{CCP}	V_{TT}/I_{MON}	Decimal	Binary (10 Bits)
<0.0156	<0.0065	<0.0042	<0.0032	<0.00293	<0.00220	0	00000000 00
0.0156 to 0.0312	0.0065 to 0.0130	0.0042 to 0.0085	0.0032 to 0.0065	0.0293 to 0.0058	0.00220 to 0.00440	1	00000000 01
0.0312 to 0.0469	0.0130 to 0.0195	0.0085 to 0.0128	0.0065 to 0.0097	0.0058 to 0.0087	0.00440 to 0,00660	2	00000000 10
0.0469 to 0.0625	0.0195 to 0.0260	0.0128 to 0.0171	0.0097 to 0.0130	0.0087 to 0.0117	0,00660 to 0.00881	3	00000000 11
0.0625 to 0.0781	0.0260 to 0.0325	0.0171 to 0.0214	0.0130 to 0.0162	0.0117 to 0.0146	0.00881 to 0.01100	4	00000001 00
0.0781 to 0.0937	0.0325 to 0.0390	0.0214 to 0.0257	0.0162 to 0.0195	0.0146 to 0.0175	0.01100 to 0.01320	5	00000001 01
0.0937 to 0.1093	0.0390 to 0.0455	0.0257 to 0.0300	0.0195 to 0.0227	0.0175 to 0.0205	0.01320 to 0.01541	6	00000001 10
0.1093 to 0.1250	0.0455 to 0.0521	0.0300 to 0.0343	0.0227 to 0.0260	0.0205 to 0.0234	0.01541 to 0.01761	7	00000001 11
0.1250 to 0.14060	0.0521 to 0.0586	0.0343 to 0.0386	0.0260 to 0.0292	0.0234 to 0.0263	0.01761 to 0.01981	8	00000010 00
–	–	–	–	–	–	–	–
4.0000 to 4.0156	1.6675 to 1.6740	1.1000 to 1.1042	0.8325 to 0.8357	0.7500 to 0.7529	0.5636 to 0.5658	256 (1/4 scale)	01000000 00
–	–	–	–	–	–	–	–
8.0000 to 8.0156	3.3300 to 3.3415	2.2000–2.204 2	1.6650 to 1.6682	1.5000 to 1.5029	1.1272 to 1.1294	512 (1/2 scale)	10000000 00
–	–	–	–	–	–	–	–
12.0000 to 12.0156	5.0025 to 5.0090	3.3000 to 3.3042	2.4975 to 2.5007	2.2500 to 2.2529	1.6809 to 1.6930	768 (3/4 scale)	11000000 00
–	–	–	–	–	–	–	–
15.8281 to 15.8437	6.5983 to 6.6048	4.3527 to 4.3570	3.2942 to 3.2974	2.9677 to 2.9707	2.2301 to 2.2323	1013	11111101 01
15.8437 to 15.8593	6.6048 to 6.6113	4.3570 to 4.3613	3.2974 to 3.3007	2.9707 to 2.9736	2.2323 to 2.2346	1014	11111101 10
15.8593 to 15.8750	6.6113 to 6.6178	4.3613 to 4.3656	3.3007 to 3.3039	2.9736 to 2.9765	2.2346 to 2.2368	1015	11111101 11
15.8750 to 15.8906	6.6178 to 6.6244	4.3656 to 4.3699	3.3039 to 3.3072	2.9765 to 2.9794	2.2368 to 2.23899	1016	11111110 00
15.8906 to 15.9062	6.6244 to 6.6309	4.3699 to 4.3742	3.3072 to 3.3104	2.9794 to 2.9824	2,23899 to 2.2412	1017	11111110 01
15.9062 to 15.9218	6.6309 to 6.6374	4.3742 to 4.3785	3.3104 to 3.3137	2.9824 to 2.9853	2.2412 to 2.2434	1018	11111110 10
15.9218 to 15.9375	6.6374 to 6.4390	4.3785 to 4.3828	3.3137 to 3.3169	2.9853 to 2.9882	2.2434 to 2.2456	1019	11111110 11
15.9375 to 15.9531	6.6439 to 6.6504	4.3828 to 4.3871	3.3169 to 3.3202	2.9882 to 2.9912	2.2456 to 2.2478	1020	11111111 00
15.9531 to 15.9687	6.6504 to 6.6569	4.3871 to 4.3914	3.3202 to 3.3234	2.9912 to 2.9941	2.2478 to 2.25	1021	11111111 01
15.9687 to 15.9843	6.6569 to 6.6634	4.3914 to 4.3957	3.3234 to 3.3267	2.9941 to 2.9970	2.25 to 2.2522	1022	11111111 10
>15.9843	>6.6634	>4.3957	>3.3267	>2.9970	>2.2522	1023	11111111 11

VID Code Monitoring

The ADT7476A has five dedicated voltage ID (VID code) inputs. These are digital inputs that can be read back through the VID/GPIO register (0x43) to determine the processor voltage required or the system being used. Five VID code inputs support VRM9.x solutions. In addition, Pin 21 (12 V input) can be reconfigured as a sixth VID input to satisfy future VRM requirements.

VID/GPIO Register (0x43)

[0] = VID0, reflects logic state of Pin 5.

[1] = VID1, reflects logic state of Pin 6.

[2] = VID2, reflects logic state of Pin 7.

[3] = VID3, reflects logic state of Pin 8.

[4] = VID4, reflects logic state of Pin 19.

[5] = VID5, reconfigurable 12 V input. This bit reads 0 when Pin 21 is configured as the 12 V input. This bit reflects the logic state of Pin 21 when the pin is configured as VID5.

VID Code Input Threshold Voltage

The switching threshold for the VID code inputs is approximately 1.0 V. To enable future compatibility, it is possible to reduce the VID code input threshold to 0.6 V. Bit 6 (THLD) of the VID/GPIO register (0x43) controls the VID input threshold voltage.

VID/GPIO Register (0x43)

[6] THLD = 0, VID switching threshold = 1 V,
V_{OL} < 0.8 V, V_{IH} > 1.7 V, V_{MAX} = 3.3 V.

[6] THLD = 1, VID switching threshold = 0.6 V,
V_{OL} < 0.4 V, V_{IH} > 0.8 V, V_{MAX} = 3.3 V.

Reconfiguring Pin 21 as VID5 Input

Pin 21 can be reconfigured as a sixth VID code input (VID5) for VRM10 compatible systems. Because the pin is configured as VID5, it is not possible to monitor a 12 V supply.

Bit 7 of the VID/GPIO register (0x43) determines the function of Pin 21. System or BIOS software can read the state of Bit 7 to determine whether the system is designed to monitor 12 V or a sixth VID input.

VID/GPIO Register (0x43)

[7] VIDSEL = 0, Pin 21 functions as a 12 V measurement input. Software can read this bit to determine that there are five VID inputs being monitored. Bit 5 of VID/GPIO Register (0x43) always reads back 0. Bit 0 of Interrupt Status Register 2 (0x42) reflects 12 V out-of-limit measurements.

[7] VIDSEL = 1, Pin 21 functions as the sixth VID code input (VID5). Software can read this bit to determine that there are six VID inputs being monitored. Bit 5 of Register 0x43 reflects the logic state of Pin 21. Bit 0 of Interrupt Status Register 2 (0x42) reflects VID code changes.

VID Code Change Detect Function

The ADT7476A has a VID code change detect function. When Pin 21 is configured as the VID5 input, VID code changes are detected and reported back by the ADT7476A. Bit 0 of Interrupt Status Register 2 (0x42) is the 12 V/VC bit and denotes a VID change when set. The VID code change bit is set when the logic states on the VID inputs are different than they were 11 μs previously. The change of VID code is used to generate an $\overline{\text{SMBALERT}}$ interrupt. If an $\overline{\text{SMBALERT}}$ interrupt is not required, Bit 0 of Interrupt Mask Register 2 (0x75), when set, prevents $\overline{\text{SMBALERT}}$s from occurring on VID code changes.

Interrupt Status Register 2 (0x42)

[0] 12 V/VC = 0, if Pin 21 is configured as VID5, Logic 0 denotes no change in VID code within the last 11 μs.

[0] 12 V/VC = 1, if Pin 21 is configured as VID5, Logic 1 means that a change has occurred on the VID code inputs within the last 11 μs. An $\overline{\text{SMBALERT}}$ is generated, if this function is enabled.

Programming the GPIOs

The ADT7476A follows an upgrade path from the ADM1027 to the ADT7476A. In order to maintain consistency between versions, it is necessary to omit references to GPIO5. As a result, there are six GPIOs as follows: GPIO0, GPIO1, GPIO2, GPIO3, GPIO4, and GPIO6.

Setting Bit 4 of Configuration Register 5 (0x7C) to 1 enables GPIO functionality. This turns all pins configured as VID inputs into general-purpose outputs. Writing to the corresponding VID bit in the VID/GPIO register (0x43) sets the polarity for the corresponding GPIO. GPIO6 can be programmed independently as, for example, an input or output, using Bits [3:2] of Configuration Register 5 (0x7C).

Temperature Measurement Method

Local Temperature Measurement

The ADT7476A contains an on-chip band gap temperature sensor whose output is digitized by the on-chip, 10-bit ADC. The 8-bit MSB temperature data is stored in the temperature registers (Addresses 0x25, 0x26, and 0x27). Because both positive and negative temperatures can be measured, the temperature data is stored in Offset 64 format or twos complement format, as shown in Table 14 and Table 15. Theoretically, the temperature sensor and ADC can measure temperatures from −63°C to +127°C (or −61°C to +191°C in the extended temperature range) with a resolution of 0.25°C. However, this exceeds the operating temperature range of the device, so local temperature measurements outside the ADT7476A operating temperature range are not possible.

Table 14. TWOS COMPLEMENT TEMPERATURE DATA FORMAT

Temperature	Digital Output (10-bit) (Note 1)
–128°C	1000 0000 **00** (Diode Fault)
–50°C	1100 1110 **00**
–25°C	1110 0111 **00**
–10°C	1111 0110 **00**
0°C	0000 0000 **00**
+10.25°C	0000 1010 **01**
+25.5°C	0001 1001 **10**
+50.75°C	0011 0010 **11**
+75°C	0100 1011 **00**
+100°C	0110 0100 **00**
+125°C	0111 1101 **00**
+127°C	0111 1111 **00**

1. Bold numbers denote 2 LSB of measurement in the Extended Resolution Register 2 (0x77) with 0.25°C resolution.

Table 15. EXTENDED RANGE, TEMPERATURE DATA FORMAT

Temperature	Digital Output (10-bit) (Note 1)
–64°C	0000 0000 **00** (Diode Fault)
–1°C	0011 1111 **00**
0°C	0100 0000 **00**
1°C	0100 0001 **00**
10°C	0100 1010 **00**
25°C	0101 1001 **00**
50°C	0111 0010 **00**
75°C	1000 1001 **00**
100°C	1010 0100 **00**
125°C	1011 1101 **00**
191°C	1111 1111 **00**

1. Bold numbers denote 2 LSB of measurement in the Extended Resolution Register 2 (0x77) with 0.25°C resolution.

Remote Temperature Measurement

The ADT7476A can measure the temperature of two remote diode sensors or diode-connected transistors connected to Pin 17 and Pin 18, or Pin 15 and Pin 16.

The forward voltage of a diode or diode-connected transistor operated at a constant current exhibits a negative temperature coefficient of about –2 mV/°C. Unfortunately, the absolute value of V_{BE} varies from device to device, and individual calibration is required to null this out. As a result, this technique is unsuitable for mass production. The technique used in the ADT7476A is to measure the change in V_{BE} when the device is operated at two different currents. This is given by:

$$\Delta V_{BE} = \frac{kT}{q} \times \ln(N) \qquad \text{(eq. 1)}$$

where:

k is the Boltzmann's constant.

q is the charge on the carrier.

T is the absolute temperature in Kelvin.

N is the ratio of the two currents.

Figure 25 shows the input signal conditioning used to measure the output of a remote temperature sensor. This figure shows the external sensor as a substrate transistor, which is provided on some microprocessors for temperature monitoring. It could also be a discrete transistor such as a 2N3904/2N3906.

If a discrete transistor is used, the collector is not grounded and is linked to the base. If a PNP transistor is used, the base is connected to the D– input and the emitter to the D+ input. If an NPN transistor is used, the emitter is connected to the D– input and the base to the D+ input. Figure 26 and Figure 27 show how to connect the ADT7476A to an NPN or PNP transistor for temperature measurement. To prevent ground noise from interfering with the measurement, the more negative terminal of the sensor is not referenced to ground, but is biased above ground by an internal diode at the D– input.

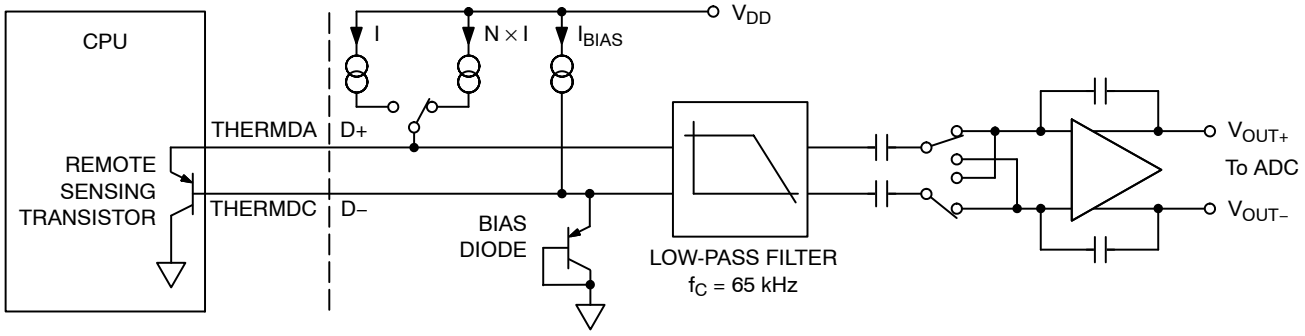


Figure 25. Signal Conditioning for Remote Diode Temperature Sensors

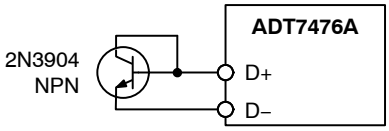


Figure 26. Measuring Temperature by Using an NPN Transistor

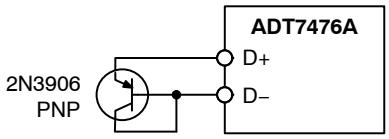


Figure 27. Measuring Temperature by Using an PNP Transistor

To measure ΔV_{BE}, the sensor switches between operating currents of I and N × I. The resulting waveform passes through a 65 kHz low-pass filter to remove noise and through a chopper-stabilized amplifier. The amplifier performs the amplification and rectification of the waveform to produce a dc voltage proportional to ΔV_{BE}. This voltage is measured by the ADC to give a temperature output in 10-bit, twos complement format. To further reduce the effects of noise, digital filtering is performed by averaging the results of 16 measurement cycles.

A remote temperature measurement takes nominally 38 ms. The results of remote temperature measurements are stored in 10-bit, twos complement format, as illustrated in Table 22. The extra resolution for the temperature measurements is held in the Extended Resolution Register 2 (0x77). This gives temperature readings with a resolution of 0.25°C.

Noise Filtering

For temperature sensors operating in noisy environments, previous practice placed a capacitor across the D+ pin and the D− pin to help combat the effects of noise. However, large capacitances affect the accuracy of the temperature measurement, leading to a recommended maximum capacitor value of 1,000 pF.

This capacitor reduces the noise but does not eliminate it, which makes using the sensor difficult in a very noisy environment. In most cases, a capacitor is not required because differential inputs by their very nature have a high immunity to noise.

Factors Affecting Diode Accuracy

Remote Sensing Diode

The ADT7476A is designed to work with substrate transistors built into processors or with discrete transistors. Substrate transistors are generally PNP types with the collector connected to the substrate. Discrete types can be either PNP or NPN transistors connected as a diode (base-shorted to the collector). If an NPN transistor is used, the collector and base are connected to D+ and the emitter to D−. If a PNP transistor is used, the collector and base are connected to D− and the emitter is connected to D+.

To reduce the error due to variations in both substrate and discrete transistors, a number of factors should be taken into consideration:

- The ideality factor, n_f, of the transistor is a measure of the deviation of the thermal diode from ideal behavior. The ADT7476A is trimmed for an n_f value of 1.008. Use the following equation to calculate the error introduced at a temperature T (°C), when using a transistor whose n_f does not equal 1.008 (see the processor's data sheet for the n_f values):

$$\Delta T = (nf - 1.008) \times (273.15\ K + T) \quad \text{(eq. 2)}$$

  To factor this in, the user can write the ΔT value to the offset register. The ADT7476A then automatically adds it to or subtracts it from the temperature measurement.
- Some CPU manufacturers specify the high and low current levels of the substrate transistors. The high current level of the ADT7476A, I_{HIGH}, is 180 μA, and the low level current, I_{LOW}, is 11 μA. If the ADT7476A current levels do not match the current levels specified by the CPU manufacturer, it could be necessary to remove an offset. The CPU's data sheet advises whether this offset needs to be removed and how to calculate it. This offset can be programmed to the offset register. It is important to note that if more than one offset must be considered, then the algebraic sum of these offsets must be programmed to the offset register.

If a discrete transistor is used with the ADT7476A, the best accuracy is obtained by choosing devices according to the following criteria:

- Base-emitter voltage greater than 0.25 V at 11 μA, at the highest operating temperature.
- Base-emitter voltage less than 0.95 V at 180 μA, at the lowest operating temperature.
- Base resistance less than 100 Ω.
- Small variation in the current gain, h_{FE}, (approximately 50 to 150) that indicates tight control of V_{BE} characteristics.

Transistors, such as 2N3904, 2N3906, or equivalents in SOT−23 packages, are suitable devices to use.

Nulling Out Temperature Errors

As CPUs run faster, it is more difficult to avoid high frequency clocks when routing the D+/D− traces around a system board. Even when recommended layout guidelines are followed, some temperature errors can still be attributable to noise coupled onto the D+/D− lines. Constant high frequency noise usually attenuates, or increases, temperature measurements by a linear, constant value.

The ADT7476A has temperature offset registers (0x70 and 0x72) for the Remote 1 and Remote 2 temperature channels. By doing a one-time calibration of the system, the user can determine the offset caused by system board noise

and null it out using the offset registers. The offset registers automatically add a twos complement 8-bit reading to every temperature measurement.

Changing Bit 1 of Configuration Register 5 (0x7C) changes the resolution and therefore, the range of the temperature offset as either having a −63°C to +127°C range with a resolution of 1°C or having a −63°C to +64°C range with a resolution of 0.5°C. This temperature offset can be used to compensate for linear temperature errors introduced by noise.

Table 16. TEMPERATURE OFFSET REGISTERS

Register	Description	Default
0x70	Remote 1 Temperature Offset	0x00 (0°C)
0x71	Local Temperature Offset	0x00 (0°C)
0x72	Remote 2 Temperature Offset	0x00 (0°C)

ADT7463/ADT7476A Backwards Compatible Mode

By setting Bit 0 of Configuration Register 5 (0x7C), all temperature measurements are stored in the zone temperature reading registers (0x25, 0x26, and 0x27) in twos complement in the −63°C to +127°C range. The temperature limits must be reprogrammed in twos complement.

If a twos complement temperature below −63°C is entered, the temperature is clamped to −63°C. In this mode, the diode fault condition remains −128°C = 1000 0000, while in the extended temperature range (−63°C to +191°C), the fault condition is represented by −64°C = 0000 0000.

Table 17. TEMPERATURE READING REGISTERS

Register	Description	Default
0x25	Remote 1 Temperature	–
0x26	Local Temperature	–
0x27	Remote 2 Temperature	–
0x77	Extended Resolution 2	0x00

Table 18. EXTENDED RESOLUTION TEMPERATURE MEASUREMENT REGISTER BITS

Bit	Mnemonic	Description
[7:6]	TDM2	Remote 2 Temperature LSBs
[5:4]	LTMP	Local Temperature LSBs
[3:2]	TDM1	Remote 1 Temperature LSBs

Temperature Limit Registers

Associated with each temperature measurement channel are high and low limit registers. Exceeding the programmed high or low limit causes the appropriate status bit to be set. Exceeding either limit can also generate $\overline{\text{SMBALERT}}$ interrupts (depending on the way the interrupt mask register is programmed and assuming that $\overline{\text{SMBALERT}}$ is set as an output on the appropriate pin).

Table 19. TEMPERATURE LIMIT REGISTERS

Register	Description	Default
0x4E	Remote 1 Temperature Low Limit	0x81
0x4F	Remote 1 Temperature High Limit	0x7F
0x50	Local Temperature Low Limit	0x81
0x51	Local Temperature High Limit	0x7F
0x52	Remote 2 Temperature Low Limit	0x81
0x53	Remote 2 Temperature High Limit	0x7F

Reading Temperature from the ADT7476A

It is important to note that temperature can be read from the ADT7476A as an 8-bit value (with 1°C resolution) or as a 10-bit value (with 0.25°C resolution). If only 1°C resolution is required, the temperature readings can be read back at any time and in no particular order.

If the 10-bit measurement is required, this involves a 2-register read for each measurement. Extended Resolution Register 2 (0x77) should be read first. This causes all temperature reading registers to be frozen until all temperature reading registers have been read from. This prevents an MSB reading from being updated while its two LSBs are being read and vice versa.

Additional ADC Functions for Temperature Measurement

A number of other functions are available on the ADT7476A to offer the system designer increased flexibility.

Turn-off Averaging

For each temperature measurement read from a value register, 16 readings have actually been made internally, and the results averaged, before being placed into the value register. Sometimes it is necessary to take a very fast measurement. Setting Bit 4 of Configuration Register 2 (0x73) turns averaging off. The default round robin cycle time takes 146.5 ms.

Table 20. CONVERSION TIME WITH AVERAGING DISABLED

Channel	Measurement Time (ms)
Voltage Channels	0.7
Remote Temperature 1	7
Remote Temperature 2	7
Local Temperature	1.3

When Bit 7 of Configuration Register 6 (0x10) is set, the default round robin cycle time increases to 240 ms.

Table 21. CONVERSION TIME WITH AVERAGING ENABLED

Channel	Measurement Time (ms)
Voltage Channels	11
Remote Temperature	39
Local Temperature	12

Single-channel ADC Conversions

Setting Bit 6 of Configuration Register 2 (0x73) places the ADT7476A into single-channel ADC conversion mode. In this mode, the ADT7476A can be made to read a single temperature channel only. The appropriate ADC channel is selected by writing to Bits [7:5] of the TACH1 minimum high byte register (0x55).

Table 22. PROGRAMMING SINGLE-CHANNEL ADC MODE FOR TEMPERATURES

Bits [7:5], Register 0x55	Channel Selected
101	Remote 1 Temperature
110	Local Temperature
111	Remote 2 Temperature

Table 23. CONFIGURATION REGISTER 2 (REG. 0x73)

Bit	Description
[4]	1: Averaging Off
[6]	1: Single-channel Convert Mode

TACH1 Minimum High Byte (0x55)

[7:5] selects ADC channel for single-channel convert mode.

Overtemperature Events

Overtemperature events on any of the temperature channels can be detected and dealt with automatically in automatic fan speed control mode. Register 0x6A to Register 0x6C are the $\overline{\text{THERM}}$ temperature limits. When a temperature exceeds its $\overline{\text{THERM}}$ temperature limit, all PWM outputs run at the maximum PWM duty cycle (Register 0x38, Register 0x39, and Register 0x3A). This effectively runs the fans at the fastest allowed speed.

The fans run at this speed until the temperature drops below $\overline{\text{THERM}}$ minus hysteresis. This can be disabled by setting Bit 2, the boost bit, in Configuration Register 3 (0x78). The hysteresis value for the $\overline{\text{THERM}}$ temperature limit is the value programmed into the hysteresis registers (0x6D and 0x6E). The default hysteresis value is 4°C.

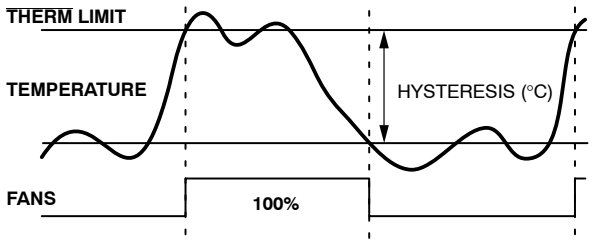


Figure 28. $\overline{\text{THERM}}$ Temperature Limit Operation

$\overline{\text{THERM}}$ can be disabled on specific temperature channels using Bits [7:5] of Configuration Register 5 (0x7C). $\overline{\text{THERM}}$ can also be disabled by:

- Writing −64°C to the appropriate $\overline{\text{THERM}}$ temperature limit in Offset 64 mode.
- Writing −128°C to the appropriate $\overline{\text{THERM}}$ temperature limit in twos complement mode.

Limits, Status Registers, and Interrupts

Limit Values

Associated with each measurement channel on the ADT7476A are high and low limits. These can form the basis of system status monitoring; a status bit can be set for any out-of-limit condition and is detected by polling the device. Alternatively, $\overline{\text{SMBALERT}}$ interrupts can be generated to flag out-of-limit conditions to a processor or microcontroller.

8-bit Limits

The following is a list of 8-bit limits on the ADT7476A.

Table 24. VOLTAGE LIMIT REGISTERS

Register	Description	Default
0x44	2.5 V Low Limit	0x00
0x45	2.5 V High Limit	0xFF
0x46	V_{CCP} Low Limit	0x00
0x47	V_{CCP} High Limit	0xFF
0x48	V_{CC} Low Limit	0x00
0x49	V_{CC} High Limit	0xFF
0x4A	5.0 V Low Limit	0x00
0x4B	5.0 V High Limit	0xFF
0x4C	12 V Low Limit	0x00
0x4D	12 V High Limit	0xFF

Table 25. TEMPERATURE LIMIT REGISTERS

Register	Description	Default
0x4E	Remote 1 Temperature Low Limit	0x81
0x4F	Remote 1 Temperature High Limit	0x7F
0x6A	Remote 1 $\overline{\text{THERM}}$ Temp. Limit	0x64
0x50	Local Temperature Low Limit	0x81
0x51	Local Temperature High Limit	0x7F
0x6B	Local $\overline{\text{THERM}}$ Temperature Limit	0x64
0x52	Remote 2 Temperature Low Limit	0x81
0x53	Remote 2 Temperature High Limit	0x7F
0x6C	Remote 2 $\overline{\text{THERM}}$ Temp. Limit	0x64

Table 26. $\overline{\text{THERM}}$ TIMER LIMIT REGISTER

Register	Description	Default
0x7A	$\overline{\text{THERM}}$ Timer Limit	0x00

16-bit Limits

The fan TACH measurements are 16-bit results. The fan TACH limits are also 16 bits, consisting of a high byte and low byte. Because fans running under speed or stalled are normally the only conditions of interest, only high limits exist for fan TACHs. Because the fan TACH period is actually being measured, exceeding the limit indicates a slow or stalled fan.

Table 27. FAN LIMIT REGISTERS

Register	Description	Default
0x54	TACH1 Minimum Low Byte	0xFF
0x55	TACH1 Minimum High Byte	0xFF
0x56	TACH2 Minimum Low Byte	0xFF
0x57	TACH2 Minimum High Byte	0xFF
0x58	TACH3 Minimum Low Byte	0xFF
0x59	TACH3 Minimum High Byte	0xFF
0x5A	TACH4 Minimum Low Byte	0xFF
0x5B	TACH4 Minimum High Byte	0xFF

Out-of-Limit Comparisons

Once all limits have been programmed, the ADT7476A can be enabled for monitoring. The ADT7476A measures all voltage and temperature measurements in round robin format and sets the appropriate status bit for out-of-limit conditions. TACH measurements are not part of this round robin cycle. Comparisons are done differently depending on whether the measured value is being compared to a high or low limit.

High Limit: > Comparison Performed
Low Limit: ≤ Comparison Performed

Voltage and temperature channels use a window comparator for error detecting and, therefore, have high and low limits. Fan speed measurements use only a low limit. This fan limit is needed only in manual fan control mode.

Analog Monitoring Cycle Time

The analog monitoring cycle begins when a 1 is written to the start bit (Bit 0) of Configuration Register 1 (0x40). The ADC measures each analog input in turn, and, as each measurement is completed, the result is automatically stored in the appropriate value register. This round robin monitoring cycle continues unless disabled by writing a 0 to Bit 0 of Configuration Register 1.

As the ADC is normally left to free-run in this manner, the time taken to monitor all the analog inputs is normally not of interest, because the most recently measured value of any input can be read out at any time.

For applications where the monitoring cycle time is important, it can easily be calculated.

The total number of channels measured is:

- Four Dedicated Supply Voltage Inputs
- Supply Voltage (V_{CC} Pin)
- Local Temperature
- Two Remote Temperatures

As mentioned previously, the ADC performs round robin conversions and takes 11 ms for each voltage measurement, 12 ms for a local temperature reading, and 39 ms for each remote temperature reading. The total monitoring cycle time for averaged voltage and temperature monitoring is, therefore, nominally:

$$(5 \times 11) + 12 + (2 \times 39) = 145 \text{ ms} \quad \text{(eq. 3)}$$

Fan TACH measurements are made in parallel and are not synchronized with the analog measurements in any way.

Status Registers

The results of limit comparisons are stored in Interrupt Status Register 1 and Interrupt Status Register 2. The status register bit for each channel reflects the status of the last measurement and limit comparison on that channel. If a measurement is within limits, the corresponding status register bit is cleared to 0. If the measurement is out-of-limits, the corresponding status register bit is set to 1.

The state of the various measurement channels can be polled by reading the status registers over the serial bus. In Bit 7 (OOL) of Interrupt Status Register 1 (0x41), 1 means an out-of-limit event has been flagged in Interrupt Status Register 2. This means the user also needs to read Interrupt Status Register 2. Alternatively, Pin 10 or Pin 14 can be configured as an $\overline{\text{SMBALERT}}$ output. This hard interrupt automatically notifies the system supervisor of an out-of-limit condition. Reading the status registers clears the appropriate status bit as long as the error condition that caused the interrupt has cleared. Status register bits are *sticky*. Whenever a status bit is set, indicating an out-of-limit condition, it remains set even if the event that caused it has gone away (until read).

The only way to clear the status bit is to read the status register after the event has gone away. Interrupt mask registers (0x74 and 0x75) allow individual interrupt sources to be masked from causing an $\overline{\text{SMBALERT}}$. However, if one of these masked interrupt sources goes out of limit, its associated status bit is set in the status registers.

Table 28. INTERRUPT STATUS REGISTER 1 (0x41)

Bit	Mnemonic	Description
[7]	OOL	1 denotes a bit in Interrupt Status Register 2 is set and Interrupt Status Register 2 should be read.
[6]	R2T	1 indicates that the Remote 2 Temperature High or Low limit has been exceeded.
[5]	LT	1 indicates that the Local Temperature High or Low Limit has been exceeded.
[4]	R1T	1 indicates that the Remote 1 Temperature High or Low Limit has been exceeded.
[3]	5.0 V	1 indicates that the 5.0 V High or Low Limit has been exceeded.
[2]	V_{CC}	1 indicates that the V_{CC} High or Low Limit has been exceeded.
[1]	V_{CCP}	1 indicates that the V_{CCP} High or Low Limit has been exceeded.
[0]	2.5 V	1 indicates that the 2.5 V High or Low Limit has been exceeded. If the 2.5 V input is configured as $\overline{\text{THERM}}$, this bit represents the status of $\overline{\text{THERM}}$.

Table 29. INTERRUPT STATUS REGISTER 2 (0x42)

Bit	Mnemonic	Description
[7]	D2	1 indicates an open or short on D2+/D2− inputs.
[6]	D1	1 indicates an open or short on D1+/D1− inputs.
[5]	F4P	1 indicates Fan 4 has dropped below minimum speed. Alternatively, indicates that the $\overline{\text{THERM}}$ limit has been exceeded, if the $\overline{\text{THERM}}$ function is used. Alternatively, indicates the status of GPIO6.
[4]	FAN3	1 indicates that Fan 3 has dropped below minimum speed.
[3]	FAN2	1 indicates that Fan 2 has dropped below minimum speed.
[2]	FAN1	1 indicates that Fan 1 has dropped below minimum speed.
[1]	OVT	1 indicates that a $\overline{\text{THERM}}$ overtemperature limit has been exceeded.
[0]	12 V/VC	1 indicates a 12 V high or low limit has been exceeded. If the VID code change function is used, this bit indicates a change in VID code on the VID0 to VID4 inputs.

$\overline{\text{SMBALERT}}$ Interrupt Behavior

The ADT7476A can be polled for status, or an $\overline{\text{SMBALERT}}$ interrupt can be generated for out-of-limit conditions. It is important to note how the $\overline{\text{SMBALERT}}$ output and status bits behave when writing interrupt handler software.

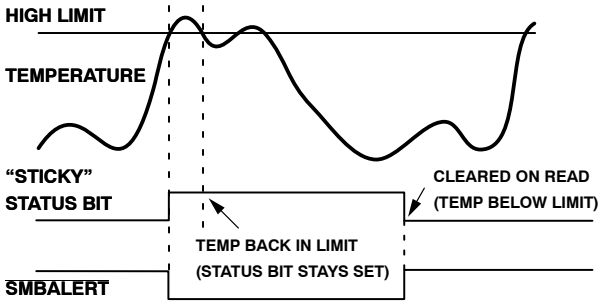


Figure 29. $\overline{\text{SMBALERT}}$ and Status Bit Behavior

Figure 29 shows how the $\overline{\text{SMBALERT}}$ output and sticky status bits behave. Once a limit is exceeded, the corresponding status bit is set to 1. The status bit remains set until the error condition subsides and the status register is read. The status bits are referred to as sticky because they remain set until read by software. This ensures that an out-of-limit event cannot be missed if the software is periodically polling the device.

Note that:

- The $\overline{\text{SMBALERT}}$ output remains low for the entire duration that a reading is out-of-limit and until the status register has been read. This has implications on how software handles the interrupt.
- $\overline{\text{THERM}}$ overtemperature events are not *sticky*. They reset immediately after the overtemperature condition ceases.

Handling $\overline{\text{SMBALERT}}$ Interrupts

To prevent the system from being tied up servicing interrupts, it is recommend to handle the $\overline{\text{SMBALERT}}$ interrupt as follows:

1. Detect the $\overline{\text{SMBALERT}}$ assertion.
2. Enter the interrupt handler.
3. Read the status registers to identify the interrupt source.
4. Mask the interrupt source by setting the appropriate mask bit in the interrupt mask registers (0x74 and 0x75).
5. Take the appropriate action for a given interrupt source.
6. Exit the interrupt handler.
7. Periodically poll the status registers. If the interrupt status bit has cleared, reset the corresponding interrupt mask bit to 0. This causes the $\overline{\text{SMBALERT}}$ output and status bits to behave as shown in Figure 30.

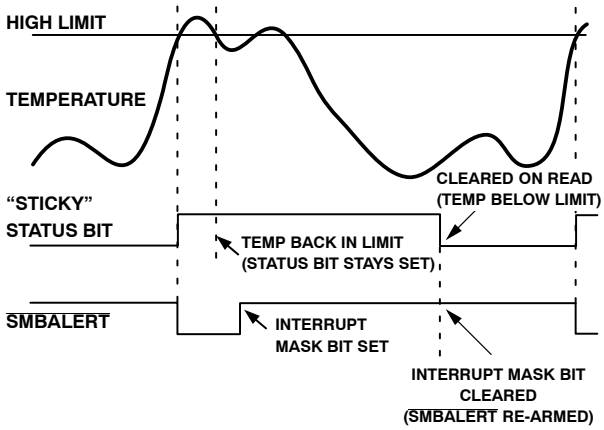


Figure 30. How Masking the Interrupt Source Affects $\overline{\text{SMBALERT}}$ Output

Masking Interrupt Sources

Interrupt Mask Register 1 (0x74) and Interrupt Mask Register 2 (0x75) allow individual interrupt sources to be masked to prevent $\overline{\text{SMBALERT}}$ interrupts.

NOTE: Masking an interrupt source prevents only the $\overline{\text{SMBALERT}}$ output from being asserted; the appropriate status bit is set normally.

Table 30. INTERRUPT MASK REGISTER 1 (0x74)

Bit	Mnemonic	Description
[7]	OOL	1 masks $\overline{\text{SMBALERT}}$ for any alert condition flagged in Interrupt Status Register 2.
[6]	R2T	1 masks $\overline{\text{SMBALERT}}$ for Remote 2 temperature.
[5]	LT	1 masks $\overline{\text{SMBALERT}}$ for Local temperature.
[4]	R1T	1 masks $\overline{\text{SMBALERT}}$ for Remote 1 temperature.
[3]	5.0 V	1 masks $\overline{\text{SMBALERT}}$ for the 5.0 V channel.
[2]	V_{CC}	1 masks $\overline{\text{SMBALERT}}$ for the V_{CC} channel.
[1]	V_{CCP}	1 masks $\overline{\text{SMBALERT}}$ for the V_{CCP} channel.
[0]	2.5 V	1 masks $\overline{\text{SMBALERT}}$ for the 2.5 V_{IN}/$\overline{\text{THERM}}$ channel.

Table 31. INTERRUPT MASK REGISTER 2 (0x75)

Bit	Mnemonic	Description
[7]	D2	1 masks $\overline{\text{SMBALERT}}$ for Diode 2 errors.
[6]	D1	1 masks $\overline{\text{SMBALERT}}$ for Diode 1 errors.
[5]	FAN4	1 masks $\overline{\text{SMBALERT}}$ for Fan 4 failure. If the TACH4 pin is being used as the $\overline{\text{THERM}}$ input, this bit masks $\overline{\text{SMBALERT}}$ for a $\overline{\text{THERM}}$ event. If the TACH4 pin is being used as GPIO6, setting this bit masks interrupts related to GPIO6.
[4]	FAN3	1 masks $\overline{\text{SMBALERT}}$ for Fan 3.
[3]	FAN2	1 masks $\overline{\text{SMBALERT}}$ for Fan 2.
[2]	FAN1	1 masks $\overline{\text{SMBALERT}}$ for Fan 1.
[1]	OVT	1 masks $\overline{\text{SMBALERT}}$ for overtemperature (exceeding $\overline{\text{THERM}}$ limits).
[0]	12 V/VC	1 masks $\overline{\text{SMBALERT}}$ for 12 V channel or for a VID code change, depending on the function used.

Enabling the $\overline{\text{SMBALERT}}$ Interrupt Output

The $\overline{\text{SMBALERT}}$ interrupt function is disabled by default. Pin 10 or Pin 14 can be reconfigured as an $\overline{\text{SMBALERT}}$ output to signal out-of-limit conditions.

Table 32. CONFIGURING PIN 10 AS $\overline{\text{SMBALERT}}$ OUTPUT

Register	Bit Setting
Configuration Register 3 (0x78)	[1] Pin 10 = $\overline{\text{SMBALERT}}$ [0] Pin 10 = PWM2

Assigning $\overline{\text{THERM}}$ Functionality to a Pin

Pin 14 on the ADT7476A has four possible functions: $\overline{\text{SMBALERT}}$, $\overline{\text{THERM}}$, GPIO6, and TACH4. The user chooses the required functionality by setting Bit 0 and Bit 1 of Configuration Register 4 (0x7D).

If $\overline{\text{THERM}}$ is enabled on Bit 1, Configuration Register 3 (0x78):

- Pin 22 becomes $\overline{\text{THERM}}$.
- If Pin 14 is configured as $\overline{\text{THERM}}$ on Bit 0 and Bit 1 of Configuration Register 4 (0x7D), $\overline{\text{THERM}}$ is enabled on this pin.

If $\overline{\text{THERM}}$ is not enabled:

- Pin 22 becomes a 2.5 V measurement input.
- If Pin 14 is configured as $\overline{\text{THERM}}$, then $\overline{\text{THERM}}$ is disabled on this pin.

Table 33. CONFIGURING PIN 14

Bit 1	Bit 0	Function
0	0	TACH4
0	1	$\overline{\text{THERM}}$
1	0	$\overline{\text{SMBALERT}}$
1	1	GPIO6

$\overline{\text{THERM}}$ as an Input

When $\overline{\text{THERM}}$ is configured as an input, the user can time assertions on the $\overline{\text{THERM}}$ pin. This can be useful for connecting to the $\overline{\text{PROCHOT}}$ output of a CPU to gauge system performance.

When the $\overline{\text{THERM}}$ pin is driven low externally, the user can also set up the ADT7476A to run the fans at 100%. The fans run at 100% for the duration of time that the $\overline{\text{THERM}}$ pin is pulled low. This is done by setting the BOOST bit (Bit 2) in Configuration Register 3 (0x78) to 1. This works only if the fan is already running, for example, in manual mode, when the current duty cycle is above 0x00, or in automatic mode when the temperature is above T_{MIN}.

If the temperature is below T_{MIN} or if the duty cycle in manual mode is set to 0x00, pulling the $\overline{\text{THERM}}$ low externally has no effect. See Figure 31 for more information.

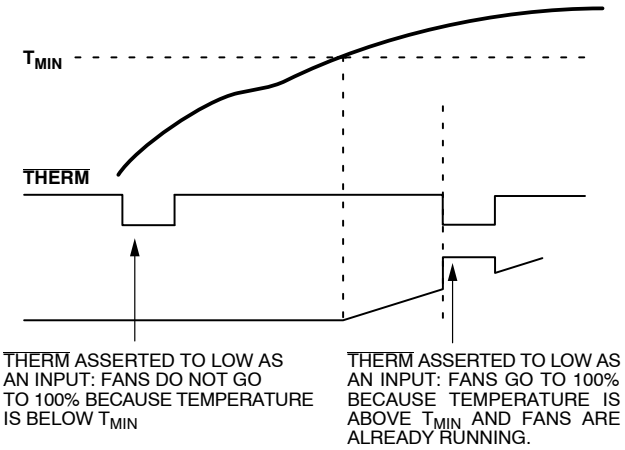


Figure 31. Asserting $\overline{\text{THERM}}$ Low as an Input in Automatic Fan Speed Control Mode

THERM Timer

The ADT7476A has an internal timer to measure THERM assertion time. For example, the THERM input can be connected to the PROCHOT output of a Pentium® 4 CPU to measure system performance. The THERM input can also be connected to the output of a trip-point temperature sensor.

The timer is started on the assertion of the ADT7476A's THERM input and stopped when THERM is de-asserted. The timer counts THERM times cumulatively; that is, the timer resumes counting on the next THERM assertion. The THERM timer continues to accumulate THERM assertion times until the timer is read (where it is cleared), or until it reaches full scale. If the counter reaches full scale, it stops at that reading until cleared.

The 8-bit THERM timer status register (0x79) is designed so that Bit 0 is set to 1 on the first THERM assertion. Once the cumulative THERM assertion time has exceeded 45.52 ms, Bit 1 of the THERM timer is set and Bit 0 now becomes the LSB of the timer with a resolution of 22.76 ms (see Figure 32).

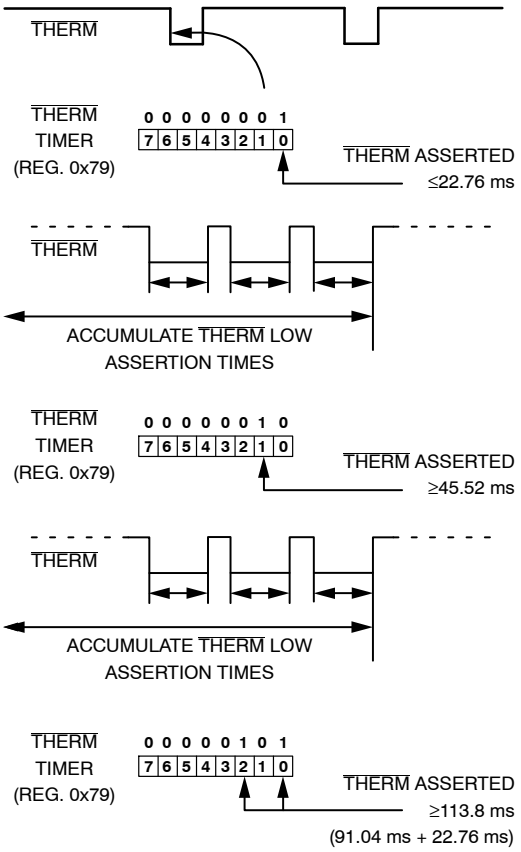


Figure 32. Understanding the THERM Timer

When using the THERM timer, be aware of the following:

After a THERM timer read (0x79)

1. The contents of the timer are cleared on read.
2. The F4P bit (Bit 5) of Interrupt Status Register 2 needs to be cleared (assuming that the THERM timer limit has been exceeded).

If the THERM timer is read during a THERM assertion, the following occurs:

1. The contents of the timer are cleared.
2. Bit 0 of the THERM timer is set to 1, because a THERM assertion is occurring.
3. The THERM timer increments from zero.
4. If the THERM timer limit register (0x7A) = 0x00, the F4P bit is set.

Generating SMBALERT Interrupts from THERM Timer Events

The ADT7476A can generate SMBALERTs when a programmable THERM timer limit has been exceeded. This allows the system designer to ignore brief, infrequent THERM assertions, while capturing longer THERM timer events. Register 0x7A is the THERM timer limit register. This 8-bit register allows a limit from 0 sec (first THERM assertion) to 5.825 sec to be set before an SMBALERT is generated. The THERM timer value is compared with the contents of the THERM timer limit register. If the THERM timer value exceeds the THERM timer limit value, then the F4P bit (Bit 5) of Interrupt Status Register 2 is set and an SMBALERT is generated.

NOTE: Depending on which pins are configured as a THERM timer, setting the F4P bit (Bit 5) of Mask Register 2 (0x75) or Bit 0 of Mask Register 1 (0x74) masks out SMBALERT; although the F4P bit of Interrupt Status Register 2 is still set if the THERM timer limit is exceeded.

Figure 33 is a functional block diagram of the THERM timer, limit, and associated circuitry. Writing a value of 0x00 to the THERM timer limit register (0x7A) causes an SMBALERT to be generated on the first THERM assertion. A THERM timer limit value of 0x01 generates an SMBALERT once cumulative THERM assertions exceed 45.52 ms.

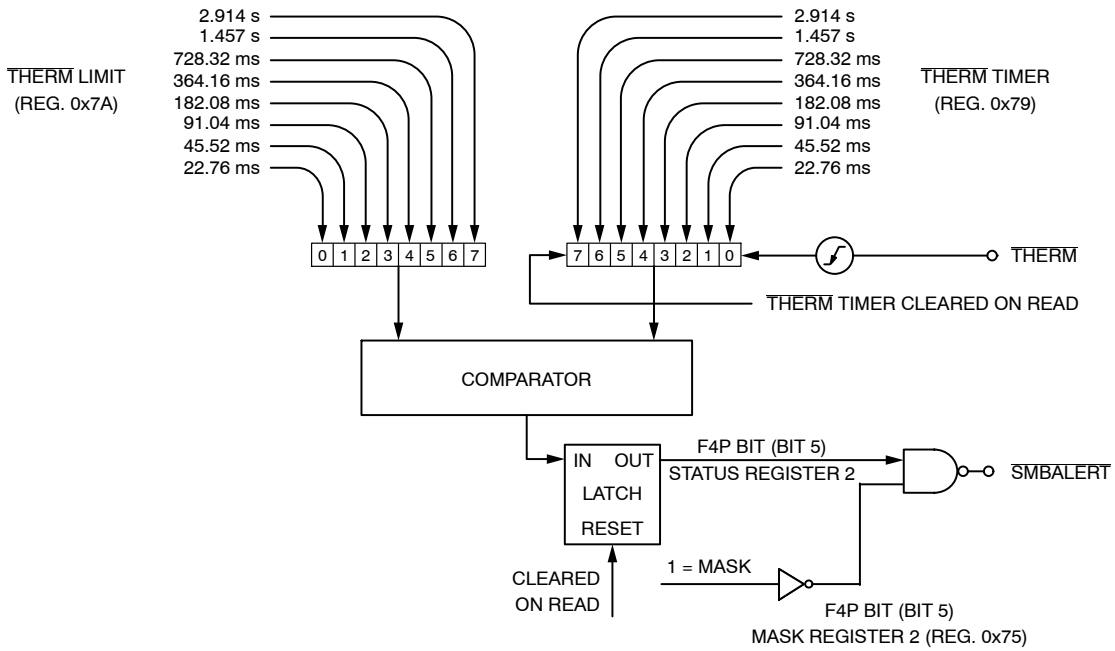


Figure 33. Functional Block Diagram of THERM Monitoring Circuitry

Configuring the Relevant THERM Behavior

1. Configure the desired pin as the THERM timer input.
   Setting Bit 1 (THERM timer enable) of Configuration Register 3 (0x78) enables the THERM timer monitoring functionality. This is disabled on Pin 14 and Pin 22 by default.
   Setting Bit 0 and Bit 1 (PIN14FUNC) of Configuration Register 4 (0x7D) enables THERM timer output functionality on Pin 22 (Bit 1 of Configuration Register 3, THERM, must also be set). Pin 14 can also be used as TACH4.
2. Select the desired fan behavior for THERM timer events.
   Assuming the fans are running, setting Bit 2 (BOOST bit) of Configuration Register 3 (0x78) causes all fans to run at 100% duty cycle whenever THERM is asserted. This allows fail-safe system cooling. If this bit is 0, the fans run at their current settings and are not affected by THERM events. If the fans are not already running when THERM is asserted, then the fans do not run to full speed.
3. Select whether THERM timer events should generate SMBALERT interrupts.
   Setting Bit 5 (F4P) of Mask Register 2 (0x75) or Bit 0 of Mask Register 1 (0x74), depending on which pins are configured as a THERM timer, masks SMBALERTs when the THERM timer limit value is exceeded. This bit should be cleared if SMBALERTs based on THERM events are required.
4. Select a suitable THERM limit value.
   This value determines whether an SMBALERT is generated on the first THERM assertion, or if only a cumulative THERM assertion time limit is exceeded. A value of 0x00 causes an SMBALERT to be generated on the first THERM assertion.
5. Select a THERM monitoring time.
   This value specifies how often OS- or BIOS-level software checks the THERM timer. For example, BIOS can read the THERM timer once an hour to determine the cumulative THERM assertion time. If, for example, the total THERM assertion time is <22.76 ms in Hour 1, >182.08 ms in Hour 2, and >5.825 s in Hour 3, system performance is degrading significantly because THERM is asserting more frequently on an hourly basis. Alternatively, OS- or BIOS-level software can timestamp when the system is powered on. If an SMBALERT is generated due to the THERM timer limit being exceeded, another timestamp can be taken. The difference in time can be calculated for a fixed THERM timer limit time. For example, if it takes one week for a THERM timer limit of 2.914 sec to be exceeded, and the next time it takes only 1 hour, then a serious degradation in system performance has occurred.

Configuring the THERM Pin as an Output

In addition to monitoring THERM as an input, the ADT7476A can optionally drive THERM low as an output. When PROCHOT is bidirectional, THERM can be used to throttle the processor by asserting PROCHOT. The user can preprogram system-critical thermal limits. If the temperature exceeds a thermal limit by 0.25°C, THERM asserts low. If the temperature is still above the thermal limit on the next monitoring cycle, THERM stays low. THERM remains asserted low until the temperature is equal to or

below the thermal limit. Because the temperature for that channel is measured only once for every monitoring cycle, after $\overline{\text{THERM}}$ asserts, it is guaranteed to remain low for at least one monitoring cycle.

The $\overline{\text{THERM}}$ pin can be configured to assert low, if the Remote 1, local, or Remote 2 $\overline{\text{THERM}}$ temperature limits are exceeded by 0.25°C. The $\overline{\text{THERM}}$ temperature limit registers are at Register 0x6A, Register 0x6B, and Register 0x6C, respectively. Setting Bits [5:7] of Configuration Register 5 (0x7C) enables the $\overline{\text{THERM}}$ output feature for the Remote 1, local, and Remote 2 temperature channels, respectively. Figure 34 shows how the $\overline{\text{THERM}}$ pin asserts low as an output in the event of a critical overtemperature.

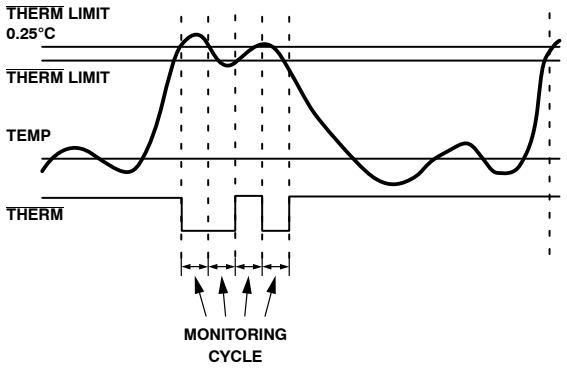


Figure 34. Asserting $\overline{\text{THERM}}$ as an Output, Based on Tripping $\overline{\text{THERM}}$ Limits

An alternative method of disabling $\overline{\text{THERM}}$ is to program the $\overline{\text{THERM}}$ temperature limit to –63°C or less in Offset 64 mode, or –128°C or less in twos complement mode; that is, for $\overline{\text{THERM}}$ temperature limit values less than –63°C or –128°C, respectively, $\overline{\text{THERM}}$ is disabled.

Enabling and Disabling THERM on individual Channels

$\overline{\text{THERM}}$ can be enabled/disabled for individual or combinations of temperature channels using Bits [7:5] of Configuration Register 5 (0x7C).

$\overline{\text{THERM}}$ Hysteresis

Setting Bit 0 of Configuration Register 7 (0x11) disables $\overline{\text{THERM}}$ hysteresis.

If $\overline{\text{THERM}}$ hysteresis is enabled and $\overline{\text{THERM}}$ is disabled (Bit 2 of Configuration Register 4, 0x7D), the $\overline{\text{THERM}}$ pin does not assert low when a $\overline{\text{THERM}}$ event occurs. If $\overline{\text{THERM}}$ hysteresis is disabled and $\overline{\text{THERM}}$ is disabled (Bit 2 of Configuration Register 4, 0x7D) and assuming the appropriate pin is configured as $\overline{\text{THERM}}$), the $\overline{\text{THERM}}$ pin asserts low when a $\overline{\text{THERM}}$ event occurs.

If $\overline{\text{THERM}}$ and $\overline{\text{THERM}}$ hysteresis are both enabled, the $\overline{\text{THERM}}$ output asserts as expected.

$\overline{\text{THERM}}$ Operation in Manual Mode

In manual mode, $\overline{\text{THERM}}$ events do not cause fans to go to full speed, unless Bit 3 of Configuration Register 6 (0x10) is set to 1.

Additionally, Bit 3 of Configuration Register 4 (0x7D) can be used to select the PWM speed on a $\overline{\text{THERM}}$ event (100% or maximum PWM).

Bit 2 in Configuration Register 4 (0x7D) can be set to disable $\overline{\text{THERM}}$ events from affecting the fans.

Fan Drive Using PWM Control

The ADT7476A uses pulse-width modulation (PWM) to control fan speed. This relies on varying the duty cycle (or on/off ratio) of a square wave applied to the fan to vary the fan speed. The external circuitry required to drive a fan using PWM control is extremely simple. For 4-wire fans, the PWM drive might need only a pullup resistor. In many cases, the 4-wire fan PWM input has a built-in, pullup resistor.

The ADT7476A PWM frequency can be set to a selection of low frequencies or a single high PWM frequency. The low frequency options are used for 3-wire fans, while the high frequency option is usually used with 4-wire fans.

For 3-wire fans, a single N-channel MOSFET is the only drive device required. The specifications of the MOSFET depend on the maximum current required by the fan being driven and the input capacitance of the FET. Because a 10 kΩ (or greater) resistor must be used as a PWM pullup, an FET with large input capacitance can cause the PWM output to become distorted and adversely affect the fan control range. This is a requirement only when using high frequency PWM mode.

Typical notebook fans draw a nominal 170 mA, so SOT devices can be used where board space is a concern. In desktops, fans typically draw 250 mA to 300 mA each. If you drive several fans in parallel from a single PWM output or drive larger server fans, the MOSFET must handle the higher current requirements. The only other stipulation is that the MOSFET should have a gate voltage drive, V_{GS} < 3.3 V, for direct interfacing to the PWM output pin. The MOSFET should also have a low on resistance to ensure that there is not a significant voltage drop across the FET, which would reduce the voltage applied across the fan and, therefore, the maximum operating speed of the fan.

Figure 35 shows how to drive a 3-wire fan using PWM control.

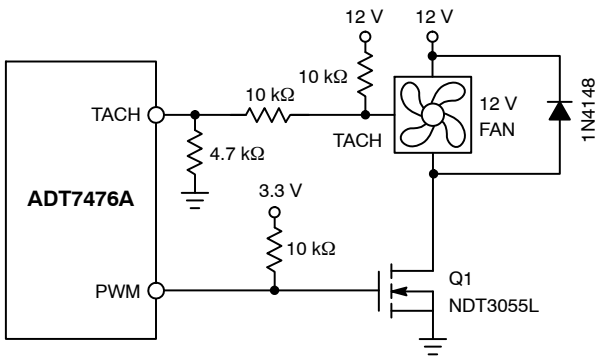


Figure 35. Driving a 3-wire Fan Using an N-channel MOSFET

Figure 35 uses a 10 kΩ pullup resistor for the TACH signal. This assumes that the TACH signal is an open-collector from the fan. In all cases, the TACH signal from the fan must be kept below 5.5 V maximum to prevent damaging the ADT7476A.

Figure 36 shows a fan drive circuit using an NPN transistor such as a general-purpose MMBT2222. While these devices are inexpensive, they tend to have much lower current handling capabilities and higher on resistance than MOSFETs. When choosing a transistor, care should be taken to ensure that it meets the fan's current requirements. Ensure that the base resistor is chosen so that the transistor is saturated when the fan is powered on.

Because the fan drive circuitry in 4-wire fans is not switched on or off, as with previous PWM driven/powered fans, the internal drive circuit is always on and uses the PWM input as a signal instead of a power supply. This enables the internal fan drive circuit to perform better than 3-wire fans, especially for high frequency applications.

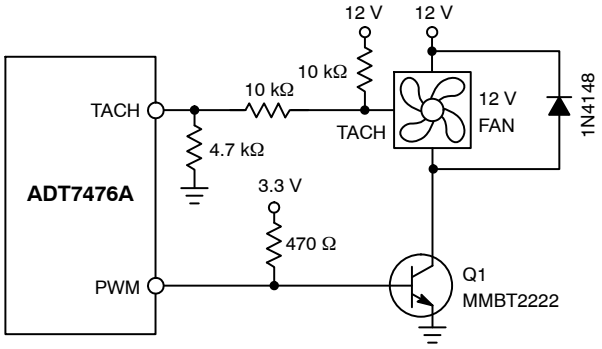


Figure 36. Driving a 3-wire Fan Using an NPN Transistor

Figure 37 shows a typical drive circuit for 4-wire fans.

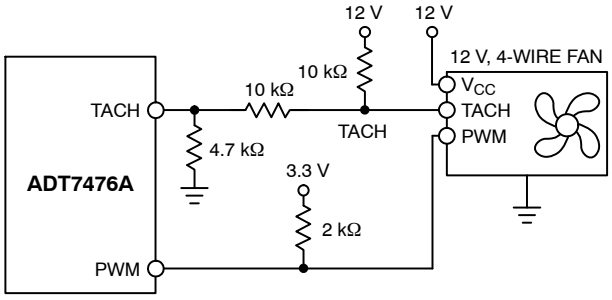


Figure 37. Driving a 4-wire Fan

Driving Two Fans from PWM3

The ADT7476A has four TACH inputs available for fan speed measurement, but only three PWM drive outputs. If a fourth fan is being used in the system, it should be driven from the PWM3 output in parallel with the third fan. Figure 38 shows how to drive two fans in parallel using low cost NPN transistors. Figure 39 shows the equivalent circuit using a MOSFET.

Because the MOSFET can handle up to 3.5 A, users can connect another fan directly in parallel with the first. Care should be taken in designing drive circuits with transistors and FETs to ensure that the PWM outputs are not required to source current, and that they sink less than the 5 mA maximum current specified on the data sheet.

Driving up to Three Fans from PWM3

TACH measurements for fans are synchronized to particular PWM channels; for example, TACH1 is synchronized to PWM1. TACH3 and TACH4 are both synchronized to PWM3, so PWM3 can drive two fans. Alternatively, PWM3 can be programmed to synchronize TACH2, TACH3, and TACH4 to the PWM3 output. This allows PWM3 to drive two or three fans. In this case, the drive circuitry looks the same, as shown in Figure 38 and Figure 39. The SYNC bit in Register 0x62 enables this function.

Synchronization is not required in high frequency mode when used with 4-wire fans.

Table 34. SYNC: ENHANCE ACOUSTICS REGISTER 1 (REG. 0x62)

Bit	Mnemonic	Description
[4]	SYNC	1, Synchronizes TACH2, TACH3, and TACH4 to PWM3.

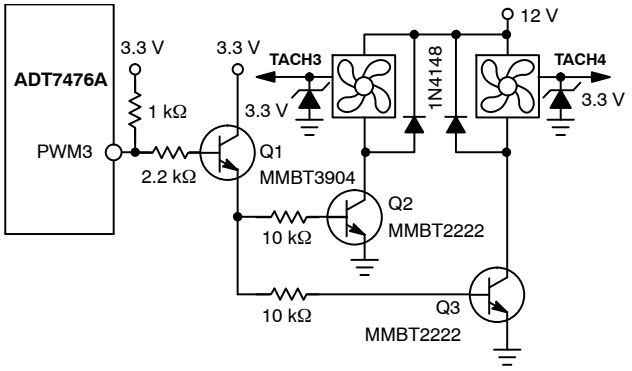


Figure 38. Interfacing Two Fans in Parallel to the PWM3 Output Using Low Cost NPN Transistors

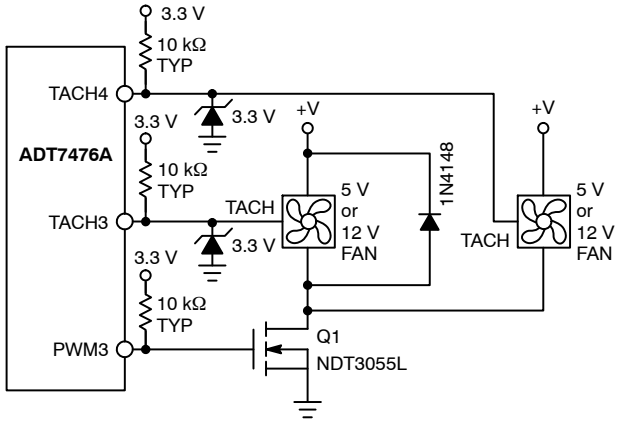


Figure 39. Interfacing Two Fans in Parallel to the PWM3 Output Using a Single N-channel MOSFET

Laying Out 3-Wire Fans

Figure 40 shows how to lay out a common circuit arrangement for 3-wire fans.

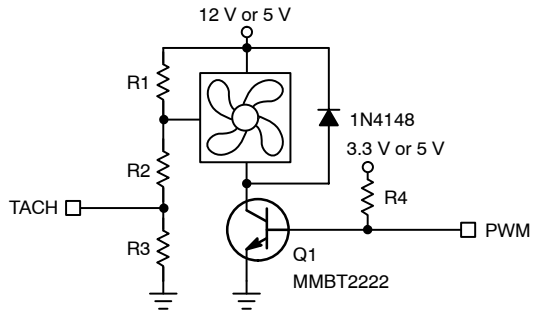


Figure 40. Planning for 3-wire Fans on a PCB

TACH Inputs

Pin 9, Pin 11, Pin 12, and Pin 14 (when configured as TACH inputs) are high impedance inputs intended for fan speed measurement.

Signal conditioning in the ADT7476A accommodates the slow rise and fall times typical of fan tachometer outputs. The maximum input signal range is 0 V to 5.5 V, even though V_{CC} is 3.3 V. In the event that these inputs are supplied from fan outputs that exceed 0 V to 5.5 V, either resistive attenuation of the fan signal or diode clamping must be included to keep inputs within an acceptable range.

Figure 41 to Figure 44 show circuits for most common fan TACH outputs.

If the fan TACH output has a resistive pullup to V_{CC}, it can be connected directly to the fan input, as shown in Figure 41.

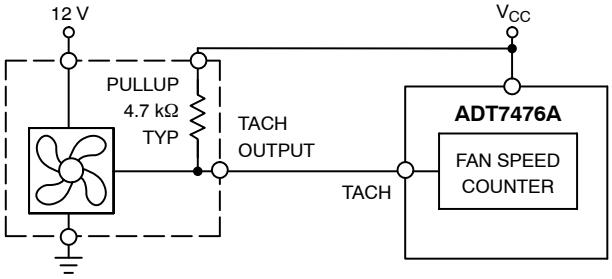


Figure 41. Fan with TACH Pullup to V_{CC}

If the fan output has a resistive pullup to 12 V, or other voltage greater than 5.5 V, the fan output can be clamped with a Zener diode, as shown in Figure 42. The Zener diode voltage should be chosen so that it is greater than V_{IH} of the TACH input but less than 5.5 V, allowing for the voltage tolerance of the Zener. A value between 5.0 V and 5.5 V is suitable.

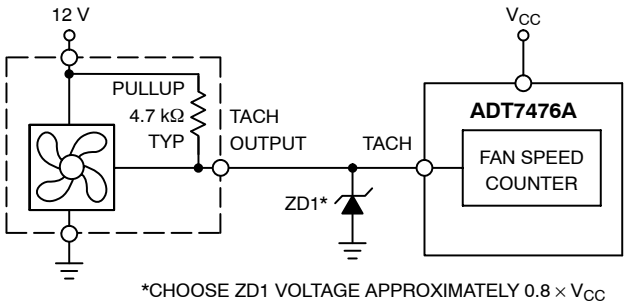


Figure 42. Fan with Strong TACH Pullup to > 5.5 V, (for Example, 12 V) Clamped with Zener Diode

If the fan has a strong pullup (less than 1 kΩ) to 12 V or a totem-pole output, a series resistor can be added to limit the Zener current, as shown in Figure 43.

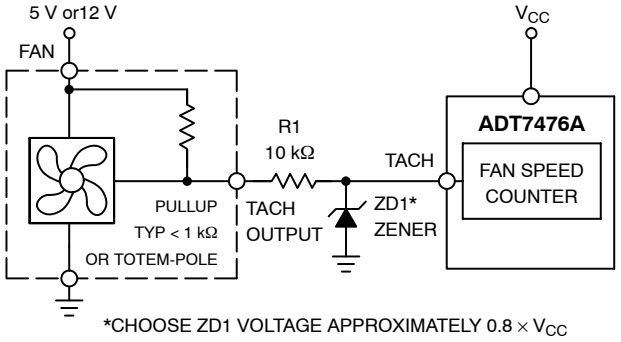


Figure 43. Fan with Strong TACH. Pullup to > V_{CC} or Totem-Pole Output, Clamped with Zener Diode and Resistor

Alternatively, a resistive attenuator can be used, as shown in Figure 44. R1 and R2 should be chosen such that:

$$2\ V < V_{PULLUP} \times R2/(R_{PULLUP} + R1 + R2) < 5.5\ V \quad \text{(eq. 4)}$$

The fan inputs have an input resistance of nominally 160 kΩ to ground, which should be taken into account when calculating resistor values.

With a pullup voltage of 12 V and pullup resistor less than 1 kΩ, suitable values for R1 and R2 are 100 kΩ and 40 kΩ, respectively. This gives a high input voltage of 3.42 V.

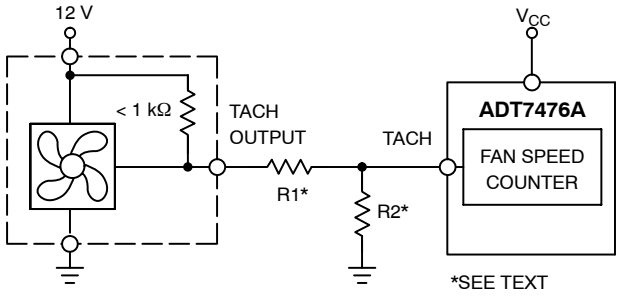


Figure 44. Fan with Strong TACH. Pullup to > V_{CC} or Totem-Pole Output, Attenuated with R1/R2

The fan counter does not count the fan TACH output pulses directly because the fan speed could be less than 1,000 RPM, and it takes several seconds to accumulate a reasonably large and accurate count. Instead, the period of the fan revolution is measured by gating an on-chip 90 kHz oscillator into the input of a 16-bit counter for *N* periods of the fan TACH output (Figure 45), so the accumulated count is actually proportional to the fan tachometer period and inversely proportional to the fan speed.

N, the number of pulses counted, is determined by the settings of TACH pulses per revolution register (0x7B). This register contains two bits for each fan, allowing one, two (default), three, or four TACH pulses to be counted.

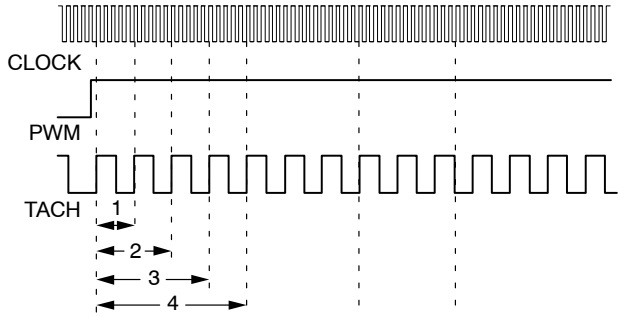


Figure 45. Fan Speed Measurement

Fan TachometerReading Registers

The fan tachometer readings are 16-bit values consisting of a 2-byte read from the ADT7476A.

Table 35. FAN TACHOMETER READING REGISTERS

Register	Description	Default
0x28	TACH1 Low Byte	0x00
0x29	TACH1 High Byte	0x00
0x2A	TACH2 Low Byte	0x00
0x2B	TACH2 High Byte	0x00
0x2C	TACH3 Low Byte	0x00
0x2D	TACH3 High Byte	0x00
0x2E	TACH4 Low Byte	0x00
0x2F	TACH4 High Byte	0x00

Reading Fan Speed from the ADT7476A

The measurement of fan speeds involves a 2-register read for each measurement. The low byte should be read first. This causes the high byte to be frozen until both high and low byte registers have been read, preventing erroneous TACH readings. The fan tachometer reading registers report back the number of 11.11 μs period clocks (90 kHz oscillator) gated to the fan speed counter from the rising edge of the first fan TACH pulse to the rising edge of the third fan TACH pulse (assuming two pulses per revolution are being counted).

Because the device is essentially measuring the fan TACH period, the higher the count value, the slower the fan is actually running. A 16-bit fan tachometer reading of 0xFFFF indicates that either the fan has stalled or is running very slowly (<100 RPM).

High Limit: > Comparison Performed

Because the actual fan TACH period is being measured, falling below a fan TACH limit by 1 sets the appropriate status bit and can be used to generate an $\overline{\text{SMBALERT}}$.

Measuring fan TACH has the following caveat: When the ADT7476A starts up, TACH measurements are locked. In effect, an internal read of the low byte has been made for each TACH input. The net result of this is that all TACH readings are locked until the high byte is read from the corresponding TACH registers. All TACH-related interrupts are also ignored until the appropriate high byte is read.

Once the corresponding high byte has been read, TACH measurements are unlocked and interrupts are processed as normal.

Fan TACH Limit Registers

The fan TACH limit registers are 16-bit values consisting of two bytes.

Table 36. FAN TACH LIMIT REGISTERS

Register	Description	Default
0x54	TACH1 Minimum Low Byte	0xFF
0x55	TACH1 Minimum High Byte	0xFF
0x56	TACH2 Minimum Low Byte	0xFF
0x57	TACH2 Minimum High Byte	0xFF
0x58	TACH3 Minimum Low Byte	0xFF
0x59	TACH3 Minimum High Byte	0xFF
0x5A	TACH4 Minimum Low Byte	0xFF
0x5B	TACH4 Minimum High Byte	0xFF

Fan Speed Measurement Rate

The fan TACH readings are normally updated once every second.

When set, the FAST bit (Bit 3) of Configuration Register 3 (0x78) updates the fan TACH readings every 250 ms.

DC Bits

If any of the fans are not being driven by a PWM channel but are powered directly from 5.0 V or 12 V, their associated dc bit in Configuration Register 3 should be set. This allows TACH readings to be taken on a continuous basis for fans connected directly to a dc source. Once high frequency mode is enabled in 4-wire fans, the dc bits do not need to be set because this is automatically done internally.

Calculating Fan Speed

Assuming a fan with two pulses per revolution, and with the ADT7476A programmed to measure two pulses per revolution, fan speed is calculated by:

$$\text{Fan Speed (RPM)} = (90{,}000 \times 60)/\text{Fan TACH Reading}$$

where Fan TACH Reading is the 16-bit fan tachometer reading.

Example:

TACH1 High Byte (0x29) = 0x17
TACH1 Low Byte (0x28) = 0xFF

What is Fan 1 speed in RPM?

Fan 1 TACH Reading = 0x17FF = 6143 (decimal)
RPM = (f × 60)/Fan 1 TACH Reading
RPM = (90,000 × 60)/6143
Fan Speed = 879 RPM

TACH Pulses per Revolution

Different fan models can output either one, two, three, or four TACH pulses per revolution. Once the number of fan TACH pulses has been determined, it can be programmed into the TACH Pulses per Revolution Register (0x7B) for each fan. Alternatively, this register can be used to determine the number of pulses per revolution output by a given fan. By plotting fan speed measurements at 100% speed with different pulses per revolution settings, the smoothest graph with the lowest ripple determines the correct pulses per revolution value.

Table 37. FAN PULSES PER REVOLUTION REGISTER (REG. 0x7B)

Bit	Mnemonic	Description
[1:0]	FAN1 Default	2 Pulses per Revolution
[3:2]	FAN2 Default	2 Pulses per Revolution
[5:4]	FAN3 Default	2 Pulses per Revolution
[7:6]	FAN4 Default	2 Pulses per Revolution

Table 38. FAN PULSES PER REVOLUTION REGISTER BIT VALUES

Value	Description
00	1 Pulse per Revolution
01	2 Pulses per Revolution
10	3 Pulses per Revolution
11	4 Pulses per Revolution

Fan Spin-up

The ADT7476A has a unique fan spin-up function. It spins the fan at 100% PWM duty cycle until two TACH pulses are detected on the TACH input. Once two TACH pulses have been detected, the PWM duty cycle goes to the expected running value, for example, 33%. Fans have different spin-up characteristics and take different times to overcome inertia. The advantage of the ADT7476A is that it runs the fans just fast enough to overcome inertia and is quieter on spin-up than fans that are programmed to spin up for a given time.

Fan Startup Timeout

To prevent the generation of false interrupts as a fan spins up (because it is below running speed), the ADT7476A includes a fan startup timeout function. During this time, the ADT7476A looks for two TACH pulses. If two TACH pulses are not detected, an interrupt is generated.

Fan startup timeout can be disabled by setting Bit 5 (FSPDIS) of Configuration Register 1 (0x40).

Table 39. PWM1 TO PWM3 CONFIGURATION (REG. 0x5C TO 0x5E)

Bit	Mnemonic	Description
[2:0]	SPIN	These Bits Control the Startup Timeout for PWM1 (0x5C), PWM2 (0x5D), PWM3 (0x5E). 000 = No Startup Timeout 001 = 100 ms 010 = 250 ms (Default) 011 = 400 ms 100 = 667 ms 101 = 1 s 110 = 2 s 111 = 4 s

Disabling Fan Startup Timeout

Although fan startup makes fan spin-ups much quieter than fixed-time spin-ups, the option exists to use fixed spin-up times. Setting Bit 5 (FSPDIS) to 1 in Configuration Register 1 (0x40) disables the spin-up for two TACH pulses. Instead, the fan spins up for the fixed time as selected in Register 0x5C to Register 0x5E.

PWM Logic State

The PWM outputs can be programmed high for 100% duty cycle (non-inverted) or low for 100% duty cycle (inverted).

Table 40. PWM1 TO PWM3 CONFIGURATION (REG. 0x5C TO 0x5E) BITS

Bit	Mnemonic	Description
[4]	INV	0 = Logic High for 100% PWM Duty Cycle 1 = Logic Low for 100% PWM Duty Cycle

Low Frequency Mode PWM Drive Frequency

The PWM drive frequency can be adjusted for the application. Register 0x5F to Register 0x61 configure the PWM frequency for PWM1 to PWM3, respectively.

Table 41. PWM FREQUENCY REGISTERS (REG. 0x5F TO 0x61)

Bit	Mnemonic	Description
[2:0]	FREQ	000 = 11.0 Hz 001 = 14.7 Hz 010 = 22.1 Hz 011 = 29.4 Hz 100 = 35.3 Hz (Default) 101 = 44.1 Hz 110 = 58.8 Hz 111 = 88.2 Hz

High Frequency Mode PWM Drive

Setting Bit 3 of Register 0x5F, Register 0x60, and Register 0x61 enables high frequency mode for Fan 1, Fan 2, and Fan 3 respectively.

In high frequency mode, the PWM drive frequency is always 22.5 kHz. When high frequency mode is enabled, the dc bits are automatically asserted internally and do not need to be changed.

Fan Speed Control

The ADT7476A controls fan speed using automatic and manual modes:

- In automatic fan speed control mode, fan speed is automatically varied with temperature and without CPU intervention once initial parameters are set up. The advantage is that if the system hangs, the user is guaranteed that the system is protected from overheating.
- In manual fan speed control mode, the ADT7476A allows the duty cycle of any PWM output to be adjusted manually. This can be useful if the user wants to change fan speed in software or adjust PWM duty cycle output for test purposes. Bits [7:5] of Register 0x5C to Register 0x5E (PWM Configuration) control the behavior of each PWM output.

Table 42. PWM CONFIGURATION REGISTERS (REG. 0x5C TO 0x5E)

Bit	Mnemonic	Description
[7:5]	BHVR	111 = Manual Mode

Once under manual control, each PWM output can be manually updated by writing to Register 0x30 to Register 0x32 (PWM current duty cycle registers).

Programming the PWM Current Duty Cycle Registers

The PWM current duty cycle registers are 8-bit registers that allow the PWM duty cycle for each output to be set anywhere from 0% to 100% in steps of 0.39%. The value to be programmed into the PWM_{MIN} register is given by:

Value (decimal) = $PWM_{MIN}/0.39$

Example 1:

For a PWM duty cycle of 50%,
Value (decimal) = 50/0.39 = 128 (decimal)
Value = 128 (decimal) or 0x80 (hex)

Example 2:

For a PWM duty cycle of 33%,
Value (decimal) = 33/0.39 = 85 (decimal)
Value = 85 (decimal) or 0x54 (hex)

Table 43. PWM CURRENT DUTY CYCLE REGISTERS

Register	Description	Default
0x30	PWM1 Current Duty Cycle	0xFF (100%)
0x31	PWM2 Current Duty Cycle	0xFF (100%)
0x32	PWM3 Current Duty Cycle	0xFF (100%)

By reading the PWMx current duty cycle registers, the user can keep track of the current duty cycle on each PWM output, even when the fans are running in automatic fan speed control mode or acoustic enhancement mode.

Programming T_{RANGE}

T_{RANGE} defines the distance between T_{MIN} and 100% PWM. For the ADT7467, ADT7468 and ADT7473, T_{RANGE} is effectively a slope. For the ADT7475 andADT7476A, T_{RANGE} is no longer a slope, but defines the temperature region where the PWM output linearly ramps from PWM_{MIN} to 100% PWM.

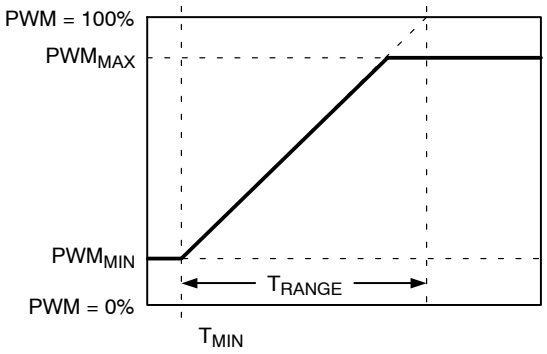


Figure 46. T_{RANGE}

Programming the Automatic Fan Speed Control Loop

To understand the automatic fan speed control loop more efficiently, it is recommended to use the ADT7476A evaluation board and software while reading this section.

This section provides the system designer with an understanding of the automatic fan control loop and provides step-by-step guidance on effectively evaluating and selecting critical system parameters. To optimize the system characteristics, the designer needs to give some thought to system configuration, including the number of fans, where they are located, and what temperatures are being measured in the particular system.

The mechanical or thermal engineer who is tasked with the system thermal characterization should also be involved at the beginning of the system development process.

Manual Fan Control Overview

In unusual circumstances, it can be necessary to manually control the speed of the fans. Because the ADT7476A has an SMBus interface, a system can read back all necessary voltage, fan speed, and temperature information, and use this information to control the speed of the fans by writing to the PWM current duty cycle register (0x30, 0x31, and 0x32) of the appropriate fan. Bits [7:5] of the PWMx configuration registers (0x5C, 0x5D, 0x5E) are used to set fans up for manual control.

$\overline{\text{THERM}}$ Operation in Manual Mode

In manual mode, if the temperature increases above the programmed $\overline{\text{THERM}}$ temperature limit, the fans automatically speed up to maximum PWM or 100% PWM, whichever way the appropriate fan channel is configured.

Automatic Fan Control Overview

The ADT7476A can automatically control the speed of fans based on the measured temperature. This is done independently of CPU intervention once initial parameters are set up.

The ADT7476A has a local temperature sensor and two remote temperature channels that can be connected to a CPU on-chip thermal diode (available on Intel Pentium class and other CPUs). These three temperature channels can be used as the basis for automatic fan speed control to drive fans using pulse-width modulation (PWM).

Automatic fan speed control reduces acoustic noise by optimizing fan speed according to accurately measured temperature. Reducing fan speed can also decrease system current consumption. The automatic fan speed control mode is very flexible due to the number of programmable parameters, including T_{MIN} and T_{RANGE}. The T_{MIN} and T_{RANGE} values for a temperature channel and, therefore, for a given fan, are critical, because they define the thermal characteristics of the system. The thermal validation of the system is one of the most important steps in the design process, so these values should be selected carefully.

Figure 47 gives a top-level overview of the automatic fan control circuitry on the ADT7476A. From a systems-level perspective, up to three system temperatures can be monitored and used to control three PWM outputs. The three PWM outputs can be used to control up to four fans. The ADT7476A allows the speed of four fans to be monitored. Each temperature channel has a thermal calibration block, allowing the designer to individually configure the thermal characteristics of each temperature channel. For example, designers can decide to run the CPU fan when CPU temperature increases above 60°C and a chassis fan when the local temperature increases above 45°C.

At this stage, the designer has not assigned these thermal calibration settings to a particular fan drive (PWM) channel. The right side of Figure 47 shows fan-specific controls. The designer has individual control over parameters such as minimum PWM duty cycle, fan speed failure thresholds, and even ramp control of the PWM outputs. Automatic fan control, then, ultimately allows graceful fan speed changes that are less perceptible to the system user.

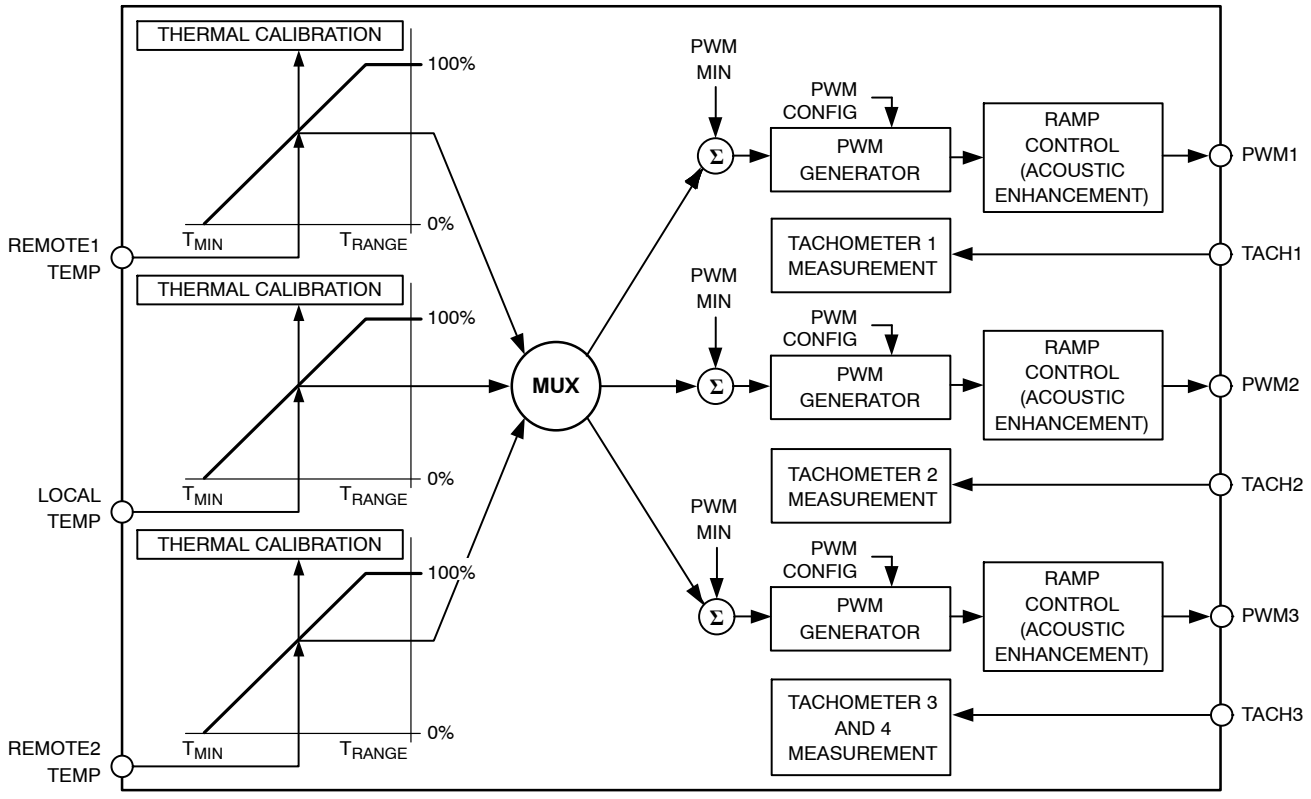


Figure 47. Automatic Fan Control Block Diagram

Step 1 – Hardware Configuration

During system design, the motherboard sensing and control capabilities should be addressed early in the design stages. Decisions about how these capabilities are used should involve the system thermal/mechanical engineer. Ask the following questions:

1. What ADT7476A functionality is used?
   - PWM2 or $\overline{\text{SMBALERT}}$?
   - TACH4 fan speed measurement or overtemperature $\overline{\text{THERM}}$ function?
   - 2.5 V voltage monitoring or overtemperature $\overline{\text{THERM}}$ function?
   - 12 V voltage monitoring or VID5 input?

   The ADT7476A offers multifunctional pins that can be reconfigured to suit different system requirements and physical layouts. These multifunction pins are software programmable.
2. How many fans are supported in system, three or four?
   This influences the choice of whether to use the TACH4 pin or to reconfigure it for the $\overline{\text{THERM}}$ function.
3. Is the CPU fan to be controlled using the ADT7476A, or will the CPU fan run at full speed 100% of the time?
   If run at 100%, this frees up a PWM output, but the system is louder.
4. Where will the ADT7476A be physically located in the system?
   This influences the assignment of the temperature measurement channels to particular system thermal zones. For example, locating the ADT7476A close to the VRM controller circuitry allows the VRM temperature to be monitored using the local temperature channel.

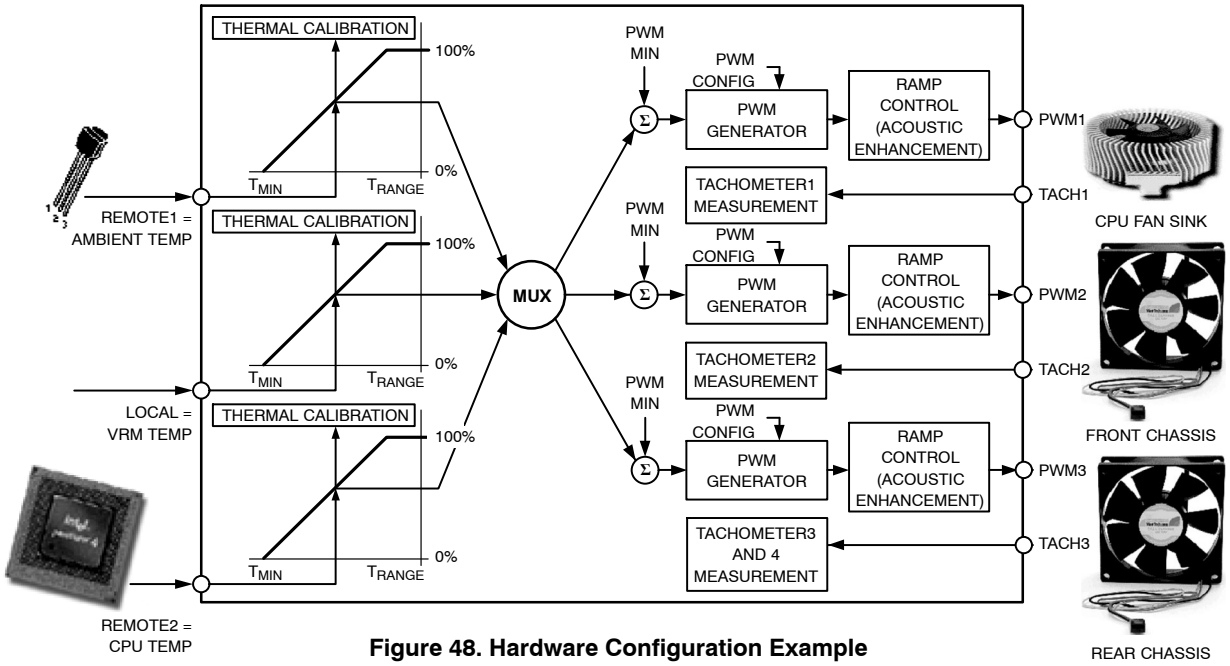


Figure 48. Hardware Configuration Example

Recommended Implementation 1

Configuring the ADT7476A as shown in Figure 49 provides the system designer with the following features:

- Six VID inputs (VID0, VID1, VID2, VID3, VID4, and VID6) for VRM10 support.
- Two PWM outputs for fan control of up to three fans. The front and rear chassis fans are connected in parallel.
- Three TACH fan speed measurement inputs.
- V_{CC} measured internally through Pin 4.
- CPU core voltage measurement (V_{CORE}).
- 2.5 V measurement input used to monitor CPU current (connected to V_{COMP} output of ADP316x VRM controller). This is used to determine CPU power consumption.
- 5.0 V measurement input.
- VRM temperature using local temperature sensor.
- CPU temperature measured using the Remote 1 temperature channel.
- Ambient temperature measured through the Remote 2 temperature channel.
- If not using VID5, it can be reconfigured as the 12 V monitoring input.
- Bidirectional $\overline{\text{THERM}}$ pin allows the monitoring of $\overline{\text{PROCHOT}}$ output from an Intel P4 processor, for example, or can be used as an overtemperature $\overline{\text{THERM}}$ output.
- $\overline{\text{SMBALERT}}$ system interrupt output.

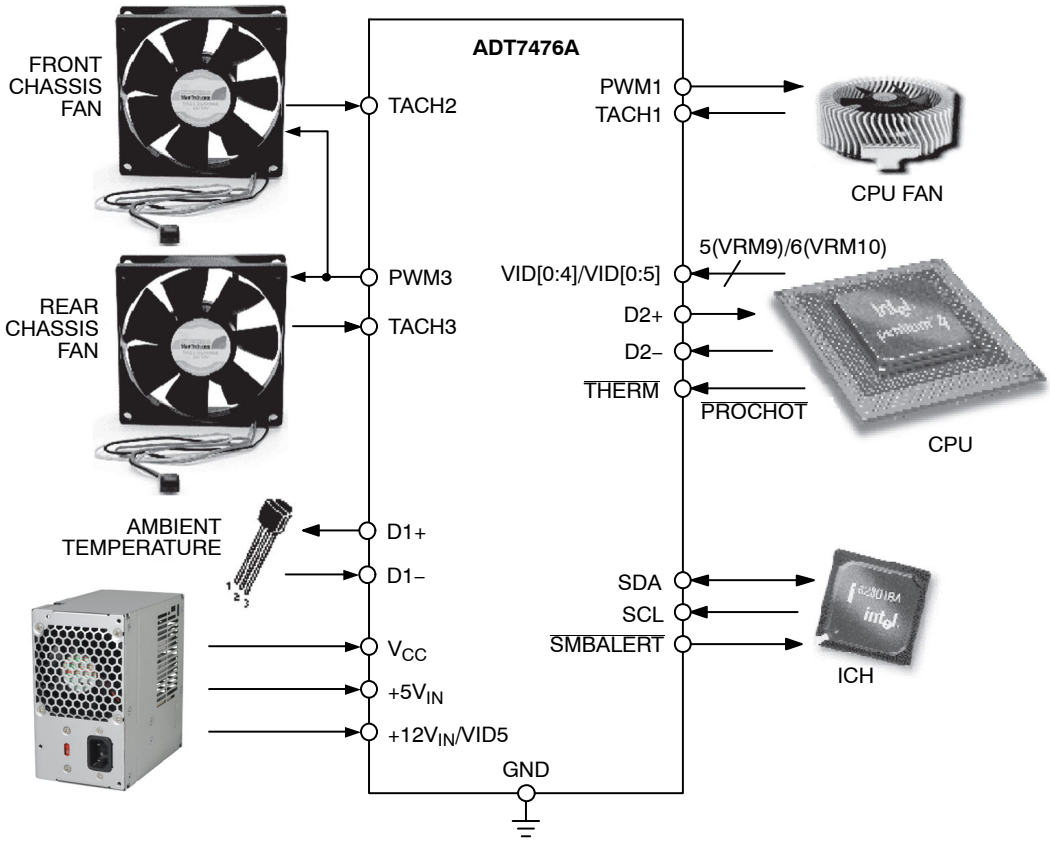


Figure 49. Recommended Implementation 1

Recommended Implementation 2

Configuring the ADT7476A as shown in Figure 50 provides the system designer with the following features:

- Six VID inputs (VID0, VID1, VID2, VID3, VID4, and VID6) for VRM10 support.
- Three PWM outputs for fan control of up to three fans. All three fans can be individually controlled.
- Three TACH fan speed measurement inputs.
- V_{CC} measured internally through Pin 4.
- CPU core voltage measurement (V_{CORE}).
- 2.5 V measurement input used to monitor CPU current (connected to V_{COMP} output of ADP316x VRM controller). This is used to determine CPU power consumption.
- 5.0 V measurement input.
- VRM temperature using local temperature sensor.
- CPU temperature measured using the Remote 1 temperature channel.
- Ambient temperature measured through the Remote 2 temperature channel.
- If not using VID5, it can be reconfigured as the 12 V monitoring input.
- Bidirectional $\overline{\text{THERM}}$ pin allows the monitoring of $\overline{\text{PROCHOT}}$ output/input from an Intel P4 processor, for example, or can be used as an overtemperature $\overline{\text{THERM}}$ output.

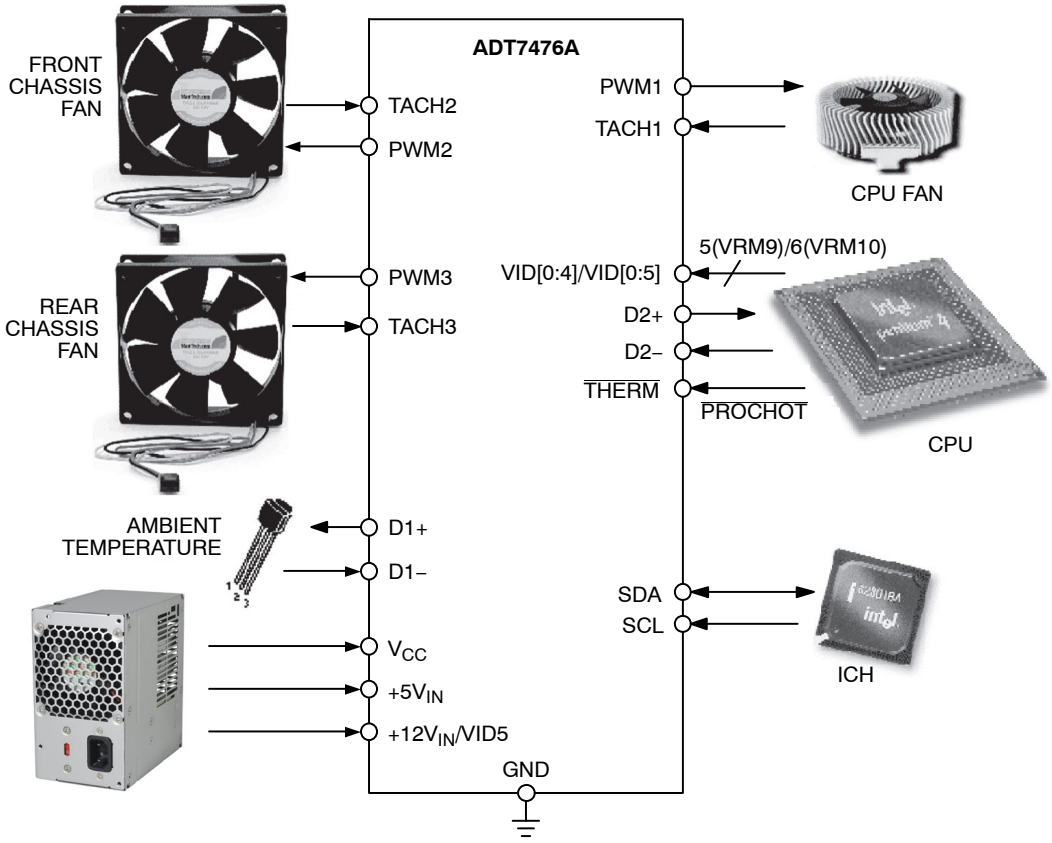


Figure 50. Recommended Implementation 2

Step 2 – Configuring the Mux

After the system hardware configuration is determined, the fans can be assigned to particular temperature channels. Not only can fans be assigned to individual channels, but the behavior of the fans is also configurable. For example, fans can be run under automatic fan control, manually (under software control), or at the fastest speed calculated by multiple temperature channels. The mux is the bridge between temperature measurement channels and the three PWM outputs.

Bits [7:5] (BHVR) of Register 0x5C, Register 0x5D, and Register 0x5E (PWM configuration registers) control the behavior of the fans connected to the PWM1, PWM2, and PWM3 outputs. The values selected for these bits determine how the mux connects a temperature measurement channel to a PWM output.

Automatic Fan Control Mux Options

[7:5] (BHVR), Register 0x5C, Register 0x5D, Register 0x5E.

000 = Remote 1 temperature controls PWMx
001 = Local temperature controls PWMx
010 = Remote 2 temperature controls PWMx
101 = Fastest speed calculated by local and Remote 2 temperature controls PWMx
110 = Fastest speed calculated by all three temperature channels controls PWMx

The fastest speed calculated options pertain to controlling one PWM output based on multiple temperature channels. The thermal characteristics of the three temperature zones can be set to drive a single fan. An example would be the fan turning on when Remote 1 temperature exceeds 60°C or if the local temperature exceeds 45°C.

Other Mux Options

[7:5] (BHVR), Register 0x5C, Register 0x5D, Register 0x5E.

011 = PWMx runs full speed
100 = PWMx disabled (default)
111 = Manual mode. PWMx is running under software control. In this mode, PWM current duty cycle registers (0x30 to 0x32) are writable and control the PWM outputs.

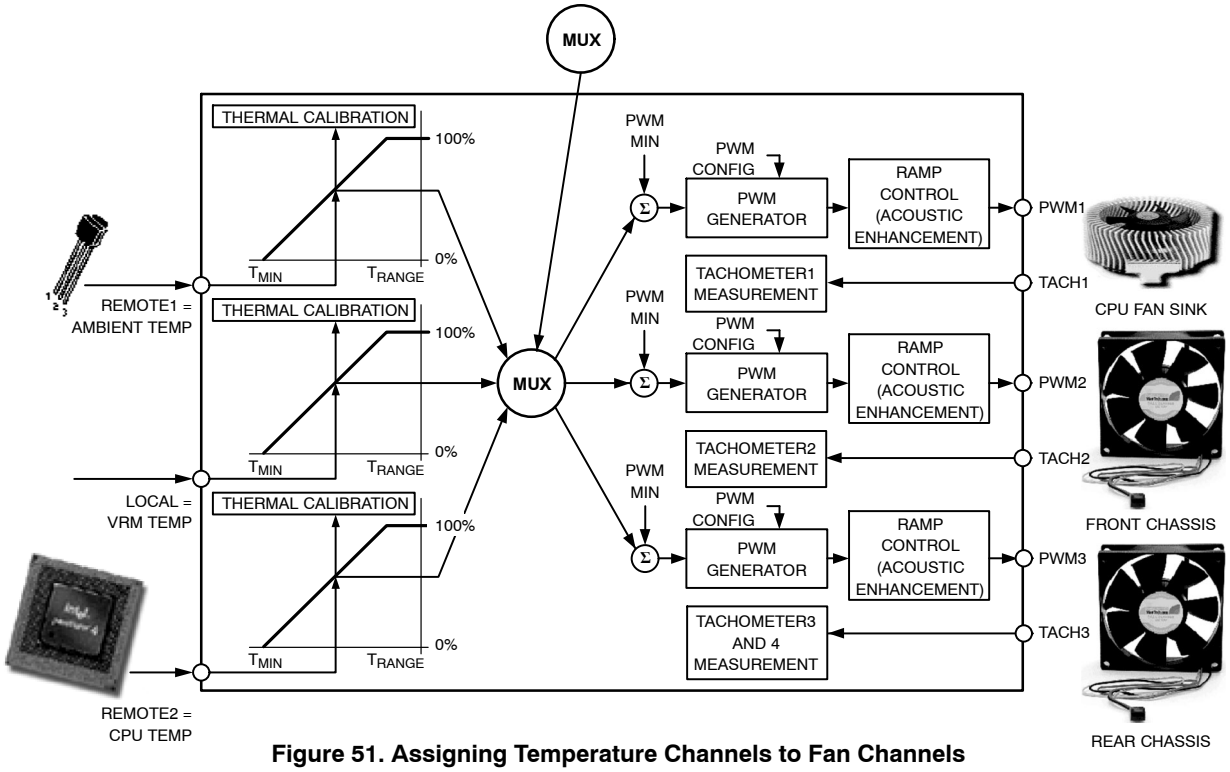


Figure 51. Assigning Temperature Channels to Fan Channels

Mux Configuration Example

This is an example of how to configure the mux in a system using the ADT7476A to control three fans. The CPU fan sink is controlled by PWM1, the front chassis fan is controlled by PWM2, and the rear chassis fan is controlled by PWM3. The mux is configured for the following fan control behavior:

- PWM1 (CPU fan sink) is controlled by the fastest speed calculated by the local (VRM temperature) and Remote 2 (processor) temperature. In this case, the CPU fan sink is also being used to cool the VRM.
- PWM2 (front chassis fan) is controlled by the Remote 1 temperature (ambient).
- PWM3 (rear chassis fan) is controlled by the Remote 1 temperature (ambient).

Example Mux Settings

[7:5] (BHVR), PWM1 Configuration Register (0x5C).
101 = Fastest speed calculated by local and Remote 2 temperature controls PWM1

[7:5] (BHVR), PWM2 Configuration Register (0x5D).
000 = Remote 1 temperature controls PWM2

[7:5] (BHVR), PWM3 Configuration Register (0x5E).
000 = Remote 1 temperature controls PWM3

These settings configure the mux, as shown in Figure 52.

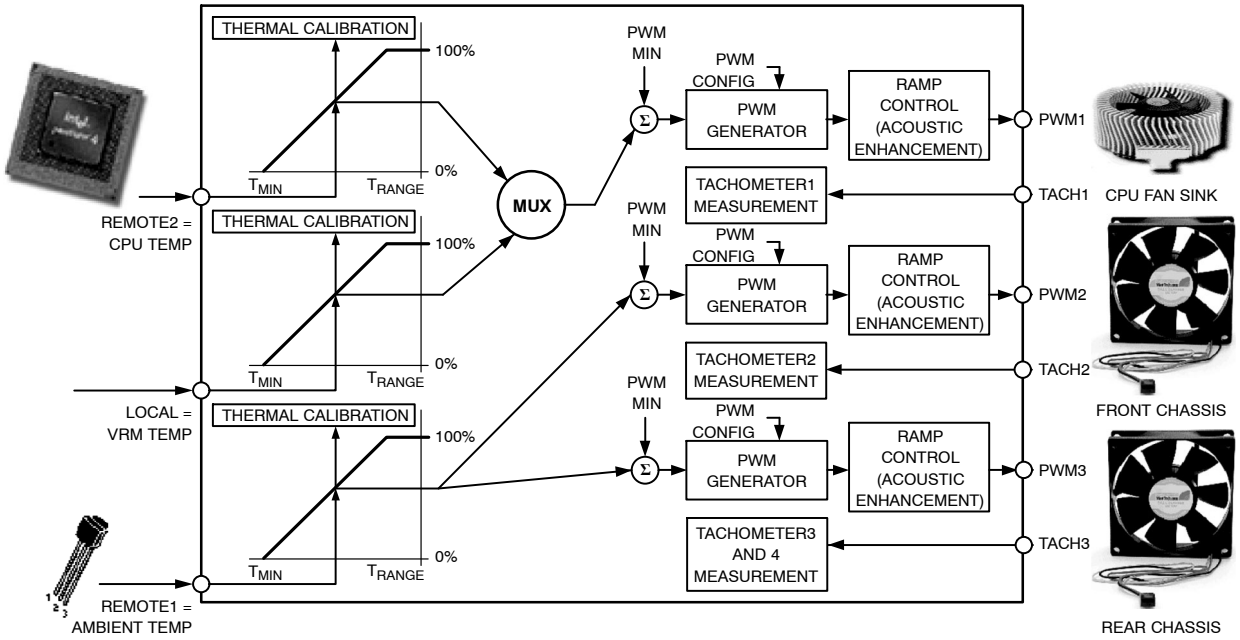


Figure 52. Mux Configuration Example

Step 3 – T_{MIN} Settings for Thermal Calibration Channels

T_{MIN} is the temperature at which the fans start to turn on under automatic fan control. The speed at which the fan runs at T_{MIN} is programmed later. The T_{MIN} values chosen are temperature channel specific, for example, 25°C for ambient channel, 30°C for VRM temperature, and 40°C for processor temperature.

T_{MIN} is an 8-bit value, either twos complement or Offset 64, which can be programmed in 1°C increments. A T_{MIN} register is associated with each temperature measurement channel: Remote 1, local, and Remote 2 temperature. Once the T_{MIN} value is exceeded, the fan turns on and runs at the minimum PWM duty cycle. The fan turns off once the temperature has dropped below $T_{MIN} - T_{HYST}$.

To overcome fan inertia, the fan is spun up until two valid TACH rising edges are counted. See the Fan Startup Timeout section for more details. In some cases, primarily for psycho-acoustic reasons, it is desirable that the fan never switch off below T_{MIN}. Setting Bits [7:5] of Enhance Acoustics Register 1 (0x62) keeps the fans running at the PWM minimum duty cycle if the temperature should fall below T_{MIN}.

Table 44. T_{MIN} REGISTERS

Register	Description	Default
0x67	Remote 1 Temperature T_{MIN}	0x5A (90°C)
0x68	Local Temperature T_{MIN}	0x5A (90°C)
0x69	Remote 2 Temperature T_{MIN}	0x5A (90°C)

Enhance Acoustics Register 1 (0x62)

Bit 7 (MIN3) = 0, PWM3 is off (0% PWM duty cycle) when temperature is below $T_{MIN} - T_{HYST}$.

Bit 7 (MIN3) = 1, PWM3 runs at PWM3 minimum duty cycle below $T_{MIN} - T_{HYST}$.

Bit 6 (MIN2) = 0, PWM2 is off (0% PWM duty cycle) when temperature is below $T_{MIN} - T_{HYST}$.

Bit 6 (MIN2) = 1, PWM2 runs at PWM2 minimum duty cycle below $T_{MIN} - T_{HYST}$.

Bit 5 (MIN1) = 0, PWM1 is off (0% PWM duty cycle) when temperature is below $T_{MIN} - T_{HYST}$.

Bit 5 (MIN1) = 1, PWM1 runs at PWM1 minimum duty cycle below $T_{MIN} - T_{HYST}$.

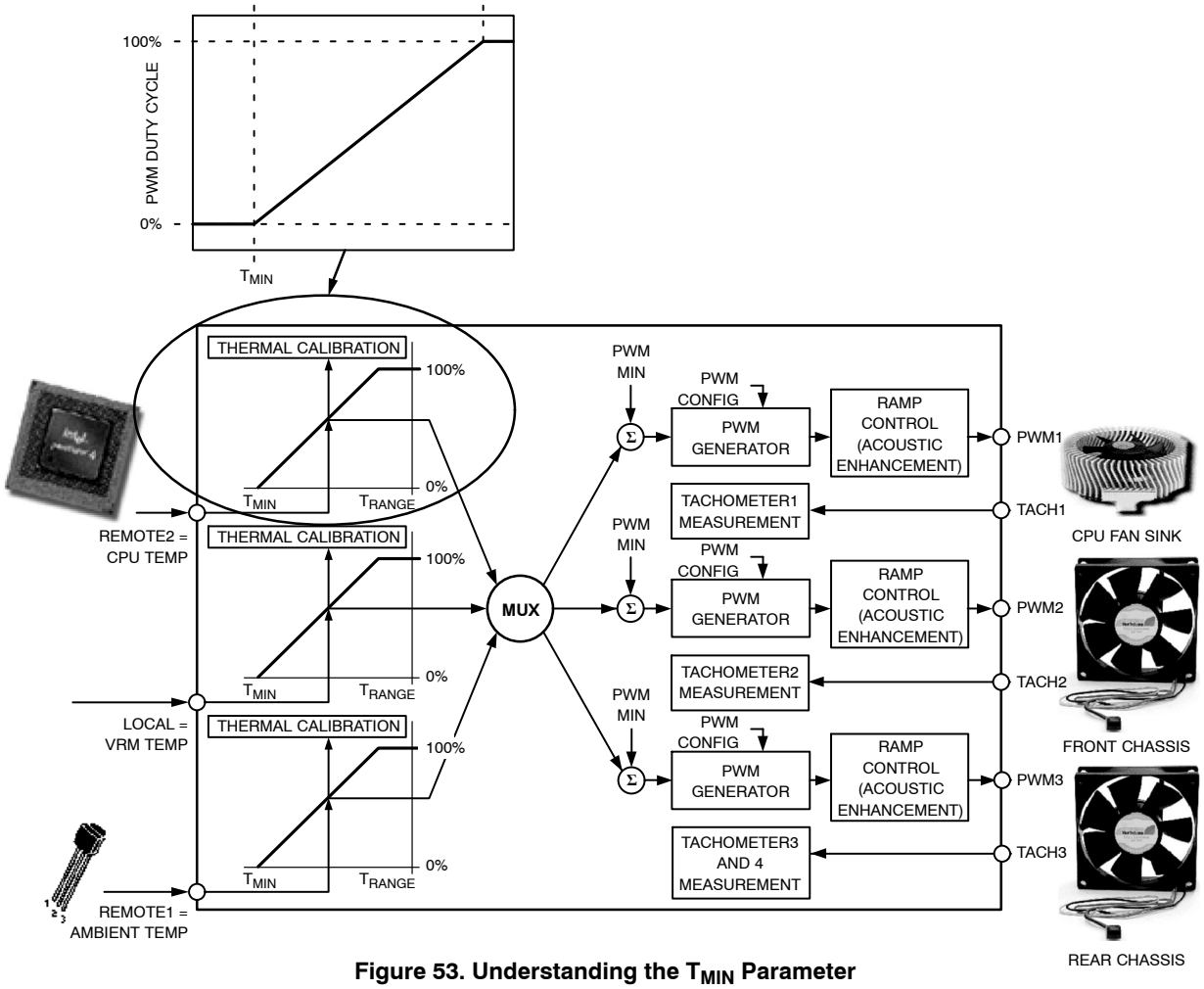


Figure 53. Understanding the T_{MIN} Parameter

Step 4 – PWM_{MIN} for Each PWM (Fan) Output

PWM_{MIN} is the minimum PWM duty cycle at which each fan in the system runs. It is also the start speed for each fan under automatic fan control once the temperature rises above T_{MIN}. For maximum system acoustic benefit, PWM_{MIN} should be as low as possible. Depending on the fan used, the PWM_{MIN} setting is usually in the 20% to 33% duty cycle range. This value can be found through fan validation.

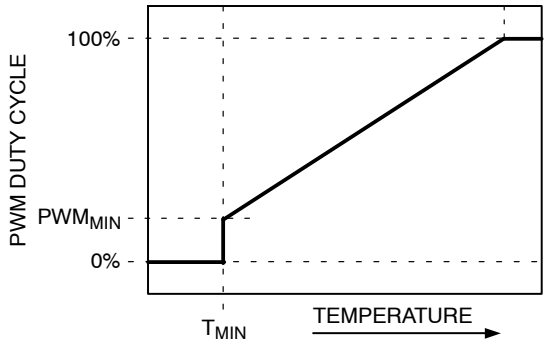


Figure 54. PWM_{MIN} Determines Minimum PWM Duty Cycle

More than one PWM output can be controlled from a single temperature measurement channel. For example, Remote 1 temperature can control PWM1 and PWM2 outputs. If two different fans are used on PWM1 and PWM2, the fan characteristics can be set up differently. As a result, Fan 1 driven by PWM1 can have a different PWM_{MIN} value than that of Fan 2 connected to PWM2. Figure 55 illustrates this as $PWM1_{MIN}$ (front fan), which is turned on at a minimum duty cycle of 20%, while $PWM2_{MIN}$ (rear fan) turns on at a minimum of 40% duty cycle.

NOTE: Both fans turn on at exactly the same temperature, defined by T_{MIN}.

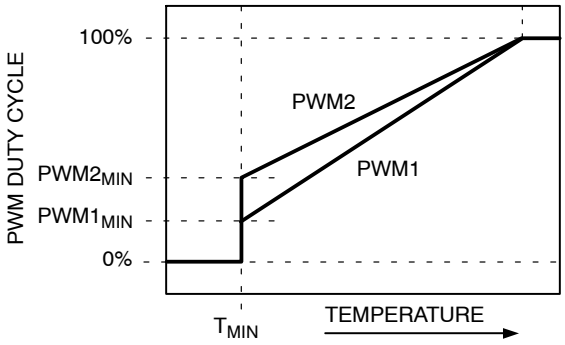


Figure 55. Operating Two Different Fans from a Single Temperature Channel

Programming the PWM Minimum Duty Cycle Registers

The PWM minimum duty cycle registers are 8-bit registers that allow the minimum PWM duty cycle for each output to be configured anywhere from 0% to 100%. This allows the minimum PWM duty cycle to be set in steps of 0.39%.

The value to be programmed into the PWM_{MIN} register is given by:

Value (decimal) = PWM_{MIN}/0.39

Example 1:

For a minimum PWM duty cycle of 50%,
Value (decimal) = 50/0.39 = 128 (decimal)
Value = 128 (decimal) or 80 (hex)

Example 2:

For a minimum PWM duty cycle of 33%,
Value (decimal) = 33/0.39 = 85 (decimal)
Value = 85 (decimal) l or 54 (hex)

Table 45. PWM MINIMUM DUTY CYCLE REGISTERS

Register	Description	Default
0x64	PWM1 Minimum Duty Cycle	0x80 (50%)
0x65	PWM2 Minimum Duty Cycle	0x80 (50%)
0x66	PWM3 Minimum Duty Cycle	0x80 (50%)

Note on Fan Speed and PWM Duty Cycle

The PWM duty cycle does not directly correlate to fan speed in RPM. Running a fan at 33% PWM duty cycle does not equate to running the fan at 33% speed. Driving a fan at 33% PWM duty cycle actually runs the fan at closer to 50% of its full speed. This is because fan speed in %RPM generally relates to the square root of PWM duty cycle. Given a PWM square wave as the drive signal, fan speed in RPM approximates to:

$$\%\ \text{fanspeed} = \sqrt{\text{PWM Duty Cycle} \times 10} \quad \text{(eq. 5)}$$

Step 5 – PWM_{MAX} for PWM (Fan) Outputs

PWM_{MAX} is the maximum duty cycle that each fan in the system runs at under the automatic fan speed control loop. For maximum system acoustic benefit, PWM_{MAX} should be as low as possible but should be capable of maintaining the processor temperature limit at an acceptable level. If the $\overline{\text{THERM}}$ temperature limit is exceeded, the fans are still boosted to 100% for fail-safe cooling.

There is a PWM_{MAX} limit for each fan channel. The default value of this register is 0xFF and has no effect unless it is programmed.

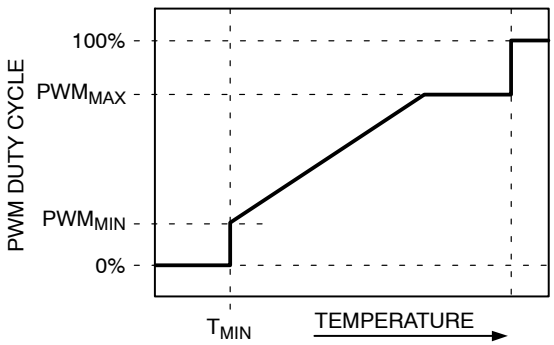


Figure 56. PWM_{MAX} Determines Maximum PWM Duty Cycle Below the $\overline{\text{THERM}}$ Temperature Limit

Programming the PWM Maximum Duty Cycle Registers

The PWM maximum duty cycle registers are 8-bit registers that allow the maximum PWM duty cycle for each output to be configured anywhere from 0% to 100%. This allows the maximum PWM duty cycle to be set in steps of 0.39%.

The value to be programmed into the PWM maximum duty cycle register is given by:

Value (decimal) = $PWM_{MAX}/0.39$

Example 1:

For a maximum PWM duty cycle of 50%,
Value (decimal) – 50/0.39 = 128 (decimal)
Value = 128 (decimal) or 80 (hex)

Example 2:

For a minimum PWM duty cycle of 75%,
Value (decimal) = 75/0.39 = 85 (decimal)
Value = 192 (decimal) or C0 (hex)

Table 46. PWM MAXIMUM DUTY CYCLE REGISTERS

Register	Description	Default
0x38	PWM1 Maximum Duty Cycle	0xFF (100%)
0x39	PWM2 Maximum Duty Cycle	0xFF (100%)
0x3A	PWM3 Maximum Duty Cycle	0xFF (100%)

Step 6 – T_{RANGE} for Temperature Channels

T_{RANGE} is the range of temperature over which automatic fan control occurs once the programmed T_{MIN} temperature has been exceeded. T_{RANGE} is the temperature range between PWM_{MIN} and 100% PWM where the fan speed changes linearly. Otherwise stated, it is the line drawn between the T_{MIN}/PWM_{MIN} and the $(T_{MIN} + T_{RANGE})/PWM100\%$ intersection points.

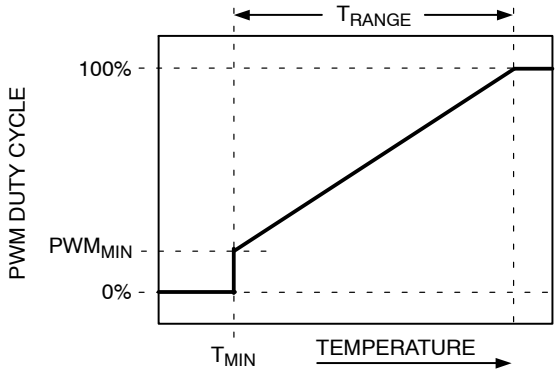


Figure 57. T_{RANGE} Parameter Affects Cooling Slope

The T_{RANGE} is determined by the following procedure:

1. Determine the maximum operating temperature for that channel (for example, 70°C).
2. Determine experimentally the fan speed (PWM duty cycle value) that does not exceed the temperature at the worst-case operating points. For example, 70°C is reached when the fans are running at 50% PWM duty cycle.
3. Determine the slope of the required control loop to meet these requirements.
4. Using the ADT7476A evaluation software, you can graphically program and visualize this functionality.

As PWM_{MIN} is changed, the automatic fan control slope changes.

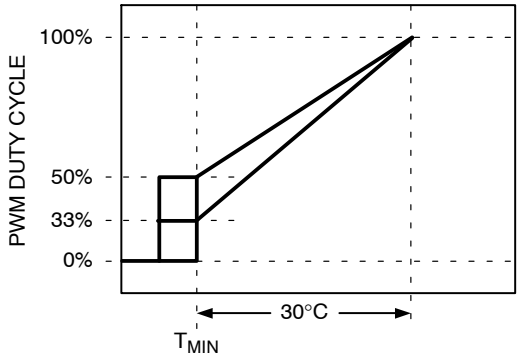


Figure 58. Adjusting PWM_{MIN} Changes the Automatic Fan Control Slope

As T_{RANGE} is changed, the slope changes. As T_{RANGE} gets smaller, the fans reach 100% speed with a smaller temperature change.

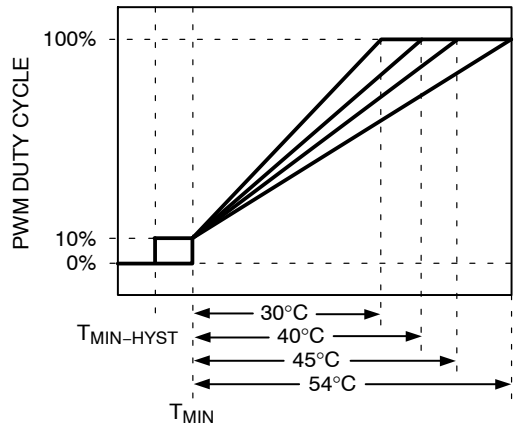


Figure 59. Increasing T_{RANGE} Changes the AFC Slope

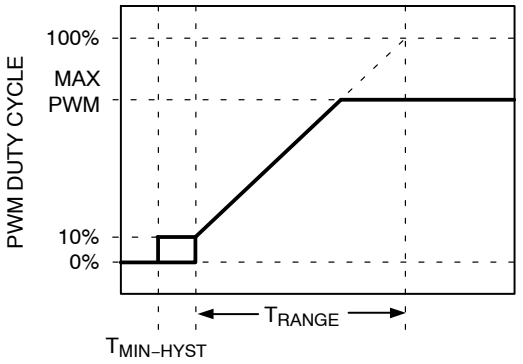


Figure 60. Changing PWM_{MAX} Does Not Change the AFC Slope

Selecting T_{RANGE}

The T_{RANGE} value can be selected for each temperature channel: Remote 1, Local, and Remote 2 temperature. Bits [7:4] (T_{RANGE}) of Register 0x5F to Register 0x61 define the T_{RANGE} value for each temperature channel.

Table 47. SELECTING A T_{RANGE} VALUE

Bits [7:4] (Note 1)	**T_{RANGE} (°C)**
0000	2
0001	2.5
0010	3.33
0011	4
0100	5
0101	6.67
0110	8
0111	10
1000	13.33
1001	16
1010	20
1011	26.67
1100	32 (Default)
1101	40
1110	53.33
1111	80

1. Register 0x5F configures Remote 1 T_{RANGE}; Register 0x60 configures Local T_{RANGE}; Register 0x61 configures Remote 2 T_{RANGE}.

Actual Changes in PWM Output (Advanced Acoustics Settings)

While the automatic fan control algorithm describes the general response of the PWM output, it is also necessary to note that the enhance acoustics registers (0x62 and 0x63) can be used to set/clamp the maximum rate of change of PWM output for a given temperature zone. This means that if T_{RANGE} is programmed with an AFC slope that is quite steep, a relatively small change in temperature could cause a large change in PWM output and possibly an audible change in fan speed, which can be noticeable/ bothersome to end users.

Decreasing the speed the PWM output changes by programming the smoothing on the appropriate temperature channels (Register 0x62 and Register 0x63) changes how fast the fan speed increases/decreases in the event of a temperature spike. The PWM duty cycle increases slowly until the PWM duty cycle reaches the appropriate duty cycle as defined by the AFC curve.

Figure 61 shows PWM duty cycle vs. temperature for each T_{RANGE} setting. The lower graph shows how each T_{RANGE} setting affects fan speed vs. temperature. As can be seen from the graph, the effect on fan speed is nonlinear.

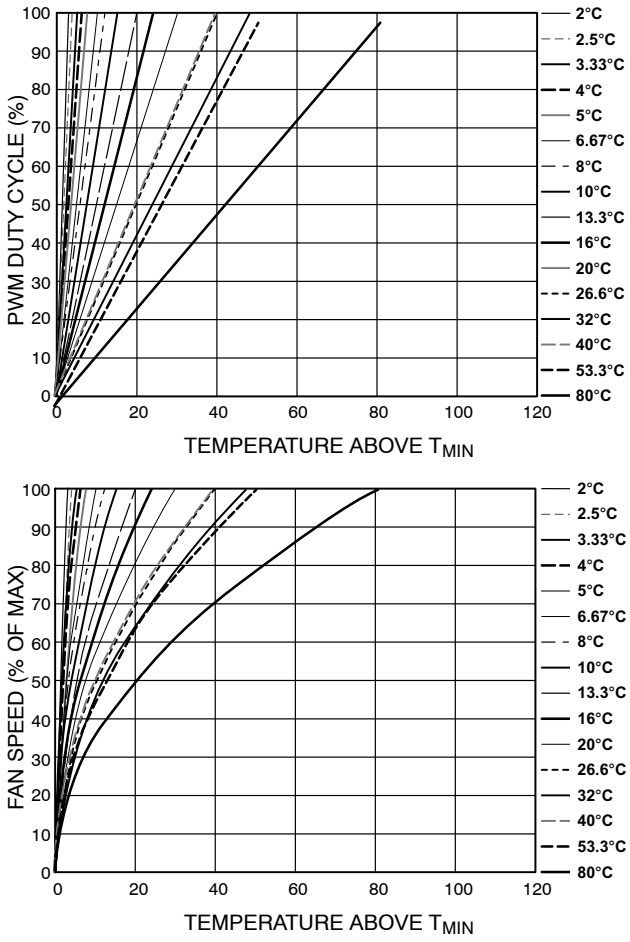


Figure 61. T_{RANGE} vs. Actual Fan Speed (Not PWM Drive) Profile

The graphs in Figure 61 assume that the fan starts from 0% PWM duty cycle. Clearly, the minimum PWM duty cycle, PWM_{MIN}, needs to be factored in to see how the loop actually performs in the system. Figure 62 shows how T_{RANGE} is affected when the PWM_{MIN} value is set to 20%. It can be seen that the fan actually runs at about 45% fan speed when the temperature exceeds T_{MIN}.

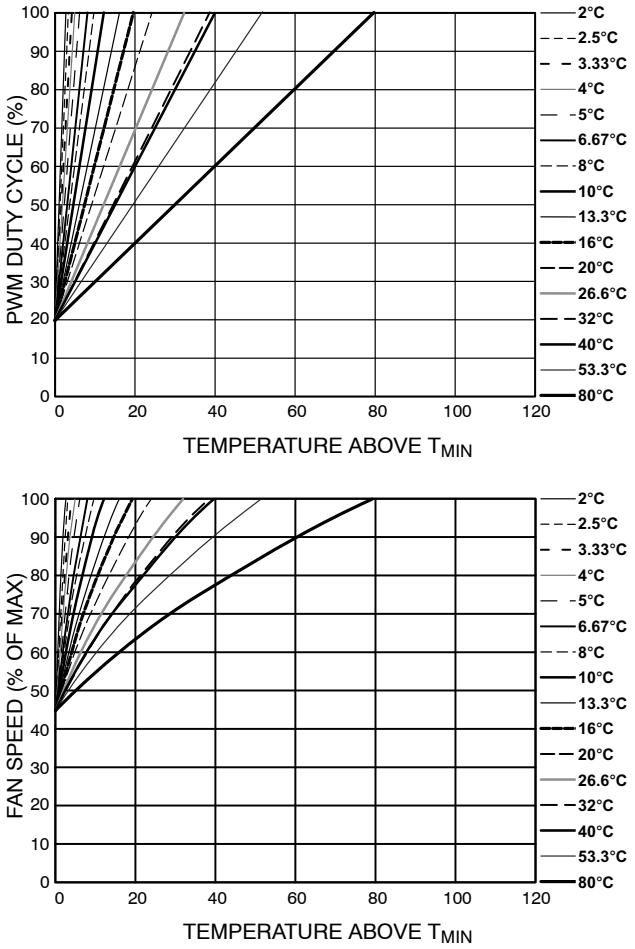


Figure 62. T_{RANGE} and % Fan Speed Slopes with PWM_{MIN} = 20%

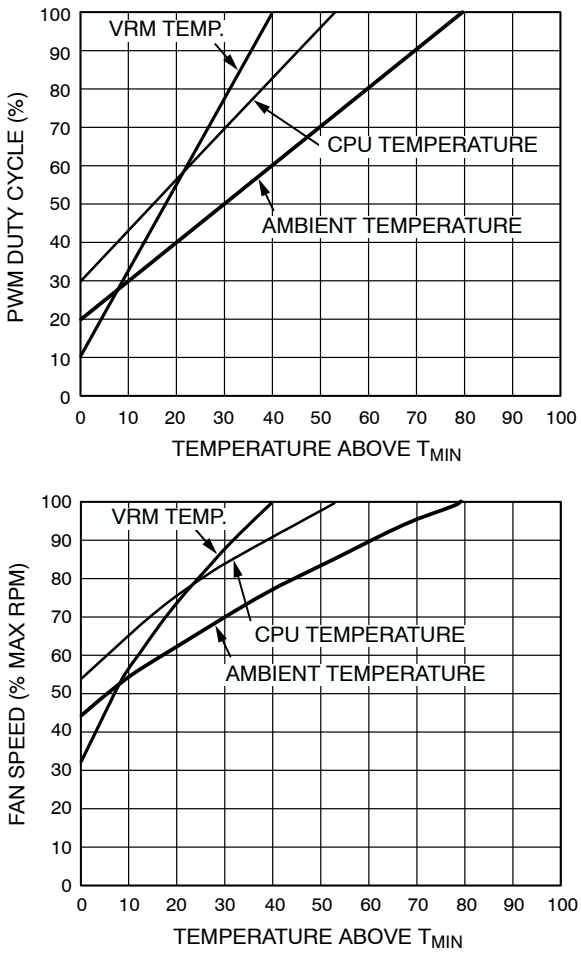


Figure 63. T_{RANGE} and % Fan Speed Slopes for VRM, Ambient, and CPU Temperature Channels

Example: Determining T_{RANGE} for Each Temperature Channel

The following example shows how the different T_{MIN} and T_{RANGE} settings can be applied to three different thermal zones. In this example, the following T_{RANGE} values apply:

T_{RANGE} = 80°C for ambient temperature

T_{RANGE} = 53.33°C for CPU temperature

T_{RANGE} = 40°C for VRM temperature

This example uses the mux configuration described in Step 2 - Configuring the Mux with the ADT7476A connected as shown in Figure 52. Both CPU temperature and VRM temperature drive the CPU fan connected to PWM1. Ambient temperature drives the front chassis fan and rear chassis fan connected to PWM2 and PWM3. The front chassis fan is configured to run at PWM_{MIN} = 20%. The rear chassis fan is configured to run at PWM_{MIN} = 30%. The CPU fan is configured to run at PWM_{MIN} = 10%.

Note: The control range for 4-wire fans is much wider than that of 3-wire fans. In many cases, 4-wire fans can start with a PWM drive of as little as 20% or less. In extreme cases, some 3-wire fans cannot run unless a PWM drive of 60% or more is applied.

Step 7 – $T_{\overline{THERM}}$ for Temperature Channels

$T_{\overline{THERM}}$ is the absolute maximum temperature allowed on a temperature channel. Above this temperature, a component such as the CPU or VRM can operate beyond its safe operating limit. When the temperature measured exceeds $T_{\overline{THERM}}$, all fans are driven at 100% PWM duty cycle (full speed) to provide critical system cooling.

The fans remain running at 100% until the temperature drops below $T_{\overline{THERM}}$ minus hysteresis, where hysteresis is the number programmed into the hysteresis registers (0x6D and 0x6E). The default hysteresis value is 4°C.

The $T_{\overline{THERM}}$ limit should be considered the maximum worst-case operating temperature of the system. Because exceeding any $T_{\overline{THERM}}$ limit runs all fans at 100%, it has very negative acoustic effects. Ultimately, this limit should be set up as a fail-safe, and users should ensure that it is not exceeded under normal system operating conditions.

Note: $T_{\overline{THERM}}$ limits are nonmaskable and affect the fan speed no matter how automatic fan control settings are configured. This allows some flexibility, because a T_{RANGE} value can be selected based on its slope, while a hard limit (such as 70°C), can be programmed as T_{MAX} (the temperature at which the fan reaches full speed) by setting $T_{\overline{THERM}}$ to that limit (for example, 70°C).

Table 48. $\overline{\text{THERM}}$ LIMIT REGISTERS

Register	Description	Default
0x6A	Remote 1 $\overline{\text{THERM}}$ Limit	0x64 (100°C)
0x6B	Local $\overline{\text{THERM}}$ Limit	0x64 (100°C)
0x6C	Remote 2 $\overline{\text{THERM}}$ Limit	0x64 (100°C)

$\overline{\text{THERM}}$ Hysteresis

$\overline{\text{THERM}}$ hysteresis on a particular channel is configured via the hysteresis settings (Register 0x6D and Register 0x6E). For example, setting hysteresis on the Remote 1 channel also sets the hysteresis on Remote 1 $\overline{\text{THERM}}$.

Hysteresis Registers

Register 0x6D, Remote 1, Local Temperature Hysteresis

[7:4], Remote 1 temperature hysteresis (4°C default).

[3:0], Local temperature hysteresis (4°C default).

Register 0x6E**,** Remote 2 Temperature Hysteresis

[7:4], Remote 2 temperature hysteresis (4°C default).

Because each hysteresis setting is four bits, hysteresis values are programmable from 1°C to 15°C. It is not recommended to program hysteresis values to 0°C, because this disables hysteresis. In effect, this causes the fans to cycle (during a $\overline{\text{THERM}}$ event) between normal speed and 100% speed, or, while operating close to T_{MIN}, between normal speed and off, creating unsettling acoustic noise.

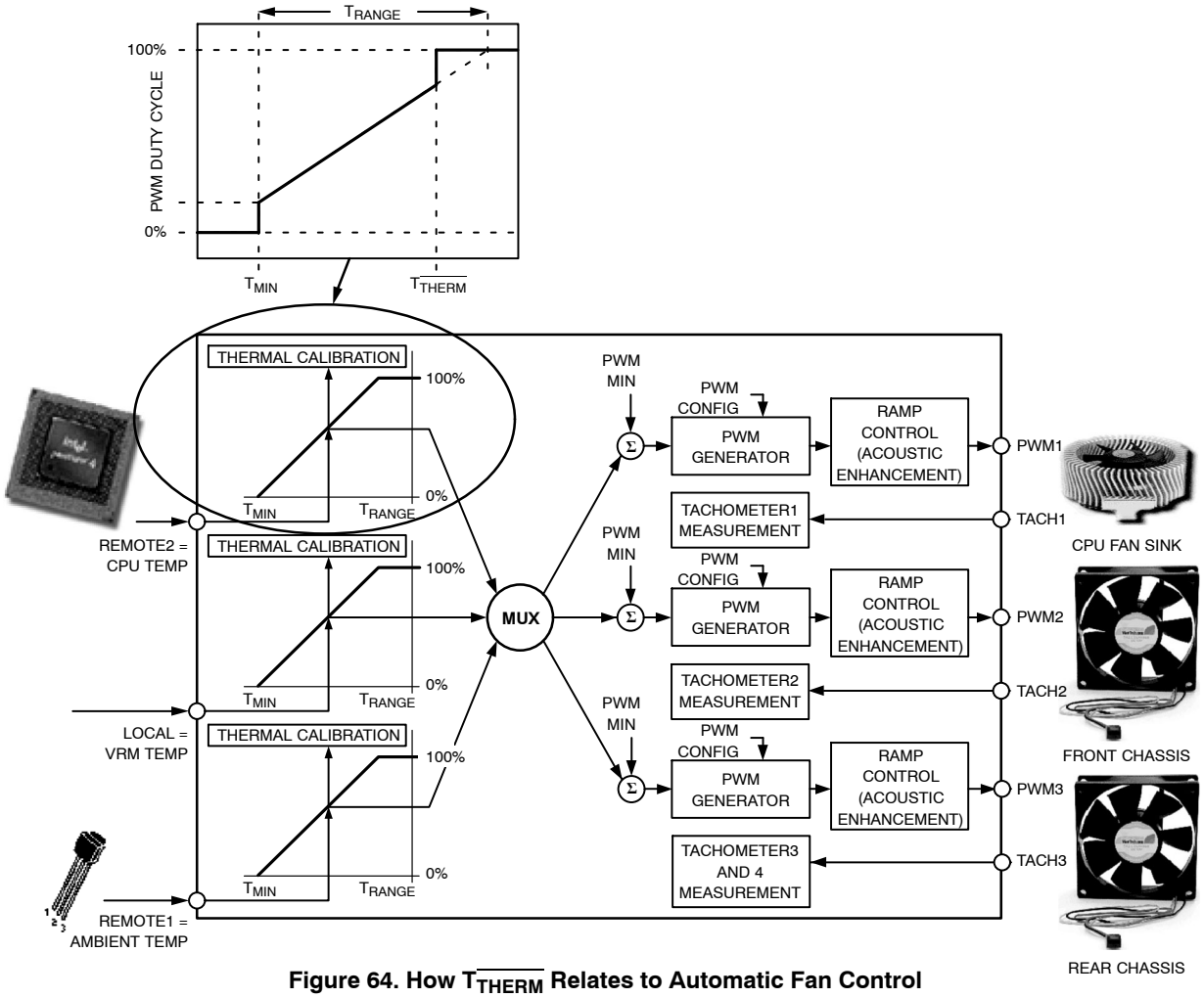


Figure 64. How $T_{\overline{\text{THERM}}}$ Relates to Automatic Fan Control

Step 8 – T_{HYST} for Temperature Channels

T_{HYST} is the amount of extra cooling a fan provides after the temperature measured has dropped back below T_{MIN} before the fan turns off. The premise for temperature hysteresis (T_{HYST}) is that without it, the fan would merely chatter, or cycle on and off regularly, whenever the temperature hovers around the T_{MIN} setting.

The T_{HYST} value chosen determines the amount of time needed for the system to cool down or heat up as the fan is turning on and off. Values of hysteresis are programmable in the range 1°C to 15°C. Larger values of T_{HYST} prevent the fans from chattering on and off. The T_{HYST} default value is set at 4°C.

The T_{HYST} setting applies not only to the temperature hysteresis for fan on/off, but the same setting is used for the $T\overline{THERM}$ hysteresis value, described in Step 6 - T_{RANGE} for Temperature Channels. Therefore, programming Register 0x6D and Register 0x6E sets the hysteresis for both fan on/off and the $\overline{THERM}$ function.

In some applications, it is required that fans not turn off below T_{MIN} but remain running at PWM_{MIN}. Bits [7:5] of Enhance Acoustics Register 1 (0x62) allow the fans to be turned off or to be kept spinning below T_{MIN}. If the fans are always on, the T_{HYST} value has no effect on the fan when the temperature drops below T_{MIN}.

$\overline{THERM}$ Hysteresis

Any hysteresis programmed via Register 0x6D and Register 0x6E also applies hysteresis on the appropriate $\overline{THERM}$ channel.

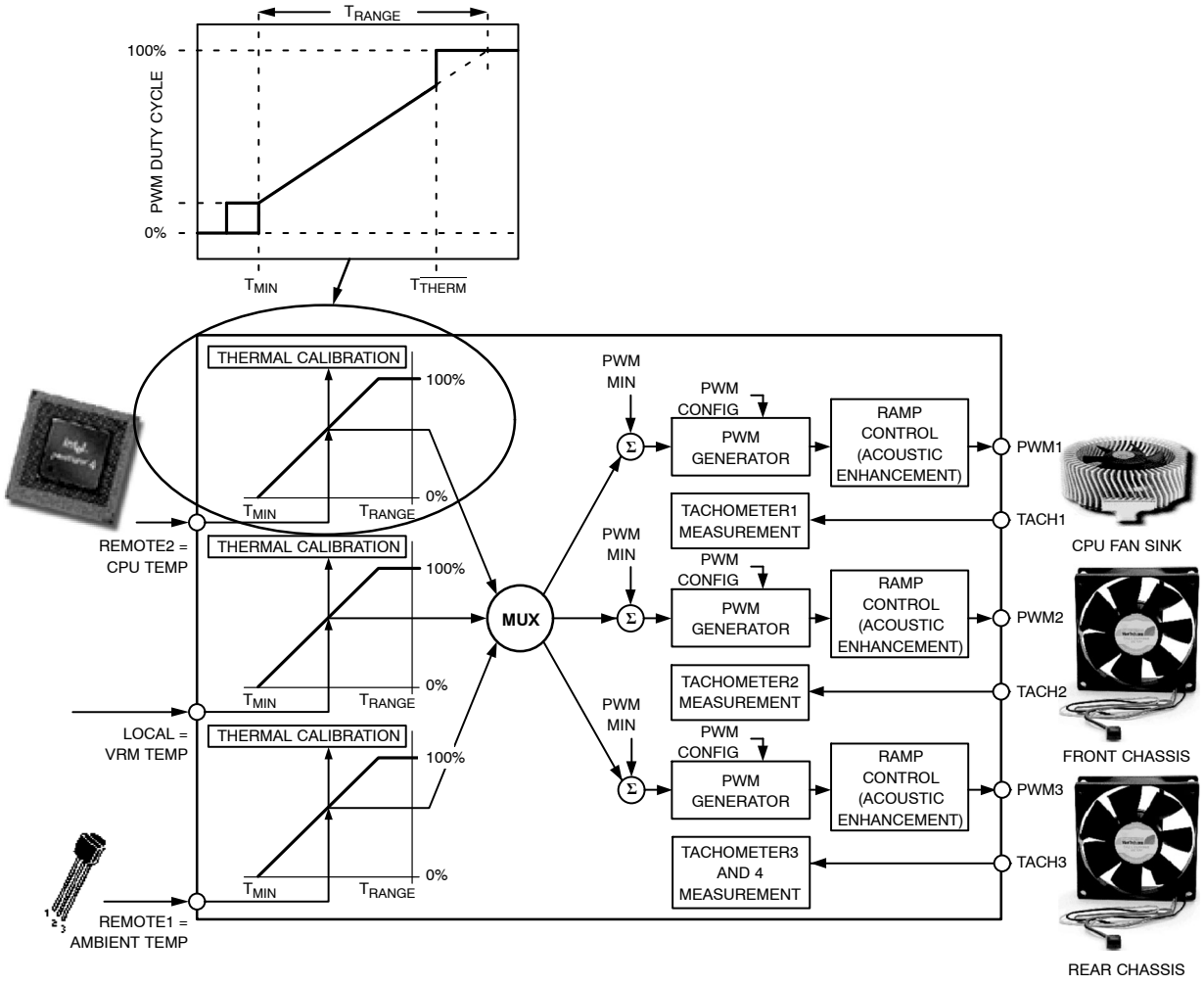


Figure 65. The T_{HYST} Value Applies to Fan On/Off Hysteresis and $\overline{THERM}$ Hysteresis

Enhance Acoustics Register 1 (0x62)

Bit 7 (MIN3) = 0, PWM3 is off (0% PWM duty cycle) when temperature is below $T_{MIN} - T_{HYST}$.

Bit 7 (MIN3) = 1, PWM3 runs at PWM3 minimum duty cycle below $T_{MIN} - T_{HYST}$.

Bit 6 (MIN2) = 0, PWM2 is off (0% PWM duty cycle) when temperature is below $T_{MIN} - T_{HYST}$.

Bit 6 (MIN2) = 1, PWM2 runs at PWM2 minimum duty cycle below $T_{MIN} - T_{HYST}$.

Bit 5 (MIN1) = 0, PWM1 is off (0% PWM duty cycle) when temperature is below $T_{MIN} - T_{HYST}$.

Bit 5 (MIN1) = 1, PWM1 runs at PWM1 minimum duty cycle below $T_{MIN} - T_{HYST}$.

Configuration Register 6 (0x10)

[0] SLOW = 1, slows the ramp rate for PWM changes associated with the Remote 1 temperature channel by a factor of 4.

[1] SLOW = 1, slows the ramp rate for PWM changes associated with the local temperature channel by a factor of 4.

[2] SLOW = 1, slows the ramp rate for PWM changes associated with the Remote 2 temperature channel by a factor of 4.

[7] ExtraSlow = 1, slows the ramp rate for all fans by a factor of 39.2%.

The following sections list the ramp-up times when enhanced acoustics is enabled for each temperature channel.

Enhance Acoustics Register 1 (0x62)

[2:0] ACOU selects the ramp rate for PWM outputs associated with the Remote Temperature 1 input.

000 = 37.5 sec
001 = 18.8 sec
010 = 12.5 sec
011 = 7.5 sec
100 = 4.7 sec
101 = 3.1 sec
110 = 1.6 sec
111 = 0.8 sec

Enhance Acoustics Register 2 (0x63)

[2:0] ACOU3 selects the ramp rate for PWM outputs associated with the local temperature channel.

000 = 37.5 sec
001 = 18.8 sec
010 = 12.5 sec
011 = 7.5 sec
100 = 4.7 sec
101 = 3.1 sec
110 = 1.6 sec
111 = 0.8 sec

[6:4] ACOU2 selects the ramp rate for PWM outputs associated with the Remote Temperature 2 input.

000 = 37.5 sec
001 = 18.8 sec
010 = 12.5 sec
011 = 7.5 sec
100 = 4.7 sec
101 = 3.1 sec
110 = 1.6 sec
111 = 0.8 sec

When Bit 7 of Configuration Register 6 (0x10) = 1, the above ramp rates change to the values below.

000 = 52.2 sec
001 = 26.1 sec
010 = 17.4 sec
011 = 10.4 sec
100 = 6.5 sec
101 = 4.4 sec
110 = 2.2 sec
111 = 1.1 sec

Setting the appropriate slow bit [2:0] of Configuration Register 6 (0x10) slows the ramp rate further by a factor of 4.

Fan Presence Detect

This feature is used to determine if a 4-wire fan is directly connected to a PWM output. This feature does not work for 3-wire fans. To detect whether a 4-wire fan is connected directly to a PWM output, the following must be performed in this order:

1. Drive the appropriate PWM outputs to 100% duty cycle.
2. Set Bit 0 of Configuration Register 2 (0x73).
3. Wait 5 ms.
4. Program fans to run at a different speed if necessary.
5. Read the state of Bits [3:1] of Configuration Register 2 (0x73). The state of these bits reflects whether a 4-wire fan is directly connected to the PWM output.

As the detection time only takes 5 ms, programming the PWM outputs to 100% and then back to its normal speed is not noticeable in most cases.

How Fan Presence Detect Works

4-wire fans typically have an internal pull up to 4.75 V ±10%, which typically sources 5 mA. While the detection cycle is on, an internal current sink is turned on, which sinks current from the fan's internal pullup. By driving some of the current from the fan's internal pullup (~100 μA) the logic buffer switches to a defined logic state. If this state is high, a fan is present; if the state is low, no fan is present.

Note: The PWM input voltage should be clamped to 3.3 V. This ensures the PWM output is not pulled to a voltage higher than the maximum allowable voltage on that pin (5.5 V).

Fan Sync

When two ADT7476As are used in a system, it is possible to synchronize them so that one PWM channel from each device can be effectively OR'ed together to create a PWM output that reflects the maximum speed of the two OR'ed PWMs. This OR'ed PWM can in turn be used to drive a chassis fan.

Standby Mode

The ADT7476A has been specifically designed to respond to the STBY supply. In computers that support S3 and S5 states, the core voltage of the processor is lowered in these states. When monitoring $\overline{\text{THERM}}$, the $\overline{\text{THERM}}$ timer should be disabled during these states.

When the V_{CCP} voltage drops below the V_{CCP} low limit, the following occurs:

1. Status Bit 1 (V_{CCP}) in Interrupt Status Register 1 is set.
2. $\overline{\text{SMBALERT}}$ is generated, if enabled.
3. $\overline{\text{THERM}}$ monitoring is disabled. The $\overline{\text{THERM}}$ timer should hold its value prior to the S3 or S5 state.

Once the core voltage, V_{CCP}, goes above the V_{CCP} low limit, everything is re-enabled and the system resumes normal operation.

XNOR Tree Test Mode

The ADT7476A includes an XNOR tree test mode. This mode is useful for in-circuit test equipment at board-level testing. By applying stimulus to the pins included in the XNOR tree, it is possible to detect opens, or shorts, on the system board.

The XNOR tree test is invoked by setting Bit 0 (XEN) of the XNOR Tree Test Enable Register (0x6F).

Figure 66 shows the signals that are exercised in the XNOR tree test mode.

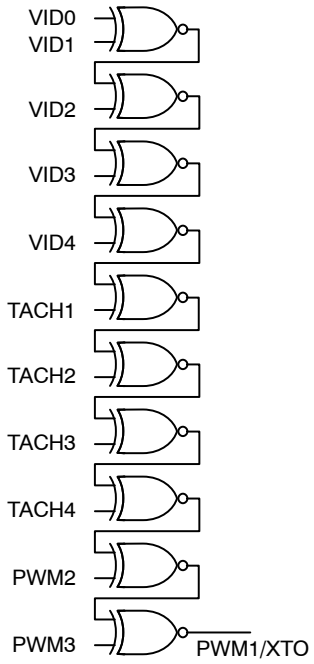


Figure 66. XNOR Tree Test

Power-On Default

When the ADT7476A is powered up, monitoring is off by default and the PWM outputs go to 100%. All necessary registers then need to be configured via the SMBus for the appropriate functions to operate.

Register Tables

Table 49. ADT7476A REGISTERS

Addr	R/W	Desc	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	De-fault	Lock-able
0x10	R/W	Configuration Register 6	Extra Slow	V_{CCP} Low	Master En	SlaveEn	$\overline{\text{THERM}}$ in Manual	SlowFan Remote 1	SlowFan Local	SlowFan Remote 1	0x00	Yes
0x11	R/W	Configuration Register 7	RES	RES	RES	RES	RES	RES	RES	Dis THERM Hys	0x00	Yes
0x20	R	2.5 V Measurement	9	8	7	6	5	4	3	2	0x00	–
0x21	R	V_{CCP} Measurement	9	8	7	6	5	4	3	2	0x00	–
0x22	R	V_{CC} Measurement	9	8	7	6	5	4	3	2	0x00	–
0x23	R	5.0 V Measurement	9	8	7	6	5	4	3	2	0x00	–
0x24	R	12 V Measurement	9	8	7	6	5	4	3	2	0x00	–
0x25	R	Remote 1 Temperature	9	8	7	6	5	4	3	2	0x80	–
0x26	R	Local Temperature	9	8	7	6	5	4	3	2	0x80	–
0x27	R	Remote 2 Temperature	9	8	7	6	5	4	3	2	0x80	–
0x28	R	TACH1 Low Byte	7	6	5	4	3	2	1	0	0x00	–
0x29	R	TACH1 High Byte	15	14	13	12	11	10	9	8	0x00	–
0x2A	R	TACH2 Low Byte	7	6	5	4	3	2	1	0	0x00	–
0x2B	R	TACH2 High Byte	15	14	13	12	11	10	9	8	0x00	–
0x2C	R	TACH3 Low Byte	7	6	5	4	3	2	1	0	0x00	–
0x2D	R	TACH3 High Byte	15	14	13	12	11	10	9	8	0x00	–
0x2E	R	TACH4 Low Byte	7	6	5	4	3	2	1	0	0x00	–
0x2F	R	TACH4 High Byte	15	14	13	12	11	10	9	8	0x00	–
0x30	R/W	PWM1 Current Duty Cycle	7	6	5	4	3	2	1	0	0xFF	–
0x31	R/W	PWM2 Current Duty Cycle	7	6	5	4	3	2	1	0	0xFF	–
0x32	R/W	PWM3 Current Duty Cycle	7	6	5	4	3	2	1	0	0xFF	–
0x38	R/W	PWM1 Max Duty Cycle	7	6	5	4	3	2	1	0	0xFF	Yes
0x39	R/W	PWM2 Max Duty Cycle	7	6	5	4	3	2	1	0	0xFF	Yes
0x3A	R/W	PWM3 Max Duty Cycle	7	6	5	4	3	2	1	0	0xFF	Yes
0x3D	R	Device ID Register	7	6	5	4	3	2	1	0	0x76	–
0x3E	R	Company ID Number	7	6	5	4	3	2	1	0	0x41	–
0x3F	R	Revision ID	7	6	5	4	3	2	1	0	0x6B	–
0x40	R/W	Configuration Register 1	RES	TODIS	FSPDIS	Vx1	FSPD	RDY	LOCK	STRT	0x04	Yes

Table 49. ADT7476A REGISTERS (continued)

Addr	R/W	Desc	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	De-fault	Lock-able
0x41	R	Interrupt Status Register 1	OOL	R2T	LT	R1T	5.0 V	V_{CC}	V_{CCP}	2.5 V/ $\overline{THERM}$	0x00	–
0x42	R	Interrupt Status Register 2	D2	D1	F4P	FAN3	FAN2	FAN1	OVT	12 V/VC	0x00	–
0x43	R/W	VID/GPIO	VIDSEL	THLD	VID 5	VID4/ GPIO4	VID3/ GPIO3	VID2/ GPIO2	VID1/ GPIO1	VID 0/ GPIO 0	0x1F	–
0x44	R/W	2.5 V Low Limit	7	6	5	4	3	2	1	0	0x00	–
0x45	R/W	2.5 V High Limit	7	6	5	4	3	2	1	0	0xFF	–
0x46	R/W	V_{CCP} Low Limit	7	6	5	4	3	2	1	0	0x00	–
0x47	R/W	V_{CCP} High Limit	7	6	5	4	3	2	1	0	0xFF	–
0x48	R/W	V_{CC} Low Limit	7	6	5	4	3	2	1	0	0x00	–
0x49	R/W	V_{CC} High Limit	7	6	5	4	3	2	1	0	0xFF	–
0x4A	R/W	5.0 V Low Limit	7	6	5	4	3	2	1	0	0x00	–
0x4B	R/W	5.0 V High Limit	7	6	5	4	3	2	1	0	0xFF	–
0x4C	R/W	12 V Low Limit	7	6	5	4	3	2	1	0	0x00	–
0x4D	R/W	12 V High Limit	7	6	5	4	3	2	1	0	0xFF	–
0x4E	R/W	Remote 1 Temp Low Limit	7	6	5	4	3	2	1	0	0x81	–
0x4F	R/W	Remote 1 Temp High Limit	7	6	5	4	3	2	1	0	0x7F	–
0x50	R/W	Local Temp Low Limit	7	6	5	4	3	2	1	0	0x81	–
0x51	R/W	Local Temp High Limit	7	6	5	4	3	2	1	0	0x7F	–
0x52	R/W	Remote 2 Temp Low Limit	7	6	5	4	3	2	1	0	0x81	–
0x53	R/W	Remote 2 Temp High Limit	7	6	5	4	3	2	1	0	0x7F	–
0x54	R/W	TACH1 Min Low Byte	7	6	5	4	3	2	1	0	0xFF	–
0x55	R/W	TACH1 Min High Byte	15	14	13	12	11	10	9	8	0xFF	–
0x56	R/W	TACH2 Min Low Byte	7	6	5	4	3	2	1	0	0xFF	–
0x57	R/W	TACH2 Min High Byte	15	14	13	12	11	10	9	8	0xFF	–
0x58	R/W	TACH3 Min Low Byte	7	6	5	4	3	2	1	0	0xFF	–
0x59	R/W	TACH3 Min High Byte	15	14	13	12	11	10	9	8	0xFF	–
0x5A	R/W	TACH4 Min Low Byte	7	6	5	4	3	2	1	0	0xFF	–
0x5B	R/W	TACH4 Min High Byte	15	14	13	12	11	10	9	8	0xFF	–
0x5C	R/W	PWM1 Configuration	BHVR	BHVR	BHVR	INV	RES	SPIN	SPIN	SPIN	0x62	Yes
0x5D	R/W	PWM2 Configuration	BHVR	BHVR	BHVR	INV	RES	SPIN	SPIN	SPIN	0x62	Yes
0x5E	R/W	PWM3 Configuration	BHVR	BHVR	BHVR	INV	RES	SPIN	SPIN	SPIN	0x62	Yes
0x5F	R/W	Remote 1 T_{RANGE}/PWM1 Frequency	RANGE	RANGE	RANGE	RANGE	HF/LF	FREQ	FREQ	FREQ	0XC4	Yes

Table 49. ADT7476A REGISTERS (continued)

Addr	R/W	Desc	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	De-fault	Lock-able
0x60	R/W	Local T_{RANGE}/PWM2 Frequency	RANGE	RANGE	RANGE	RANGE	HF/LF	FREQ	FREQ	FREQ	0XC4	Yes
0x61	R/W	Remote 2 T_{RANGE}/PWM3 Frequency	RANGE	RANGE	RANGE	RANGE	HF/LF	FREQ	FREQ	FREQ	0XC4	Yes
0x62	R/W	Enhance Acoustics Register 1	MIN3	MIN2	MIN1	SYNC	EN1	ACOU	ACOU	ACOU	0X00	Yes
0x63	R/W	Enhance Acoustics Register 2	EN2	ACOU2	ACOU2	ACOU2	EN3	ACOU3	ACOU3	ACOU3	0X00	Yes
0x64	R/W	PWM1 Min Duty Cycle	7	6	5	4	3	2	1	0	0X80	Yes
0x65	R/W	PWM2 Min Duty Cycle	7	6	5	4	3	2	1	0	0X80	Yes
0x66	R/W	PWM3 Min Duty Cycle	7	6	5	4	3	2	1	0	0X80	Yes
0x67	R/W	Remote 1 Temp T_{MIN}	7	6	5	4	3	2	1	0	0X5A	Yes
0x68	R/W	Local Temp T_{MIN}	7	6	5	4	3	2	1	0	0X5A	Yes
0x69	R/W	Remote 2 Temp T_{MIN}	7	6	5	4	3	2	1	0	0X5A	Yes
0x6A	R/W	Remote 1 $\overline{\text{THERM}}$ Limit	7	6	5	4	3	2	1	0	0X64	Yes
0x6B	R/W	Local $\overline{\text{THERM}}$ Limit	7	6	5	4	3	2	1	0	0X64	Yes
0x6C	R/W	Remote 2 $\overline{\text{THERM}}$ Limit	7	6	5	4	3	2	1	0	0X64	Yes
0x6D	R/W	Remote 1 and Local Temp/T_{MIN} Hysteresis	HYSR1	HYSR1	HYSR1	HYSR1	HYSL	HYSL	HYSL	HYSL	0X44	Yes
0x6E	R/W	Remote 2 Temp/T_{MIN} Hysteresis	HYSR2	HYSR2	HYSR2	HYRS	RES	RES	RES	RES	0X40	Yes
0x6F	R/W	XNOR Tree Test Enable	RES	RES	RES	RES	RES	RES	RES	XEN	0X00	Yes
0x70	R/W	Remote 1 Temp Offset	7	6	5	4	3	2	1	0	0X00	Yes
0x71	R/W	Local Temp Offset	7	6	5	4	3	2	1	0	0X00	Yes
0x72	R/W	Remote 2 Temp Offset	7	6	5	4	3	2	1	0	0X00	Yes
0x73	R/W	Configuration Register 2	RES	CONV	ATTN	AVG	Fan3 Detect	Fan2 Detect	Fan1 Detect	Fan PresDT	0X00	Yes
0x74	R/W	Interrupt Mask Register 1	OOL	R2T	LT	R1T	5.0 V	VCC	VCCP	2.5 V/ $\overline{\text{THERM}}$	0X00	–
0x75	R/W	Interrupt Mask Register 2	D2	D1	F4P	FAN3	FAN2	FAN1	OVT	12 V/VC	0X00	–
0x76	R/W	Extended Resolution Register 1	5.0 V	5.0 V	V_{CC}	V_{CC}	V_{CCP}	V_{CCP}	2.5 V	2.5 V	0X00	–
0x77	R/W	Extended Resolution Register 2	TDM2	TDM2	LTMP	LTMP	TDM1	TDM1	12 V	12 V	0X00	–
0x78	R/W	Configuration Register 3	DC4	DC3	DC2	DC1	FAST	BOOST	$\overline{\text{THERM}}$/ 2.5V	ALERT	0x00	Yes
0x79	R	$\overline{\text{THERM}}$ Timer Status	TMR	TMR	TMR	TMR	TMR	TMR	TMR	ASRT/T MRO	0x00	–

Table 49. ADT7476A REGISTERS (continued)

Addr	R/W	Desc	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	De-fault	Lock-able
0x7A	R/W	$\overline{\text{THERM}}$ Timer Limit	LIMT	LIMT	LIMT	LIMT	LIMT	LIMT	LIMT	LIMT	0x00	–
0x7B	R/W	TACH Pulses per Revolution	FAN4	FAN4	FAN3	FAN3	FAN2	FAN2	FAN1	FAN1	0x55	–
0x7C	R/W	Configuration Register 5	R2 $\overline{\text{THERM}}$	Local $\overline{\text{THERM}}$	R1 $\overline{\text{THERM}}$	VID/ GPIO	GPIO6P	GPIO6D	Temp Offset	2sC	0x01	Yes
0x7D	R/W	Configuration Register 4	BpAtt 12 V	BpAtt 5.0 V	BpAtt V_{CCP}	BpAtt 2.5 V	Max Speed on $\overline{\text{THERM}}$	$\overline{\text{THERM}}$ Disable	PIN14 FUNC	PIN14 FUNC	0x00	Yes
0x7E	R	Test 1	DO NOT WRITE TO THESE REGISTERS								0x00	Yes
0x7F	R	Test 2	DO NOT WRITE TO THESE REGISTERS								0x00	Yes

Table 50. REGISTER 0x10 – CONFIGURATION REGISTER 6 (POWER-ON DEFAULT = 0x00) (Note 1 and 2)

Bit No.	Mnemonic	R/W	Description
[0]	SlowFan Remote 1	R/W	When this bit is set, Fan 1 smoothing times are multiplied x4 for Remote 1 temperature channel (as defined in Register 0x62).
[1]	SlowFan Local	R/W	When this bit is set, Fan 2 smoothing times are multiplied x4 for local temperature channel (as defined in Register 0x63).
[2]	SlowFan Remote 2	R/W	When this bit is set, Fan 3 smoothing times are multiplied x4 for Remote 2 temperature channel (as defined in Register 0x63).
[3]	$\overline{\text{THERM}}$ in Manual	R/W	When this bit is set, $\overline{\text{THERM}}$ is enabled in manual mode. (Note 1)
[4]	SlaveEn	R/W	Setting this bit configures the ADT7476A as a slave for use in fan sync mode.
[5]	MasterEn	R/W	Setting this bit configures the ADT7476A as a master for use in fan sync mode.
[6]	V_{CCP} Low	R/W	V_{CCP}Low = 1. When the power is supplied from 3.3 V STANDBY and the core voltage (V_{CCP}) drops below its V_{CCP} low limit value (Register 0x46), the following occurs: Status Bit 1 in Interrupt Status Register 1 is set. $\overline{\text{SMBALERT}}$ is generated, if enabled. $\overline{\text{PROCHOT}}$ monitoring is disabled. Everything is re-enabled once V_{CCP} increases above the V_{CCP} low limit.When V_{CCP} increases above the low limit: $\overline{\text{PROCHOT}}$ monitoring is enabled. Fans return to their programmed state after a spin-up cycle.
[7]	ExtraSlow	R/W	When this bit is set, all fan smoothing times are increased by a further 39.2%

1. A $\overline{\text{THERM}}$ event always overrides any fan setting (even when fans are disabled).
2. This register becomes read-only when the Configuration Register 1 Lock bit is set to 1. Any subsequent attempts to write to this register fail.

Table 51. REGISTER 0x11 – CONFIGURATION REGISTER 7 (POWER-ON DEFAULT = 0x00) (Note 1)

Bit No.	Mnemonic	R/W	Description
[0]	DisTHERM Hys	Read/Write	Setting This Bit to 1 Disables $\overline{\text{THERM}}$ Hysteresis
[7:1]	Reserved	N/A	Reserved. Do Not Write to These Bits

1. This register becomes read-only when the Configuration Register 1 Lock bit is set to 1. Any subsequent attempts to write to this register fail.

Table 52. VOLTAGE READING REGISTERS (POWER-ON DEFAULT = 0x00) (Note 1)

Register Address	R/W	Description
0x20	Read-only	Reflects the Voltage Measurement at the 2.5 V Input on Pin 22 (8 MSBs of Reading)
0x21	Read-only	Reflects the Voltage Measurement (Note 2) at the V_{CCP} Input on Pin 23 (8 MSBs of Reading)
0x22	Read-only	Reflects the Voltage Measurement (Note 3) at the V_{CC} Input on Pin 4 (8 MSBs of Reading)
0x23	Read-only	Reflects the Voltage Measurement at the 5.0 V Input on Pin 20 (8 MSBs of Reading)
0x24	Read-only	Reflects the Voltage Measurement at the 12 V Input on Pin 21 (8 MSBs of Reading)

1. If the extended resolution bits of these readings are also being read, the extended resolution registers (Register 0x76, Register 0x77) must be read first. Once the extended resolution registers have been read, the associated MSB reading registers are frozen until read. Both the extended resolution registers and the MSB registers are frozen.
2. If V_{CCP}Low (Bit 7 of 0x40) is set, V_{CCP} can control the sleep state of the ADT7476A.
3. V_{CC} (Pin 4) is the supply voltage for the ADT7476A.

Table 53. TEMPERATURE READING REGISTERS (POWER-ON DEFAULT = 0x80) (Note 1. 2 and 3)

Register Address	R/W	Description
0x25	Read-only	Remote 1 Temperature Reading (Note 3 and 4) (8 MSBs of Reading)
0x26	Read-only	Local Temperature Reading (8 MSBs of Reading)
0x27	Read-only	Remote 2 Temperature Reading (Note 3 and 4) (8 MSBs of Reading)

1. If the extended resolution bits of these readings are also being read, the extended resolution registers (Register 0x76, Register 0x77) must be read first. Once the extended resolution registers have been read, all associated MSB reading registers are frozen until read. Both the extended resolution registers and the MSB registers are frozen.
2. These temperature readings can be in twos complement or Offset 64 format; this interpretation is determined by Bit 0 of Configuration Register 5 (0x7C).
3. In twos complement mode, a temperature reading of −128°C (0x80) indicates a diode fault (open or short) on that channel.
4. In Offset 64 mode, a temperature reading of −64°C (0x00) indicates a diode fault (open or short) on that channel.

Table 54. FAN TACHOMETER READING REGISTERS (POWER-ON DEFAULT = 0x00) (Note 1)

Register Address	R/W	Description
0x28	Read-only	TACH1 Low Byte
0x29	Read-only	TACH1 High Byte
0x2A	Read-only	TACH2 Low Byte
0x2B	Read-only	TACH2 High Byte
0x2C	Read-only	TACH3 Low Byte
0x2D	Read-only	TACH3 High Byte
0x2E	Read-only	TACH4 Low Byte
0x2F	Read-only	TACH4 High Byte

1. These registers count the number of 11.11 μs periods (based on an internal 90 kHz clock) that occur between a number of consecutive fan TACH pulses (default = 2). The number of TACH pulses used to count can be changed using the TACH Pulses per Revolution register (Register 0x7B). This allows the fan speed to be accurately measured. Because a valid fan tachometer reading requires that two bytes be read, the low byte must be read first. Both the low and high bytes are then frozen until read. At power-on, these registers contain 0x0000 until the first valid fan TACH measurement is read into these registers. This prevents false interrupts from occurring while the fans are spinning up. A count of 0xFFFF indicates that a fan is one of the following: stalled or blocked (object jamming the fan), failed (internal circuitry destroyed), or not populated. (The ADT7476A expects to see a fan connected to each TACH. If a fan is not connected to that TACH, its TACH minimum high and low bytes should be set to 0xFFFF.) An alternate function, for example, is TACH4 reconfigured as the $\overline{\text{THERM}}$ pin.

Table 55. CURRENT PWM DUTY CYCLE REGISTERS (POWER-ON DEFAULT = 0xFF) (Note 1)

Register Address	R/W	Description
0x30	R/W	PWM1 Current Duty Cycle (0% to 100% Duty Cycle = 0x00 to 0xFF)
0x31	R/W	PWM2 Current Duty Cycle (0% to 100% Duty Cycle = 0x00 to 0xFF)
0x32	R/W	PWM3 Current Duty Cycle (0% to 100% Duty Cycle = 0x00 to 0xFF)

1. These registers reflect the PWM duty cycle driving each fan at any given time. When in automatic fan speed control mode, the ADT7476A reports the PWM duty cycles back through these registers. The PWM duty cycle values vary according to temperature in automatic fan speed control mode. During fan startup, these registers report back 0x00. In manual mode, the PWM duty cycle outputs can be set to any duty cycle value by writing to these registers.

Table 56. PWM MAXIMUM DUTY CYCLE (POWER-ON DEFAULT = 0xFF) (Note 1 and 2)

Register Address	R/W	Description
0x38	R/W	Maximum Duty Cycle for PWM1 Output, Default = 100% (0xFF)
0x39	R/W	Maximum Duty Cycle for PWM2 Output, Default = 100% (0xFF)
0x3A	R/W	Maximum Duty Cycle for PWM3 Output, Default = 100% (0xFF)

1. These registers set the maximum PWM duty cycle of the PWM output.
2. This register becomes read-only when the Configuration Register 1 Lock bit is set to 1. Any subsequent attempts to write to this register fail.

Table 57. REGISTER 0x40 – CONFIGURATION REGISTER 1 (POWER-ON DEFAULT = 0x04)

Bit No.	Mnemonic	R/W	Description
[0]	STRT (Notes 1, 2)	Read/Write	Logic 1 enables monitoring and PWM control outputs based on the limit settings programmed. Logic 0 disables monitoring and PWM control is based on the default powerup limit settings. Note that the limit values programmed are preserved even if a Logic 0 is written to this bit and the default settings are enabled. This bit does not become locked once Bit 1 (LOCK bit) has been set.
[1]	LOCK	Write once	Logic 1 locks all limit values to their current settings. Once this bit is set, all lockable registers become read-only and cannot be modified until the ADT7476A is powered down and powered up again. This prevents rogue programs such as viruses from modifying critical system limit settings. (Lockable.)
[2]	RDY	Read-only	This bit is set to 1 by the ADT7476A to indicate that the device is fully powered-up and ready to begin system monitoring.
[3]	FSPD	R/W	When set to 1, this bit runs all fans at max speed as programmed in the max PWM current duty cycle registers (0x30 to 0x32). Power-on default = 0. This bit is not locked at any time.
[4]	Vx1	R/W	BIOS should set this bit to a 1 when the ADT7476A is configured to measure current from an ADOPT® VRM controller and to measure the CPU's core voltage. This bit allows monitoring software to display CPU watts usage. (Lockable.)
[5]	FSPDIS	R/W	Logic 1 disables fan spin-up for two TACH pulses. Instead, the PWM outputs go high for the entire fan spin-up timeout selected.
[6]	TODIS	R/W	When this bit is set to 1, the SMBus timeout feature is disabled. This allows the ADT7476A to be used with SMBus controllers that cannot handle SMBus timeouts. This bit is lockable.
[7]	Reserved	N/A	Reserved. Do not write to this bit.

1. Bit 0 (STRT) of Configuration Register 1 (0x40) remains writable after lock bit is set.
2. When monitoring (STRT) is disabled, PWM outputs always go to 100% for thermal protection.

Table 58. REGISTER 0x41 – INTERRUPT STATUS REGISTER 1 (POWER-ON DEFAULT = 0x00)

Bit No.	Mnemonic	R/W	Description
[0]	2.5 V/ $\overline{\text{THERM}}$	Read-only	2.5 V = 1 indicates that the 2.5 V high or low limit has been exceeded. This bit is cleared on a read of the status register only if the error condition has subsided. If Pin 22 is configured as $\overline{\text{THERM}}$, this bit is asserted when the timer limit has been exceeded.
[1]	V_{CCP}	Read-only	V_{CCP} = 1 indicates that the V_{CCP} high or low limit has been exceeded. This bit is cleared on a read of the status register only if the error condition has subsided.
[2]	V_{CC}	Read-only	V_{CC} = 1 indicates that the V_{CC} high or low limit has been exceeded. This bit is cleared on a read of the status register only if the error condition has subsided.
[3]	5.0 V	Read-only	A 1 indicates that the 5.0 V high or low limit has been exceeded. This bit is cleared on a read of the status register only if the error condition has subsided.
[4]	R1T	Read-only	R1T = 1 indicates that the Remote 1 low or high temperature has been exceeded. This bit is cleared on a read of the status register only if the error condition has subsided.
[5]	LT	Read-only	LT = 1 indicates that the local low or high temperature has been exceeded. This bit is cleared on a read of the status register only if the error condition has subsided.
[6]	R2T	Read-only	R2T = 1 indicates that the Remote 2 low or high temperature has been exceeded. This bit is cleared on a read of the status register only if the error condition has subsided.
[7]	OOL	Read-only	OOL = 1 indicates that an out-of-limit event has been latched in Interrupt Status Register 2. This bit is a logical OR of all status bits in Interrupt Status Register 2. Software can test this bit in isolation to determine whether any of the voltage, temperature, or fan speed readings represented by Interrupt Status Register 2 are out-of-limit, which eliminates the need to read Interrupt Status Register 2 during every interrupt or polling cycle.

Table 59. REGISTER 0x42 – INTERRUPT STATUS REGISTER 2 (POWER-ON DEFAULT = 0x00)

Bit No.	Mnemonic	R/W	Description
[0]	12 V/VC	Read-only	A 1 indicates that the 12 V high or low limit has been exceeded. This bit is cleared on a read of the status register only if the error condition has subsided. If Pin 21 is configured as VID5, this bit is the VID change bit. This bit is set when the levels on VID0 to VID5 are different than they were 11 μs previously. This pin can be used to generate an SMBALERT whenever the VID code changes.
[1]	OVT	Read-only	OVT = 1 indicates that one of the THERM overtemperature limits has been exceeded. This bit is cleared on a read of the status register when the temperature drops below THERM – T_{HYST}.
[2]	FAN1	Read-only	FAN1 = 1 indicates that Fan 1 has dropped below minimum speed or has stalled. This bit is not set when the PWM1 output is off.
[3]	FAN2	Read-only	FAN2 = 1 indicates that Fan 2 has dropped below minimum speed or has stalled. This bit is not set when the PWM2 output is off.
[4]	FAN3	Read-only	FAN3 = 1 indicates that Fan 3 has dropped below minimum speed or has stalled. This bit is not set when the PWM3 output is off.
[5]	F4P	Read-only R/W Read-only	When Pin 14 is programmed as a TACH4 input, F4P = 1 indicates that Fan 4 has dropped below minimum speed or has stalled. This bit is not set when the PWM3 output is off. When Pin 14 is programmed as the GPIO6 output, writing to this bit determines the logic output of GPIO6. When GPIO6 is programmed as an input, this bit reflects the value read by GPIO6. If Pin 14 is configured as the THERM timer input for THERM monitoring, then this bit is set when the THERM assertion time exceeds the limit programmed in the THERM timer limit register (0x7A).
[6]	D1	Read-only	D1 = 1 indicates either an open or short circuit on the Thermal Diode 1 inputs.
[7]	D2	Read-only	D2 = 1 indicates either an open or short circuit on the Thermal Diode 2 inputs.

Table 60. REGISTER 0x43 – VID/GPIO REGISTER (POWER-ON DEFAULT = 0x1F)

Bit No.	Mnemonic	R/W	Description
[4:0]	VID[4:0]/ GPIO[4:0]	R/W	The VID[4:0] inputs from the CPU indicate the expected processor core voltage. On powerup, these bits reflect the state of the VID pins, even if monitoring is not enabled. When Bit 4 of Configuration Register 5 (0x7C) = 1, these bits become general-purpose outputs. The state of these bits then reflects the state of the appropriate GPIO pin.
[5]	VID5	R/W	Reads VID5 from the CPU when Bit 7 = 1. If Bit 7 = 0, the VID5 bit always reads back 0 (power-on default).
[6]	THLD	R/W	Selects the input switching threshold for the VID inputs. THLD = 0 selects a threshold of 1 V (V_{OL} < 0.8 V, V_{IH} > 1.7 V). THLD = 1 lowers the switching threshold to 0.6 V (V_{OL} < 0.4 V, V_{IH} > 0.8 V).
[7]	VIDSEL	R/W	VIDSEL = 0 configures Pin 21 as the 12 V measurement input (Default).

Table 61. VOLTAGE LIMIT REGISTERS (Note 1)

Register Address	R/W	Description (Note 2)	Power-On Default
0x44	R/W	2.5 V Low Limit	0x00
0x45	R/W	2.5 V High Limit	0xFF
0x46	R/W	V_{CCP} Low Limit	0x00
0x47	R/W	V_{CCP} High Limit	0xFF
0x48	R/W	V_{CC} Low Limit	0x00
0x49	R/W	V_{CC} High Limit	0xFF
0x4A	R/W	5.0 V Low Limit	0x00
0x4B	R/W	5.0 V High Limit	0xFF
0x4C	R/W	12 V Low Limit	0x00
0x4D	R/W	12 V High Limit	0xFF

1. Setting the Configuration Register 1 Lock bit has no effect on these registers.
2. High limits: An interrupt is generated when a value exceeds its high limit (> comparison). Low limits: An interrupt is generated when a value is equal to or below its low limit (≤ comparison).

Table 62. TEMPERATURE LIMIT REGISTERS (Note 1)

Register Address	R/W	Description (Note 2)	Power-On Default
0x4E	R/W	Remote 1 Temperature Low Limit	0x81
0x4F	R/W	Remote 1 Temperature High Limit	0x7F
0x50	R/W	Local Temperature Low Limit	0x81
0x51	R/W	Local Temperature High Limit	0x7F
0x52	R/W	Remote 2 Temperature Low Limit	0x81
0x53	R/W	Remote 2 Temperature High Limit	0x7F

1. Exceeding any of these temperature limits by 1°C causes the appropriate status bit to be set in the interrupt status register. Setting the Configuration Register 1 Lock bit has no effect on these registers.
2. High limits: An interrupt is generated when a value exceeds its high limit (> comparison). Low limits: An interrupt is generated when a value is equal to or below its low limit (≤ comparison).

Table 63. FAN TACH LIMIT REGISTERS (Note 1)

Register Address	R/W	Description	Power-On Default
0x54	R/W	TACH1 Minimum Low Byte	0xFF
0x55	R/W	TACH1 Minimum High Byte/Single-channel ADC Channel Select	0xFF
0x56	R/W	TACH2 Minimum Low Byte	0xFF
0x57	R/W	TACH2 Minimum High Byte	0xFF
0x58	R/W	TACH3 Minimum Low Byte	0xFF
0x59	R/W	TACH3 Minimum High Byte	0xFF
0x5A	R/W	TACH4 Minimum Low Byte	0xFF
0x5B	R/W	TACH4 Minimum High Byte	0xFF

1. Exceeding any of the TACH limit registers by 1 indicates that the fan is running too slowly or has stalled. The appropriate status bit is set in Interrupt Status Register 2 to indicate the fan failure. Setting the Configuration Register 1 Lock bit has no effect on these registers.

Table 64. REGISTER 0x55 – TACH1 MINIMUM HIGH BYTE (POWER-ON DEFAULT = 0xFF)

Bit No.	Mnemonic	R/W	Description
[4:0]	Reserved	Read-only	When Bit 6 of Configuration 2 Register (0x73) is set (single-channel ADC mode), these bits are reserved. Otherwise, these bits represent Bits [4:0] of the TACH1 minimum high byte.
[7:5]	SCADC	R/W	When Bit 6 of Configuration 2 Register (0x73) is set (single-channel ADC mode), these bits are used to select the only channel from which the ADC will take measurements. Otherwise, these bits represent Bits [7:5] of the TACH1 minimum high byte.

Table 65. PWM CONFIGURATION REGISTERS (Note 1)

Register Address		R/W	Description	Power-On Default
0x5C		R/W	PWM1 Configuration	0x62
0x5D		R/W	PWM2 Configuration	0x62
0x5E		R/W	PWM3 Configuration	0x62
Bit No.	**Name**	**R/W**	**Description**	
[2:0]	SPIN	R/W	These bits control the startup timeout for PWMx. The PWM output stays high until two valid TACH rising edges are seen from the fan. If there is not a valid TACH signal during the fan TACH measurement directly after the fan startup timeout period, the TACH measurement reads 0xFFFF and Interrupt Status Register 2 reflects the fan fault. If the TACH minimum high and low bytes contain 0xFFFF or 0x0000, the Interrupt Status Register 2 bit is not set, even if the fan has not started. 000 = No Startup Timeout 001 = 100 ms 010 = 250 ms (Default) 011 = 400 ms 100 = 667 ms 101 = 1 sec 110 = 2 sec 111 = 4 sec	
[3]	RES	N/A	Reserved. Do not write to this bit.	
[4]	INV	R/W	This bit inverts the PWM output. The default is 0, which corresponds to a logic high output for 100% duty cycle. Setting this bit to 1 inverts the PWM output, so 100% duty cycle corresponds to a logic low output.	
[7:5]	BHVR	R/W	These bits assign each fan to a particular temperature sensor for localized cooling. 000 = Remote 1 Temperature Controls PWMx (Automatic Fan Control Mode) 001 = Local Temperature Controls PWMx (Automatic Fan Control Mode) 010 = Remote 2 Temperature Controls PWMx (Automatic Fan Control Mode) 011 = PWMx Runs Full Speed (Default) 100 = PWMx Disabled 101 = Fastest Speed Calculated by Local and Remote 2 Temperature Controls PWMx 110 = Fastest Speed Calculated by All Three Temperature Channel Controls PWMx 111 = Manual Mode. PWM Current Duty Cycle Registers (0x30 to 0x32) Become Writable	

1. These registers become read-only when the Configuration Register 1 Lock bit is set to 1. Any subsequent attempts to write to these registers fail.

Table 66. T_{RANGE}/PWM FREQUENCY REGISTERS (Note 1)

Register Address		R/W	Description	Power-On Default
0x5F		R/W	Remote 1 T_{RANGE}/PWM1 Frequency	0xC4
0x60		R/W	Local T_{RANGE}/PWM2 Frequency	0xC4
0x61		R/W	Remote 2 T_{RANGE}/PWM3 Frequency	0xC4
Bit No.	**Name**	**R/W**	**Description**	
[2:0]	FREQ	R/W	These bits control the PWMx frequency (only apply when PWM channel is in low frequency mode). 000 = 11.0 Hz 001 = 14.7 Hz 010 = 22.1 Hz 011 = 29.4 Hz 100 = 35.3 Hz (Default) 101 = 44.1 Hz 110 = 58.8 Hz 111 = 88.2 Hz	
[3]	HF/LR	R/W	HF/LF = 1, High Frequency PWM Mode is Enabled for PWMx HF/LF = 0, Low Frequency PWM Mode is Enabled for PWMx.	
[7:4]	RANGE	R/W	These bits determine the PWM duty cycle vs. the temperature range for automatic fan control. 0000 = 2°C 0001 = 2.5°C 0010 = 3.33°C 0011 = 4°C 0100 = 5°C 0101 = 6.67°C 0110 = 8°C 0111 = 10°C 1000 = 13.33°C 1001 = 16°C 1010 = 20°C 1011 = 26.67°C 1100 = 32°C (Default) 1101 = 40°C 1110 = 53.33°C 1111 = 80°C	

1. These registers become read-only when the Configuration Register 1 Lock bit is set. Any further attempts to write to these registers have no effect.

Table 67. REGISTER 0x62 – ENHANCED ACOUSTICS REGISTER 1 (POWER-ON DEFAULT = 0x00) (Note 1)

Bit No.	Mnemonic	R/W	Description
[2:0]	ACOU (Note 2)	R/W	Assuming that PWMx is associated with the Remote 1 temperature channel, these bits define the maximum rate of change of the PWMx output for Remote 1 temperature-related changes. Instead of the fan speed jumping instantaneously to its newly determined speed, it ramps gracefully at the rate determined by these bits. This feature ultimately enhances the acoustics of the fan. **When Bit 7 of Configuration Register 6 (0x10) is 0** **Time Slot Increase** — **Time for 0% to 100%** 000 = 1 — 37.5 sec 001 = 2 — 18.8 sec 010 = 3 — 12.5 sec 011 = 4 — 7.5 sec 100 = 8 — 4.7 sec 101 = 12 — 3.1 sec 110 = 24 — 1.6 sec 111 = 48 — 0.8 sec **When Bit 7 of Configuration Register 6 (0x10) is 1** **Time Slot Increase** — **Time for 0% to 100%** 000 = 1 — 52.2 sec 001 = 2 — 26.1 sec 010 = 3 — 17.4 sec 011 = 4 — 10.4 sec 100 = 8 — 6.5 sec 101 = 12 — 4.4 sec 110 = 24 — 2.2 sec 111 = 48 — 1.1 sec
[3]	EN1	R/W	When this bit is 1, smoothing is enabled on Remote 1 temperature channel.
[4]	SYNC	R/W	SYNC = 1 synchronizes fan speed measurements on TACH2, TACH3, and TACH4 to PWM3. This allows up to three fans to be driven from PWM3 output and their speeds to be measured. SYNC = 0 synchronizes only TACH3 and TACH4 to PWM3 output.
[5]	MIN1	R/W	When the ADT7476A is in automatic fan control mode, this bit defines whether PWM1 is off (0% duty cycle) or at PWM1 minimum duty cycle when the controlling temperature is below its T_{MIN} – hysteresis value. 0 = 0% duty cycle below T_{MIN} – hysteresis 1 = PWM1 minimum duty cycle below T_{MIN} – hysteresis
[6]	MIN2	R/W	When the ADT7476A is in automatic fan speed control mode, this bit defines whether PWM2 is off (0% duty cycle) or at PWM2 minimum duty cycle when the controlling temperature is below its T_{MIN} – hysteresis value. 0 = 0% duty cycle below T_{MIN} – hysteresis 1 = PWM2 minimum duty cycle below T_{MIN} – hysteresis
[7]	MIN3	R/W	When the ADT7476A is in automatic fan speed control mode, this bit defines whether PWM3 is off (0% duty cycle) or at PWM3 minimum duty cycle when the controlling temperature is below its T_{MIN} – hysteresis value. 0 = 0% duty cycle below T_{MIN} – hysteresis 1 = PWM3 minimum duty cycle below T_{MIN} – hysteresis

1. This register becomes read-only when the Configuration Register 1 Lock bit is set to 1. Any further attempts to write to this register have no effect.
2. Setting the relevant bit of Configuration Register 6 (0x10, [2:0]) further decreases these ramp rates by a factor of 4.

Table 68. REGISTER 0x63 – ENHANCED ACOUSTICS REGISTER 2 (POWER-ON DEFAULT = 0x00) (Note 1)

Bit No.	Mnemonic	R/W	Description
[2:0]	ACOU3	R/W	Assuming that PWMx is associated with the local temperature channel, these bits define the maximum rate of change of the PWMx output for local temperature-related changes. Instead of the fan speed jumping instantaneously to its newly determined speed, it ramps gracefully at the rate determined by these bits. This feature ultimately enhances the acoustics of the fan. **When Bit 7 of Configuration Register 6 (0x10) is 0** **Time Slot Increase** — **Time for 0% to 100%** 000 = 1 — 37.5 sec 001 = 2 — 18.8 sec 010 = 3 — 12.5 sec 011 = 4 — 7.5 sec 100 = 8 — 4.7 sec 101 = 12 — 3.1 sec 110 = 24 — 1.6 sec 111 = 48 — 0.8 sec **When Bit 7 of Configuration Register 6 (0x10) is 1** **Time Slot Increase** — **Time for 0% to 100%** 000 = 1 — 52.2 sec 001 = 2 — 26.1 sec 010 = 3 — 17.4 sec 011 = 4 — 10.4 sec 100 = 8 — 6.5 sec 101 = 12 — 4.4 sec 110 = 24 — 2.2 sec 111 = 48 — 1.1 sec
[3]	EN3	R/W	When this bit is 1, smoothing is enabled on the local temperature channel.
[6:4]	ACOU2	R/W	Assuming that PWMx is associated with the Remote 2 temperature channel, these bits define the maximum rate of change of the PWMx output for Remote 2 Temperature related changes. Instead of the fan speed jumping instantaneously to its newly determined speed, it ramps gracefully at the rate determined by these bits. This feature ultimately enhances the acoustics of the fan. **When Bit 7 of Configuration Register 6 (0x10) is 0** **Time Slot Increase** — **Time for 0% to 100%** 000 = 1 — 37.5 sec 001 = 2 — 18.8 sec 010 = 3 — 12.5 sec 011 = 4 — 7.5 sec 100 = 8 — 4.7 sec 101 = 12 — 3.1 sec 110 = 24 — 1.6 sec 111 = 48 — 0.8 sec **When Bit 7 of Configuration Register 6 (0x10) is 1** **Time Slot Increase** — **Time for 0% to 100%** 000 = 1 — 52.2 sec 001 = 2 — 26.1 sec 010 = 3 — 17.4 sec 011 = 4 — 10.4 sec 100 = 8 — 6.5 sec 101 = 12 — 4.4 sec 110 = 24 — 2.2 sec 111 = 48 — 1.1 sec
[7]	EN2	R/W	When this bit is 1, smoothing is enabled on the Remote 2 temperature channel.

1. This register becomes read-only when the Configuration Register 1 Lock bit is set to 1. Any further attempts to write to this register have no effect.

Table 69. PWM MINIMUM DUTY CYCLE REGISTERS (Note 1)

Register Address		R/W	Description	Power-On Default
0x64		R/W	PWM1 Minimum Duty Cycle	0x80 (50% Duty Cycle)
0x65		R/W	PWM2 Minimum Duty Cycle	0x80 (50% Duty Cycle)
0x66		R/W	PWM3 Minimum Duty Cycle	0x80 (50% Duty Cycle)
Bit No.	**Name**	**R/W**	**Description**	
[7:0]	PWM Duty Cycle	R/W	These bits define the PWM_{MIN} duty cycle for PWMx. 0x00 = 0% Duty Cycle (Fan Off) 0x40 = 25% Duty Cycle 0x80 = 50% Duty Cycle 0xFF = 100% Duty Cycle (Fan Full Speed)	

1. These registers become read-only when the ADT7476A is in automatic fan control mode.

Table 70. T_{MIN} REGISTERS (Note 1 and 2)

Register Address	R/W	Description	Power-On Default
0x67	R/W	Remote 1 Temperature T_{MIN}	0x5A (90°C)
0x68	R/W	Local Temperature T_{MIN}	0x5A (90°C)
0x69	R/W	Remote 2 Temperature T_{MIN}	0x5A (90°C)

1. These are the T_{MIN} registers for each temperature channel. When the temperature measured exceeds T_{MIN}, the appropriate fan runs at minimum speed and increases with temperature according to T_{RANGE}.
2. These registers become read-only when the Configuration Register 1 Lock bit is set. Any further attempts to write to these registers have no effect.

Table 71. $\overline{\text{THERM}}$ LIMIT REGISTERS (Note 1 and 2)

Register Address	R/W	Description	Power-On Default
0x6A	R/W	Remote 1 $\overline{\text{THERM}}$ Temperature Limit	0x64 (100°C)
0x6B	R/W	Local $\overline{\text{THERM}}$ Temperature Limit	0x64 (100°C)
0x6C	R/W	Remote 2 $\overline{\text{THERM}}$ Temperature Limit	0x64 (100°C)

1. If any temperature measured exceeds its $\overline{\text{THERM}}$ limit, all PWM outputs drive their fans at 100% duty cycle. This is a fail-safe mechanism incorporated to cool the system in the event of a critical overtemperature. It also ensures some level of cooling in the event that software or hardware locks up. If set to 0x80, this feature is disabled. The PWM output remains at 100% until the temperature drops below $\overline{\text{THERM}}$ limit − hysteresis. If the $\overline{\text{THERM}}$ pin is programmed as an output, exceeding these limits by 0.25°C can cause the $\overline{\text{THERM}}$ pin to assert low as an output.
2. These registers become read-only when the Configuration Register 1 Lock bit is set to 1. Any further attempts to write to these registers have no effect.

Table 72. TEMPERATURE/T_{MIN} HYSTERESIS REGISTERS (Note 1 and 2)

Register Address	R/W	Description	Power-On Default
0x6D	R/W	Remote 1 and local temperature hysteresis.	0x44
[3:0]	HYSL	Local temperature hysteresis. 0°C to 15°C of hysteresis can be applied to the local temperature AFC control loops.	
[7:4]	HYSR1	Remote 1 temperature hysteresis. 0°C to 15°C of hysteresis can be applied to the Remote 1 temperature AFC control loops.	
0x6E	R/W	Remote 2 temperature hysteresis.	0x40
	HYSR2	Local temperature hysteresis. 0°C to 15°C of hysteresis can be applied to the local temperature AFC control loops.	

1. Each 4-bit value controls the amount of temperature hysteresis applied to a particular temperature channel. Once the temperature for that channel falls below its T_{MIN} value, the fan remains running at PWM_{MIN} duty cycle until the temperature = T_{MIN} − hysteresis. Up to 15°C of hysteresis can be assigned to any temperature channel. The hysteresis value chosen also applies to that temperature channel if its $\overline{\text{THERM}}$ limit is exceeded. The PWM output being controlled goes to 100% if the $\overline{\text{THERM}}$ limit is exceeded and remains at 100% until the temperature drops below $\overline{\text{THERM}}$ − hysteresis. For acoustic reasons, it is recommended that the hysteresis value not be programmed less than 4°C. Setting the hysteresis value lower than 4°C causes the fan to switch on and off regularly when the temperature is close to T_{MIN}.
2. These registers become read-only when the Configuration Register 1 Lock bit is set to 1. Any further attempts to write to these registers have no effect.

Table 73. XNOR TREE TEST ENABLE (Note 1)

Register Address	R/W	Description	Power-On Default
0x6F	R/W	XNOR tree test enable register.	0x00
[0]	XEN	If the XEN bit is set to 1, the device enters the XNOR tree test mode. Clearing the bit removes the device from the XNOR tree test mode.	
[7:1]	Reserved	Unused. Do not write to these bits.	

1. This register becomes read-only when the Configuration Register 1 Lock bit is set to 1. Any further attempts to write to this register have no effect.

Table 74. REMOTE 1 TEMPERATURE OFFSET (Note 1)

Register Address	R/W	Description	Power-On Default
0x70	R/W	Remote 1 temperature offset.	0x00
[7:0]	R/W	Allows a temperature offset to be automatically applied to the Remote Temperature 1 channel measurement. Bit 1 of Configuration Register 5 (0x7C) determines the range and resolution of this register.	

1. This register becomes read-only when the Configuration Register 1 Lock bit is set to 1. Any further attempts to write to this register have no effect.

Table 75. LOCAL TEMPERATURE OFFSET (Note 1)

Register Address	R/W	Description	Power-On Default
0x71	R/W	Local temperature offset.	0x00
[7:0]	R/W	Allows a temperature offset to be automatically applied to the local temperature measurement. Bit 1 of Configuration Register 5 (0x7C) determines the range and resolution of this register.	

1. This register becomes read-only when the Configuration Register 1 Lock bit is set to 1. Any further attempts to write to this register have no effect.

Table 76. REMOTE 2 TEMPERATURE OFFSET (Note 1)

Register Address	R/W	Description	Power-On Default
0x72	R/W	Remote 2 temperature offset.	0x00
[7:0]	R/W	Allows a temperature offset to be automatically applied to the Remote Temperature 2 channel measurement. Bit 1 of Configuration Register 5 (0x7C) determines the range and resolution of this register.	

1. This register becomes read-only when the Configuration Register 1 Lock bit is set to 1. Any further attempts to write to this register have no effect.

Table 77. REGISTER 0x73 – CONFIGURATION REGISTER 2 (POWER-ON DEFAULT = 0x00) (Note 1)

Bit No.	Mnemonic	R/W	Description
0	FanPresDT	R/W	When FanPresenceDT = 1, the state of Bits [3:1] of 0x73 reflects the presence of a 4-wire fan on the appropriate TACH channel.
1	Fan1Detect	Read-only	Fan1Detect = 1 indicates that a 4-wire fan is connected to the TACH1 input.
2	Fan2Detect	Read-only	Fan2Detect = 1 indicates that a 4-wire fan is connected to the TACH2 input.
3	Fan3Detect	Read-only	Fan3Detect = 1 indicates that a 4-wire fan is connected to the TACH3 input.
4	AVG	R/W	AVG = 1 indicates that averaging on the temperature and voltage measurements is turned off. This allows measurements on each channel to be made much faster (x16).
5	ATTN	R/W	ATTN = 1 indicates that the ADT7476A removes the attenuators from the +2.5 V_{IN}, V_{CCP}, +5.0 V_{IN}, and +12 V_{IN} inputs. These inputs can be used for other functions such as connecting up external sensors. It is also possible to remove attenuators from individual channels using Bits [7:4] of Configuration Register 4 (0x7D).
6	CONV	R/W	CONV = 1 indicates that the ADT7476A is put into a single-channel ADC conversion mode. In this mode, the ADT7476A can be made to read continuously from one input only, for example, Remote 1 temperature. The appropriate ADC channel is selected by writing to Bits [7:5] of TACH1 minimum high byte register (0x55). **Bits [7:5], Register 0x55** 000 2.5 V 001 V_{CCP} 010 V_{CC} (3.3 V) 011 5.0 V 100 12 V 101 Remote 1 Temperature 110 Local Temperature 111 Remote 2 Temperature
7	Res		This bit is reserved and should not be changed.

1. This register becomes read-only when the Configuration Register 1 lock bit is set to 1. Any further attempts to write to this register have no effect.

Table 78. REGISTER 0x74 – INTERRUPT MASK REGISTER 1 (POWER-ON DEFAULT [7:0] = 0x00)

Bit No.	Mnemonic	R/W	Description
[0]	2.5 V/$\overline{\text{THERM}}$	R/W	2.5 V/$\overline{\text{THERM}}$ = 1 masks $\overline{\text{SMBALERT}}$ for out-of-limit conditions on the 2.5 V/$\overline{\text{THERM}}$ timer channel.
[1]	V_{CCP}	R/W	V_{CCP} = 1 masks $\overline{\text{SMBALERT}}$ for out-of-limit conditions on the V_{CCP} channel.
[2]	V_{CC}	R/W	V_{CC} = 1 masks $\overline{\text{SMBALERT}}$ for out-of-limit conditions on the V_{CC} channel.
[3]	5.0 V	R/W	5.0 V = 1 masks $\overline{\text{SMBALERT}}$ for out-of-limit conditions on the 5.0 V channel.
[4]	R1T	R/W	R1T = 1 masks $\overline{\text{SMBALERT}}$ for out-of-limit conditions on the Remote 1 temperature channel.
[5]	LT	R/W	LT = 1 masks $\overline{\text{SMBALERT}}$ for out-of-limit conditions on the local temperature channel.
[6]	R2T	R/W	R2T = 1 masks $\overline{\text{SMBALERT}}$ for out-of-limit conditions on the Remote 2 temperature channel.
[7]	OOL	R/W	OOL = 0 when one or more alerts are generated in Interrupt Status Register 2, assuming all the mask bits in the Interrupt Mask Register 2 (0x75) = 1, $\overline{\text{SMBALERT}}$ is still asserted. OOL = 1 when one or more alerts are generated in Interrupt Status Register 2, assuming all the mask bits in the Interrupt Mask Register 2 (0x75) = 1, $\overline{\text{SMBALERT}}$ is not asserted.

Table 79. REGISTER 0x75 – INTERRUPT MASK REGISTER 2 (POWER-ON DEFAULT [7:0] = 0x00)

Bit No.	Mnemonic	R/W	Description
[0]	12 V/VC	R/W	When Pin 21 is configured as a 12 V input, 12 V/VC = 1 masks $\overline{\text{SMBALERT}}$ for out-of-limit conditions on the 12 V channel. When Pin 21 is programmed as VID5, this bit masks an $\overline{\text{SMBALERT}}$, if the VID5 VID code bit changes.
[1]	OVT	R/W	OVT = 1 masks $\overline{\text{SMBALERT}}$ for overtemperature $\overline{\text{THERM}}$ conditions.
[2]	FAN1	R/W	FAN1 = 1 masks $\overline{\text{SMBALERT}}$ for a Fan 1 fault.
[3]	FAN2	R/W	FAN2 = 1 masks $\overline{\text{SMBALERT}}$ for a Fan 2 fault.
[4]	FAN3	R/W	FAN3 = 1 masks $\overline{\text{SMBALERT}}$ for a Fan 3 fault.
[5]	F4P	R/W	If Pin 14 is configured as TACH4, F4P = 1 masks $\overline{\text{SMBALERT}}$ for a Fan 4 fault. If Pin 14 is configured as $\overline{\text{THERM}}$, F4P = 1 masks $\overline{\text{SMBALERT}}$ for an exceeded $\overline{\text{THERM}}$ timer limit. If Pin 14 is configured as GPIO, F4P = 1 masks $\overline{\text{SMBALERT}}$ when GPIO is an input and GPIO is asserted.
[6]	D1	R/W	D1 = 1 masks $\overline{\text{SMBALERT}}$ for a diode open or short on a Remote 1 channel.
[7]	D2	R/W	D2 = 1 masks $\overline{\text{SMBALERT}}$ for a diode open or short on a Remote 2 channel.

Table 80. REGISTER 0x76 – EXTENDED RESOLUTION REGISTER 1 (POWER-ON DEFAULT [7:0] = 0x00) (Note 1)

Bit No.	Mnemonic	R/W	Description
[1:0]	2.5 V	Read-only	2.5 V LSBs. Holds the 2 LSBs of the 10-bit 2.5 V measurement.
[3:2]	V_{CCP}	Read-only	V_{CCP} LSBs. Holds the 2 LSBs of the 10-bit V_{CCP} measurement.
[5:4]	V_{CC}	Read-only	V_{CC} LSBs. Holds the 2 LSBs of the 10-bit V_{CC} measurement.
[7:6]	5.0 V	Read-only	5.0 V LSBs. Holds the 2 LSBs of the 10-bit 5.0 V measurement.

1. If this register is read, this register and the registers holding the MSB of each reading are frozen until read.

Table 81. REGISTER 0x77 – EXTENDED RESOLUTION REGISTER 2 (POWER-ON DEFAULT [7:0] = 0x00) (Note 1)

Bit No.	Mnemonic	R/W	Description
[1:0]	12 V	Read-only	12 V LSBs. Holds the 2 LSBs of the 10-bit 12 V measurement.
[3:2]	TDM1	Read-only	Remote 1 temperature LSBs. Holds the 2 LSBs of the 10-bit Remote 1 temperature measurement.
[5:4]	LTMP	Read-only	Local temperature LSBs. Holds the 2 LSBs of the 10-bit local temperature measurement.
[7:6]	TDM2	Read-only	Remote 2 temperature LSBs. Holds the 2 LSBs of the 10-bit Remote 2 temperature measurement.

1. If this register is read, this register and the registers holding the MSB of each reading are frozen until read.

Table 82. REGISTER 0x78 – CONFIGURATION REGISTER 3 (POWER-ON DEFAULT = 0x00) (Note 1)

Bit No.	Mnemonic	R/W	Description
[0]	ALERT	R/W	ALERT = 1, Pin 10 (PWM2/$\overline{\text{SMBALERT}}$) is configured as an $\overline{\text{SMBALERT}}$ interrupt output to indicate out-of-limit error conditions. ALERT = 0, Pin 10 (PWM2/$\overline{\text{SMBALERT}}$) is configured as the PWM2 output.
[1]	$\overline{\text{THERM}}$/ 2.5V	R/W	$\overline{\text{THERM}}$ = 1 enables $\overline{\text{THERM}}$ functionality on Pin 22 and Pin 14, if Pin 14 is configured as $\overline{\text{THERM}}$, determined by Bits 0 and 1 (PIN14FUNC) of Configuration Register 4. When $\overline{\text{THERM}}$ is asserted, if the fans are running and the BOOST bit is set, then the fans run at full speed. Alternatively, $\overline{\text{THERM}}$ can be programmed so that a timer is triggered to time how long $\overline{\text{THERM}}$ has been asserted. $\overline{\text{THERM}}$ = 0 enables 2.5V measurement on Pin 22 and disables $\overline{\text{THERM}}$. If Bits [5:7] of Configuration Register 5 are set, $\overline{\text{THERM}}$ is bidirectional. If they are 0, $\overline{\text{THERM}}$ is a timer input only. **Pin14FUNC** / **$\overline{\text{THERM}}$/2.5 V** / **Pin 22** / **Pin 14** 00 / 0 / +2.5 V_{IN} / TACH4 01 / 0 / +2.5 V_{IN} / $\overline{\text{THERM}}$ 10 / 0 / +2.5 V_{IN} / $\overline{\text{SMBALERT}}$ 11 / 0 / +2.5 V_{IN} / GPIO6 00 / 1 / $\overline{\text{THERM}}$ / TACH4 01 / 1 / +2.5 V_{IN} / $\overline{\text{THERM}}$ 10 / 1 / $\overline{\text{THERM}}$ / $\overline{\text{SMBALERT}}$ 11 / 1 / $\overline{\text{THERM}}$ / GPIO6
[2]	BOOST	R/W	When $\overline{\text{THERM}}$ is an input and BOOST = 1, assertion of $\overline{\text{THERM}}$ causes all fans to run at the maximum programmed duty cycle for fail-safe cooling.
[3]	FAST	R/W	FAST = 1 enables fast TACH measurements on all channels. This increases the TACH measurement rate from once per second to once every 250 ms (4x).
[4]	DC1	R/W	DC1 = 1 enables TACH measurements to be continuously made on TACH1. Fans must be driven by dc. Setting this bit prevents pulse stretching because it is not required for dc-driven motors.
[5]	DC2	R/W	DC2 = 1 enables TACH measurements to be continuously made on TACH2. Fans must be driven by dc. Setting this bit prevents pulse stretching because it is not required for dc-driven motors.
[6]	DC3	R/W	DC3 = 1 enables TACH measurements to be continuously made on TACH3. Fans must be driven by dc. Setting this bit prevents pulse stretching because it is not required for dc-driven motors.
[7]	DC4	R/W	DC4 = 1 enables TACH measurements to be continuously made on TACH4. Fans must be driven by dc. Setting this bit prevents pulse stretching because it is not required for dc-driven motors.

1. This register become read-only when the Configuration Register 1 Lock bit is set to 1. Any further attempts to write to to this register have no effect.

Table 83. REGISTER 0x79 – $\overline{\text{THERM}}$ TIMER STATUS REGISTER (POWER-ON DEFAULT = 0x00)

Bit No.	Mnemonic	R/W	Description
[7:1]	TMR	Read-only	Times how long $\overline{\text{THERM}}$ input is asserted. These seven bits read 0 until the $\overline{\text{THERM}}$ assertion time exceeds 45.52 ms.
[0]	ASRT/ TMR0	Read-only	This bit is set high on the assertion of the $\overline{\text{THERM}}$ input and is cleared on read. If the $\overline{\text{THERM}}$ assertion time exceeds 45.52 ms, this bit is set and becomes the LSB of the 8-bit TMR reading. This allows $\overline{\text{THERM}}$ assertion times from 45.52 ms to 5.82 sec to be reported back with a resolution of 22.76 ms.

Table 84. REGISTER 0x7A – $\overline{\text{THERM}}$ TIMER LIMIT REGISTER (POWER-ON DEFAULT = 0x00)

Bit No.	Mnemonic	R/W	Description
[7:0]	LIMT	R/W	Sets maximum $\overline{\text{THERM}}$ assertion length allowed before an interrupt is generated. This is an 8-bit limit with a resolution of 22.76 ms allowing $\overline{\text{THERM}}$ assertion limits of 45.52 ms to 5.82 sec to be programmed. If the $\overline{\text{THERM}}$ assertion time exceeds this limit, Bit 5 (F4P) of Interrupt Status Register 2 (0x42) is set. If the limit value is 0x00, an interrupt is generated immediately on the assertion of the $\overline{\text{THERM}}$ input.

Table 85. REGISTER 0x7B – TACH PULSES PER REVOLUTION REGISTER (POWER-ON DEFAULT = 0x55)

Bit No.	Mnemonic	R/W	Description
[1:0]	FAN1	R/W	Sets number of pulses to be counted when measuring Fan 1 speed. Can be used to determine fan pulses per revolution for unknown fan type. **Pulses Counted** 00 = 1 01 = 2 (Default) 10 = 3 11 = 4
[3:2]	FAN2	R/W	Sets number of pulses to be counted when measuring Fan 2 speed. Can be used to determine fan pulses per revolution for unknown fan type. **Pulses Counted** 00 = 1 01 = 2 (Default) 10 = 3 11 = 4
[5:4]	FAN3	R/W	Sets number of pulses to be counted when measuring Fan 3 speed. Can be used to determine fan pulses per revolution for unknown fan type. **Pulses Counted** 00 = 1 01 = 2 (Default) 10 = 3 11 = 4
[7:6]	FAN4	R/W	Sets number of pulses to be counted when measuring Fan 4 speed. Can be used to determine fan pulses per revolution for unknown fan type. **Pulses Counted** 00 = 1 01 = 2 (Default) 10 = 3 11 = 4

Table 86. REGISTER 0x7C − CONFIGURATION REGISTER 5 (POWER-ON DEFAULT = 0x01) (Note 1)

Bit No.	Mnemonic	R/W	Description
[0]	2sC	R/W	2sC = 1 sets the temperature range to the twos complement temperature range. 2sC = 0 changes the temperature range to the Offset 64 temperature range. When this bit is changed, the ADT7476A interprets all relevant temperature register values as defined by this bit.
[1]	Temp Offset	R/W	TempOffset = 0 sets offset range to −63°C to +64°C with 0.5°C resolution. TempOffset = 1 sets offset range to −63°C to +127°C with 1°C resolution. These settings apply to Remote 1, Local, and Remote 2 temperature offset registers (0x70, 0x71, and 0x72).
[2]	GPIO6D	R/W	GPIO6 direction. When GPIO6 function is enabled, this determines whether GPIO6 is an input (0) or an output (1).
[3]	GPIO6P	R/W	GPIO6 polarity. When the GPIO6 function is enabled and is programmed as an output, this bit determines whether the GPIO6 is active low (0) or high (1).
[4]	VID/GPIO	R/W	VID/GPIO = 0 enables VID functionality on Pin 5, Pin 6, Pin 7, Pin 8, and Pin 19. VID/GPIO = 1 enables GPIO functionality on Pin 5, Pin 6, Pin 7, Pin 8, and Pin 19.
[5]	R1 $\overline{\text{THERM}}$	R/W	R1 $\overline{\text{THERM}}$ = 1 enables $\overline{\text{THERM}}$ temperature limit functionality for Remote 1 temperature channel; that is, $\overline{\text{THERM}}$ is bidirectional. R1 $\overline{\text{THERM}}$ = 0 indicates $\overline{\text{THERM}}$ is a timer input only. $\overline{\text{THERM}}$ can also be disabled on any channel by: Writing −64°C to the appropriate $\overline{\text{THERM}}$ temperature limit in Offset 64 mode. Writing −128°C to the appropriate $\overline{\text{THERM}}$ temperature limit in twos complement mode.
[6]	Local $\overline{\text{THERM}}$	R/W	Local $\overline{\text{THERM}}$ = 1 enables $\overline{\text{THERM}}$ temperature limit functionality for local temperature channel; that is, $\overline{\text{THERM}}$ is bidirectional. Local $\overline{\text{THERM}}$ = 0 indicates $\overline{\text{THERM}}$ is a timer input only. $\overline{\text{THERM}}$ can also be disabled on any channel by: Writing −64°C to the appropriate $\overline{\text{THERM}}$ temperature limit in Offset 64 mode. Writing −128°C to the appropriate $\overline{\text{THERM}}$ temperature limit in twos complement mode.
[7]	R2 $\overline{\text{THERM}}$	R/W	R2 $\overline{\text{THERM}}$ = 1 enables $\overline{\text{THERM}}$ temperature limit functionality for Remote 2 temperature channel; that is, $\overline{\text{THERM}}$ is bidirectional. R2 $\overline{\text{THERM}}$ = 0 indicates $\overline{\text{THERM}}$ is a timer input only. $\overline{\text{THERM}}$ can also be disabled on any channel by: Writing −64°C to the appropriate $\overline{\text{THERM}}$ temperature limit in Offset 64 mode. Writing −128°C to the appropriate $\overline{\text{THERM}}$ temperature limit in twos complement mode.

1. This register becomes read-only when the Configuration Register 1 Lock bit is set to 1. Any further attempts to write to this register have no effect.

Table 87. REGISTER 0x7D − CONFIGURATION REGISTER 4 (POWER-ON DEFAULT = 0x00) (Note 1)

Bit No.	Mnemonic	R/W	Description
[1:0]	PIN14FUNC	R/W	These bits set the functionality of Pin 14. 00 = TACH4 (Default) 01 = $\overline{\text{THERM}}$ 10 = $\overline{\text{SMBALERT}}$ 11 = GPIO
[2]	$\overline{\text{THERM}}$ Disable	R/W	$\overline{\text{THERM}}$ Disable = 0 enables $\overline{\text{THERM}}$ overtemperature output assuming $\overline{\text{THERM}}$ is correctly configured (Registers 0x78, 0x7C, and 0x7D). $\overline{\text{THERM}}$ Disable = 1 disables $\overline{\text{THERM}}$ overtemperature output on all channels. $\overline{\text{THERM}}$ can also be disabled on any channel by: Writing −64°C to the appropriate $\overline{\text{THERM}}$ temperature limit in Offset 64 mode. Writing −128°C to the appropriate $\overline{\text{THERM}}$ temperature limit in twos complement mode.
[3]	MaxSpeed $\overline{\text{THERM}}$	R/W	MaxSpeed on $\overline{\text{THERM}}$ = 0 indicates that fans go to full speed when $\overline{\text{THERM}}$ temperature limit is exceeded. MaxSpeed on $\overline{\text{THERM}}$ = 1 indicates that fans go to max speed (0x38, 0x39, 0x3A) when $\overline{\text{THERM}}$ temperature limit is exceeded.
[4]	BpAtt 2.5 V	R/W	Bypass 2.5 V attenuator. When set, the measurement scale for this channel changes from 0 V (0x00) to 2.25 V (0xFF).
[5]	BpAtt V_{CCP}	R/W	Bypass V_{CCP} attenuator. When set, the measurement scale for this channel changes from 0 V (0x00) to 2.25 V (0xFF).
[6]	BpAtt 5.0 V	R/W	Bypass 5.0 V attenuator. When set, the measurement scale for this channel changes from 0 V (0x00) to 2.25 V (0xFF).
[7]	BpAtt 12 V	R/W	Bypass 12 V attenuator. When set, the measurement scale for this channel changes from 0 V (0x00) to 2.25 V (0xFF).

1. This register becomes read-only when the Configuration Register 1 Lock bit is set to 1. Any further attempts to write to this register have no effect.

Table 88. REGISTER 0x7E – MANUFACTURER'S TEST REGISTER 1 (POWER-ON DEFAULT = 0x00)

Bit No.	Mnemonic	R/W	Description
[7:0]	Reserved	Read-only	Manufacturer's test register. These bits are reserved for manufacturer's test purposes and should not be written to under normal operation.

Table 89. REGISTER 0x7F – MANUFACTURER'S TEST REGISTER 2 (POWER-ON DEFAULT = 0x00)

Bit No.	Mnemonic	R/W	Description
[7:0]	Reserved	Read-only	Manufacturer's test register. These bits are reserved for manufacturer's test purposes and should not be written to under normal operation.

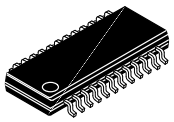
Table 90. ORDERING INFORMATION

Device Order Number*	Package Type	Package Option	Shipping†
ADT7476AARQZ−R	24-lead QSOP	RQ−24	2,500 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
*This is a Pb-Free package.

QSOP24 NB
CASE 492B−01
ISSUE A

DATE 06 MAY 2008



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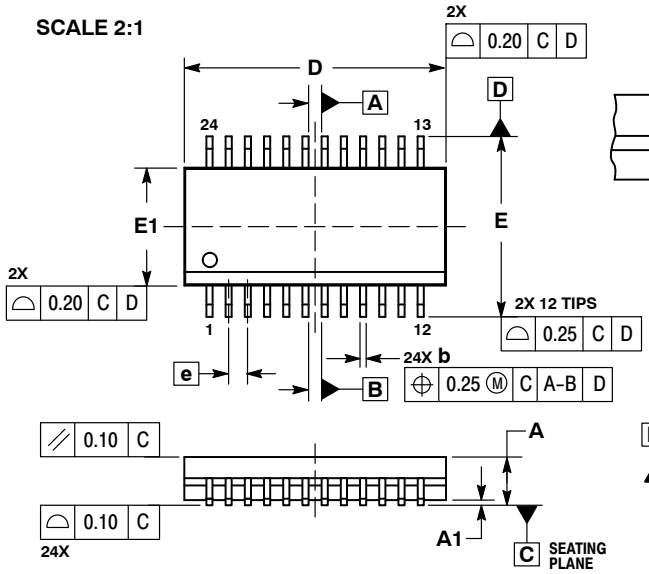
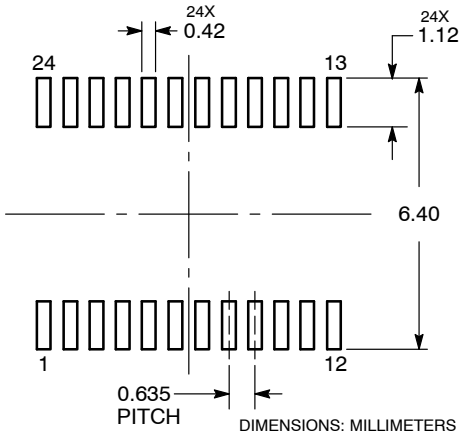


NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION.
4. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.15 PER SIDE. D AND E1 ARE DETERMINED AT DATUM H.
5. DATUMS A AND B ARE DETERMINED AT DATUM H.

	MILLIMETERS	
DIM	MIN	MAX
A	1.35	1.75
A1	0.10	0.25
b	0.20	0.30
C	0.19	0.25
D	8.65 BSC	
E	6.00 BSC	
E1	3.90 BSC	
e	0.635 BSC	
h	0.22	0.50
L	0.40	1.27
L2	0.25 BSC	
M	0 °	8 °

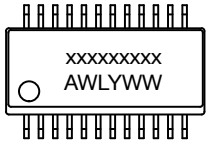
RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



xxx = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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