# CAT5271, CAT5273

# Dual 256-position I²C Compatible Digital Potentiometers (POTs)

The CAT5271 and CAT5273 are dual 256-position digital programmable linear taper potentiometers ideally suited for replacing mechanical potentiometers and variable resistors.

The wiper settings are controlled through an I²C-compatible digital interface. Upon power-up, the wiper assumes a midscale position and may be repositioned anytime after the power is stable. The devices can be programmed to go to a shutdown state during operation.

The CAT5271 and CAT5273 operate from 2.7 V to 5.5 V, while consuming less than 2 μA. This low operating current, combined with a small package footprint, makes them ideal for battery-powered portable applications.

The CAT5271 and CAT5273, designed as pin for pin replacements for the AD5243 and AD5248, are offered in the 10-lead MSOP package and operate over the −40°C to +85°C industrial temperature range.

### Features

- Dual 256-position
- End-to-End Resistance: 50 kΩ, 100 kΩ
- I²C Compatible Interface*
- Power-on Preset to Midscale
- Single Supply 2.7 V to 5.5 V
- Low Temperature Coefficient 100 ppm/°C
- Low Power, $I_{DD}$ 2 μA max
- Wide Operating Temperature −40°C to +85°C
- MSOP−10 Package (3 mm × 4.9 mm)
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

### Typical Applications

- Potentiometer Replacement
- Transducer Adjustment of Pressure, Temperature, Position, Chemical, and Optical Sensors
- RF Amplifier Biasing
- Gain Control and Offset Adjustment

*Two address decode pins (CAT5273 only) allowing multiple devices on the same bus

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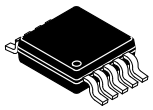
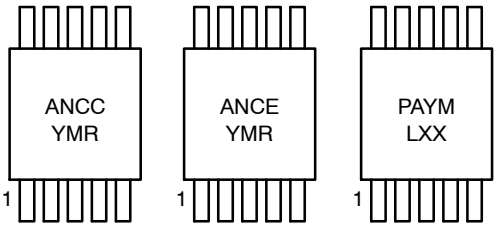


**MSOP−10**
**Z SUFFIX**
**CASE 846AE**

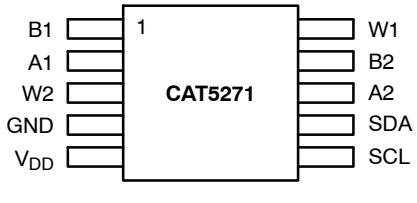
### MARKING DIAGRAMS

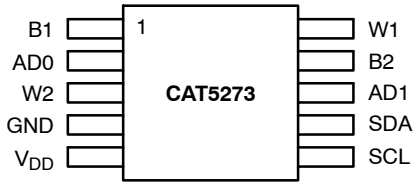



ANCC = CAT5721 − 50 kΩ
ANCE = CAT5721 − 100 kΩ
PA = CAT5273 − 50 kΩ*
Y = Production Year (Last Digit)
M = Production Month (1−9, O, N, D)
R = Revision
L = Assembly Location
XX = Last Two Digits of Assembly Lot Number

*Contact factory for availability of CAT5273 − 100 kΩ

### PIN CONNECTIONS




(Top Views)

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 12 of this data sheet.

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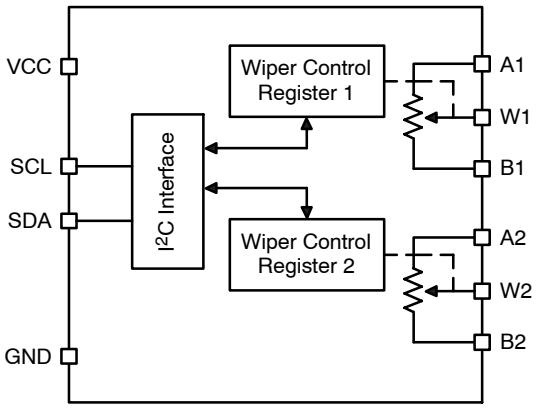



**Figure 1. CAT5271 Functional Block Diagram**

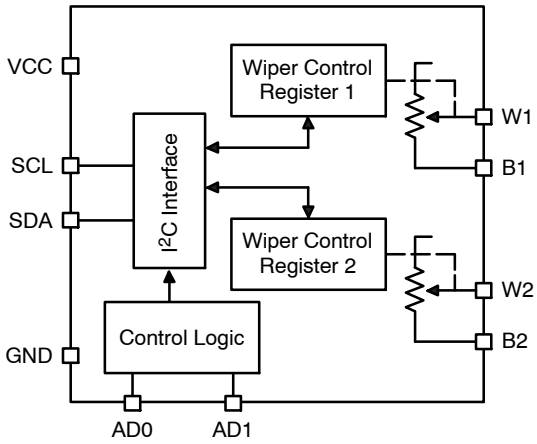



**Figure 2. CAT5273 Functional Block Diagram**

**Table 1. PIN FUNCTION DESCRIPTION**

| | CAT5271 | | CAT5273 | |
|---|---|---|---|---|
| **Pin No.** | **Pin Name** | **Description** | **Pin Name** | **Description** |
| 1 | B1 | B1 Terminal | B1 | B1 Terminal |
| 2 | A1 | A1 Terminal | AD0 | Device Address Bit 0 |
| 3 | W2 | W2 Terminal | W2 | W2 Terminal |
| 4 | GND | Digital Ground | GND | Digital Ground |
| 5 | VDD | Positive Power Supply | VDD | Positive Power Supply |
| 6 | SCL | Serial Clock Input | SCL | Serial Clock Input |
| 7 | SDA | Serial Data Input / Output | SDA | Serial Data Input / Output |
| 8 | A2 | A2 Terminal | AD1 | Device Address Bit 1 |
| 9 | B2 | B2 Terminal | B2 | B2 Terminal |
| 10 | W1 | W1 Terminal | W1 | W1 Terminal |

**Table 2. ABSOLUTE MAXIMUM RATINGS** (Note 1)

| Rating | Value | Unit |
|---|---|---|
| $V_{DD}$ to GND | −0.3 to 6.5 | V |
| A1, B1, W1, A2, B2, W2 Voltage to GND | $V_{DD}$ | |
| $I_{MAX}$ | ±20 | mA |
| Digital Inputs and Output Voltage to GND | 0 to 6.5 | V |
| Operating Temperature Range | −40 to +85 | °C |
| Maximum Junction Temperature ($T_{JMAX}$) | 150 | °C |
| Storage Temperature | −65 to +150 | °C |
| Lead Temperature (Soldering, 10 sec) | 300 | °C |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Maximum terminal current is bounded by the maximum current handling of the switches, maximum power dissipation of the package, and maximum applied voltage across any two of the A, B, and W terminals at a given resistance.

**Table 3. ELECTRICAL CHARACTERISTICS: 50 kΩ and 100 kΩ Versions**

$V_{DD}$ = 2.7 V to 5.5 V; $V_A$ = $V_{DD}$; $V_B$ = 0 V; –40°C < $T_A$ < +85°C; unless otherwise noted. (Note 2)

| Parameter | Test Conditions | Symbol | Min | Typ (Note 3) | Max | Unit |
|---|---|---|---|---|---|---|
| **DC CHARACTERISTICS – RHEOSTAT MODE** | | | | | | |
| Resistor Differential Nonlinearity (Note 4) | $R_{WB}$, $V_A$ = no connection (CAT5271) | R–DNL | –1 | ±0.1 | +1 | LSB |
| Resistor Integral Nonlinearity (Note 4) | $R_{WB}$, $V_A$ = no connection (CAT5271) | R–INL | –2 | ±0.4 | +2 | LSB |
| Nominal Resistor Tolerance (Note 5) | $T_A$ = 25°C | $\Delta R_{AB}$ | –20 | | +20 | % |
| Resistance Temperature Coefficient | $V_{AB}$ = $V_{DD}$, Wiper = no connection | $\Delta R_{AB}/\Delta T$ | | 100 | | ppm/°C |
| Wiper Resistance | $V_{DD}$ = 5 V, $I_W$ = ±3 mA | $R_W$ | | 50 | 120 | Ω |
| | $V_{DD}$ = 3 V, $I_W$ = ±3 mA | | | 100 | 250 | |
| **DC CHARACTERISTICS – POTENTIOMETER DIVIDER MODE** | | | | | | |
| Resolution | | N | | | 8 | Bits |
| Differential Nonlinearity (Note 6) | | DNL | –1 | ±0.1 | +1 | LSB |
| Integral Nonlinearity (Note 6) | | INL | –1 | ±0.4 | +1 | LSB |
| Voltage Divider Temperature Coefficient | Code = 0x80 | $\Delta V_W/\Delta T$ | | 100 | | ppm/°C |
| Full-scale Error | Code = 0xFF | $V_{WFSE}$ | –3 | –1 | 0 | LSB |
| Zero-scale Error | Code = 0x00 | $V_{WZSE}$ | 0 | 1 | 3 | LSB |
| **RESISTOR TERMINALS** | | | | | | |
| Voltage Range (Note 7) | | $V_{A,B,W}$ | GND | | $V_{DD}$ | V |
| Capacitance (Note 8) A, B | f = 1 MHz, measured to GND, Code = 0 x 80 | $C_{A,B}$ | | 45 | | pF |
| Capacitance (Note 8) W | f = 1 MHz, measured to GND, Code = 0 x 80 | $C_W$ | | 60 | | pF |
| Common-mode Leakage (Note 8) | $V_A$ = $V_B$ = $V_{DD}$/2 | $I_{CM}$ | | 1 | | nA |
| **DIGITAL INPUTS** | | | | | | |
| Input Logic High | $V_{DD}$ = 5 V | $V_{IH}$ | 0.7 x $V_{DD}$ | | | V |
| Input Logic Low | $V_{DD}$ = 5 V | $V_{IL}$ | | | 0.3$V_{DD}$ | V |
| Input Logic High | $V_{DD}$ = 3 V | $V_{IH}$ | 0.7 x $V_{DD}$ | | | V |
| Input Logic Low | $V_{DD}$ = 3 V | $V_{IL}$ | | | 0.3$V_{DD}$ | V |
| Input Current | $V_{IN}$ = 0 V or 5 V | $I_{IL}$ | | | ±1 | μA |
| **POWER SUPPLIES** | | | | | | |
| Power Supply Range | | $V_{DD\ RANGE}$ | 2.7 | | 5.5 | V |
| Supply Current | $V_{IH}$ = 5 V or $V_{IL}$ = 0 V | $I_{DD}$ | | 0.3 | 2 | μA |
| Power Dissipation (Note 8) | $V_{IH}$ = 5 V or $V_{IL}$ = 0 V, $V_{DD}$ = 5 V | $P_{DISS}$ | | | 0.2 | mW |
| Power Supply Sensitivity | $\Delta V_{DD}$ = +5 V ±10%, Code = Midscale | PSS | | | ±0.05 | %/% |
| **DYNAMIC CHARACTERISTICS** (Notes 8 and 10) | | | | | | |
| Bandwidth –3 dB | $R_{AB}$ = 50 kΩ / 100 kΩ, Code = 0x80 | BW | | 100/40 | | kHz |
| Total Harmonic Distortion | $V_A$ =1 V rms, $V_B$ = 0 V, f = 1 kHz, $R_{AB}$ = 10 kΩ | $THD_W$ | | 0.05 | | % |
| $V_W$ Settling Time (50 kΩ/100 kΩ) | $V_A$ = 5 V, $V_B$ = 0 V, ±1 LSB error band | $t_S$ | | 2 | | μs |

2. $V_A$ applies to both A1 and A2, $V_B$ applies to both B1 and B2.
3. Typical specifications represent average readings at +25°C and $V_{DD}$ = 5 V.
4. Resistor position nonlinearity error R–INL is the deviation from an ideal value measured between the maximum resistance and the minimum resistance wiper positions. R–DNL measures the relative step change from ideal between successive tap positions. Parts are guaranteed monotonic.
5. CAT5271: $V_{AB}$ = $V_{DD}$, Wiper ($V_W$) = no connect. CAT5273: $V_{WB}$ = $V_{DD}$.
6. INL and DNL are measured at VW with the digital potentiometer configured as a potentiometer divider similar to a voltage output D/A converter. $V_A$ = $V_{DD}$ and $V_B$ = 0 V. DNL specification limits of ±1 LSB maximum are guaranteed monotonic operating conditions.
7. Resistor terminals A, B, W have no limitations on polarity with respect to each other.
8. Guaranteed by design and not subject to production test.
9. Maximum terminal current is bounded by the maximum current handling of the switches, maximum power dissipation of the package, and maximum applied voltage across any two of the A, B, and W terminals at a given resistance.
10. All dynamic characteristics use $V_{DD}$ = 5 V.

**Table 4. CAPACITANCE**
$T_A$ = 25°C, f = 1.0 MHz, $V_{DD}$ = 5 V

| Symbol | Test | Conditions | Max | Units |
|---|---|---|---|---|
| $C_{I/O}$ (Note 11) | Input/Output Capacitance (SDA, SCL) | $V_{I/O}$ = 0 V | 8 | pF |

**Table 5. POWER UP TIMING** (Notes 11 and 12)

| Symbol | Parameter | Max | Units |
|---|---|---|---|
| $t_{PUR}$ | Power-up to Read Operation | 1 | ms |
| $t_{PUW}$ | Power-up to Write Operation | 1 | ms |

11. This parameter is tested initially and after a design or process change that affects the parameter.
12. $t_{PUR}$ and $t_{PUW}$ are delays required from the time $V_{CC}$ is stable until the specified operation can be initiated.

**Table 6. DIGITAL POTENTIOMETER TIMING**

| Symbol | Parameter | Min | Max | Units |
|---|---|---|---|---|
| $t_{WRPO}$ | Wiper Response Time After Power Supply Stable | | 50 | μs |
| $t_{WR}$ | Wiper Response Time: SCL falling edge after last bit of wiper position data byte to wiper change | | 20 | μs |

**Table 7. A.C. CHARACTERISTICS**
$V_{DD}$ = +2.7 V to +5.5 V, −40°C to +85°C unless otherwise specified.

| Symbol | Parameter | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| $f_{SCL}$ | Clock Frequency | | | 400 | kHz |
| $t_{HIGH}$ | Clock High Period | 600 | | | ns |
| $t_{LOW}$ | Clock Low Period | 1300 | | | ns |
| $t_{SU:STA}$ | Start Condition Setup Time (for a Repeated Start Condition) | 600 | | | ns |
| $t_{HD:STA}$ | Start Condition Hold Time | 600 | | | ns |
| $t_{SU:DAT}$ | Data in Setup Time | 100 | | | ns |
| $t_{HD:DAT}$ | Data in Hold Time | 0 | | | ns |
| $t_{SU:STO}$ | Stop Condition Setup Time | 600 | | | ns |
| $t_{BUF}$ | Time the bus must be free before a new transmission can start | 1300 | | | ns |
| $t_R$ | SDA and SCL Rise Time | | | 300 | ns |
| $t_F$ | SDA and SCL Fall Time | | | 300 | ns |
| $t_{DH}$ | Data Out Hold Time | | 100 | | ns |
| $T_I$ | Noise Suppression Time Constant at SCL, SDA Inputs | | | 50 | ns |
| $t_{AA}$ | SCL Low to SDA Data Out and ACK Out | | | 1 | μs |

## TYPICAL CHARACTERISTICS

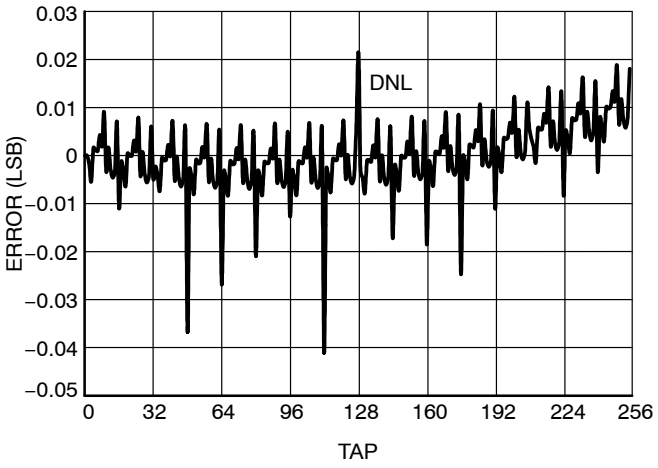



**Figure 3. Potentiometer Divider Differential Non-linearity, $V_{DD}$ = 5.6 V**

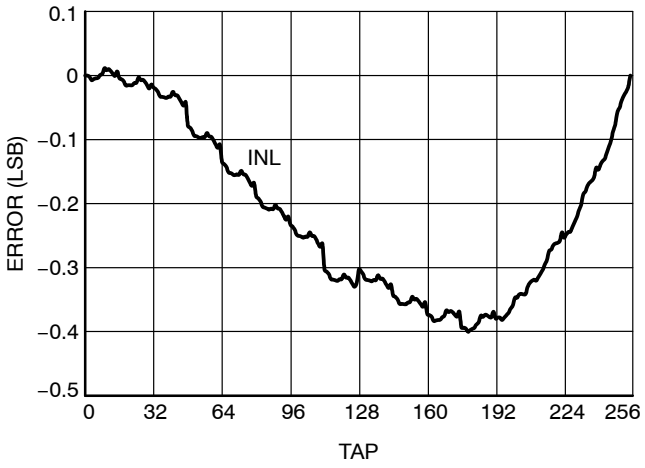



**Figure 4. Potentiometer Divider Integral Non-linearity, $V_{DD}$ = 5.6 V**

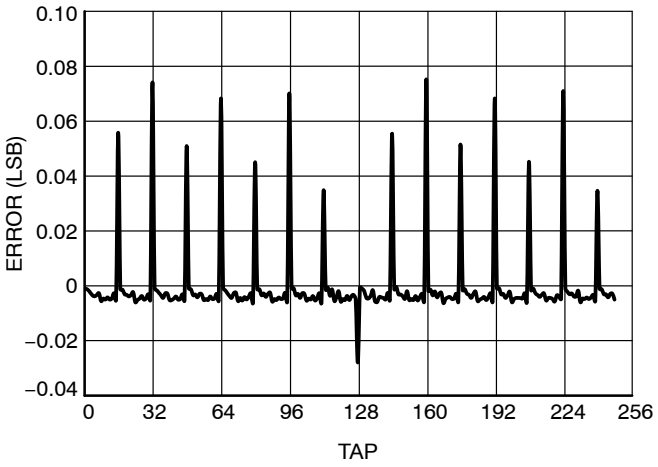



**Figure 5. Rheostat Differential Non-linearity, $V_{DD}$ = 5.6 V**

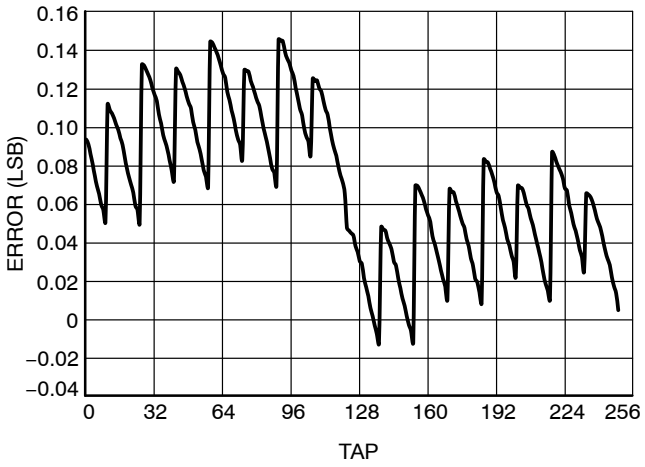



**Figure 6. Rheostat Integral Non-linearity, $V_{DD}$ = 5.6 V**

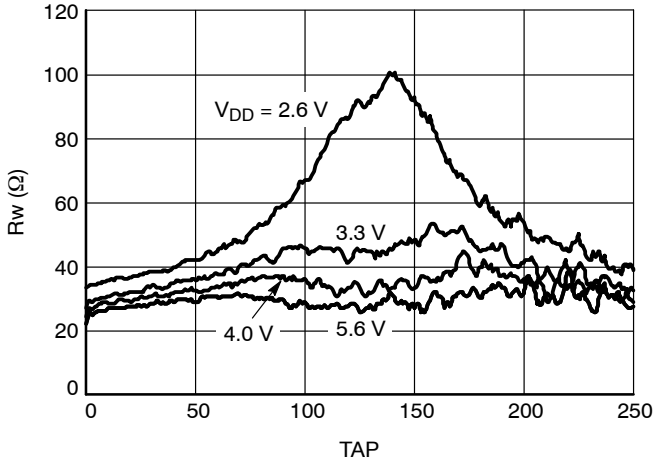



**Figure 7. Wiper Resistance at Room Temperature**

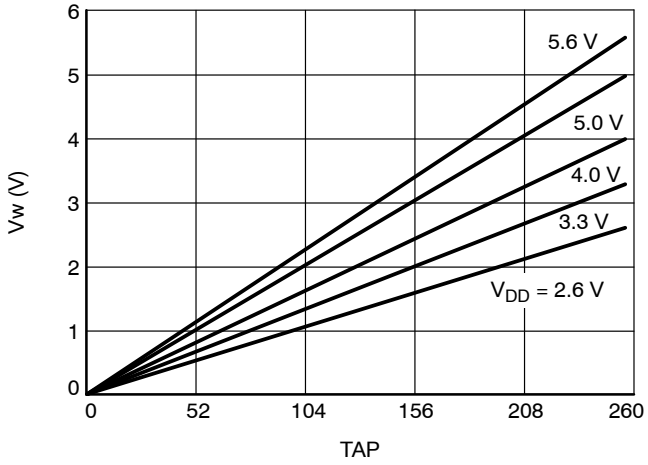



**Figure 8. Wiper Voltage**

## TYPICAL CHARACTERISTICS

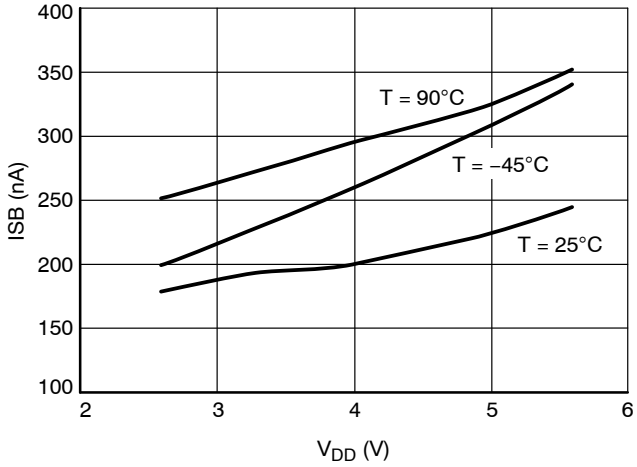



**Figure 9. Standby Current**

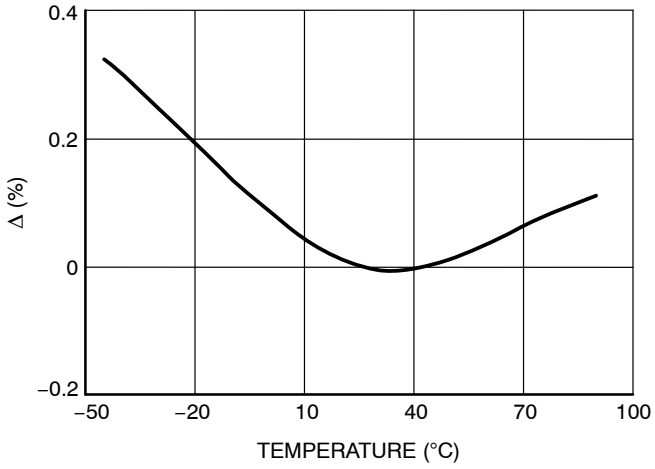



**Figure 10. Change in End-to-End Resistance**

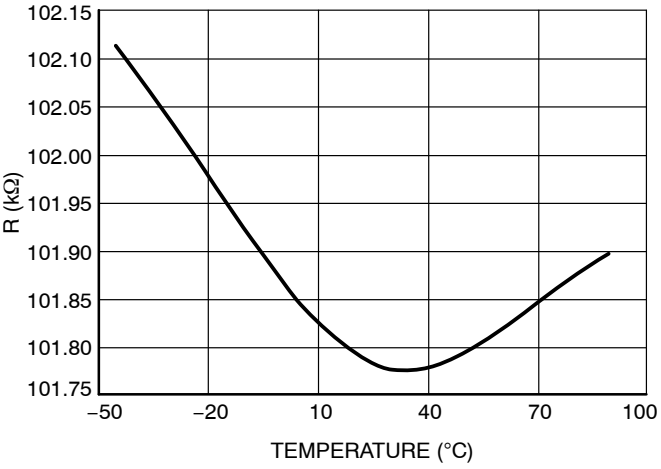



**Figure 11. End-to-End Resistance vs. Temperature**

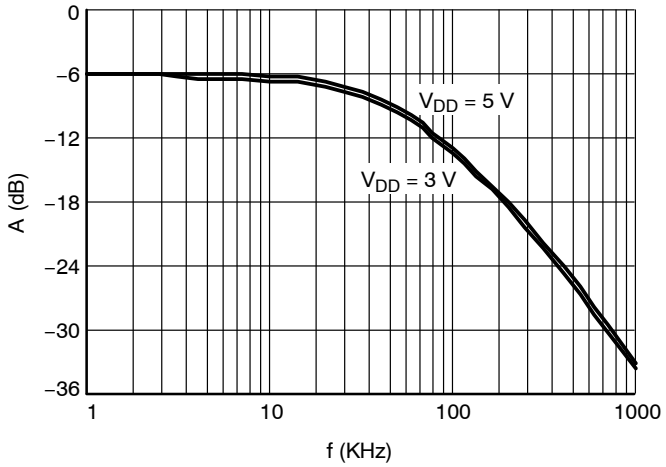



**Figure 12. Gain vs. Bandwidth (Tap 0x80)**

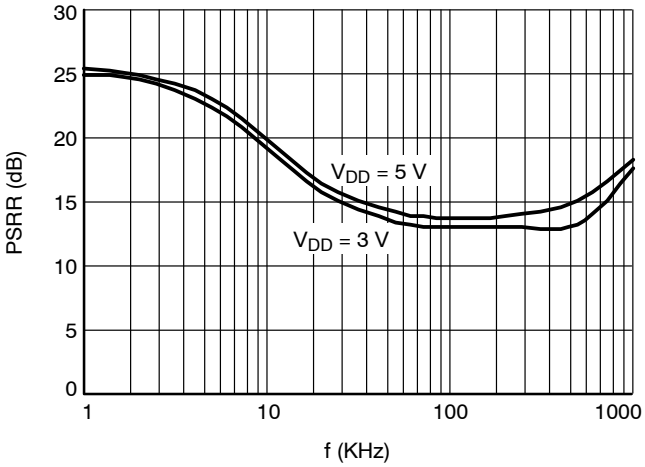



**Figure 13. PSRR**

## BASIC OPERATION

The CAT5271 and CAT5273 are dual 256-position digitally controlled potentiometers. When power is first applied, the wipers assume a mid-scale position. Once the power supply is stable, the wipers may be repositioned via the $I^2C$ compatible interface.

## PROGRAMMING: VARIABLE RESISTOR

### Rheostat Mode

(The following section refers to CAT5271. The behavior of CAT5273 is identical, but for this device terminal A of the resistor is not accessible.)

The resistance between terminals A and B, $R_{AB}$, has a nominal value of 50 kΩ or 100 kΩ and has 256 contact points accessed by the wiper terminal, plus the B terminal contact. Data in the 8-bit Wiper register is decoded to select one of these 256 possible settings.

The wiper's first connection is at the B terminal, corresponding to control position 0x00. Ideally this would present a 0 Ω between the Wiper and B, but just as with a mechanical rheostat there is a small amount of contact resistance to be considered, there is a wiper resistance comprised of the $R_{ON}$ of the FET switch connecting the wiper output with its respective contact point. In CAT5271/CAT5273 this 'contact' resistance is typically 50 Ω. Thus a connection setting of 0x00 yields a minimum resistance of 50 Ω between terminals W and B.

For a 100 kΩ device, the second connection, or the first tap point, corresponds to 441 Ω ($R_{WB} = R_{AB}/256 + R_W = 390.6 + 50$ Ω) for data 0x01. The third connection is the next tap point, is 831 Ω (2 x 390.6 + 50 Ω) for data 0x02, and so on. Figure 14 shows a simplified equivalent circuit where the last resistor string will not be accessed; therefore, there is 1 LSB less of the nominal resistance at full scale in addition to the wiper resistance.

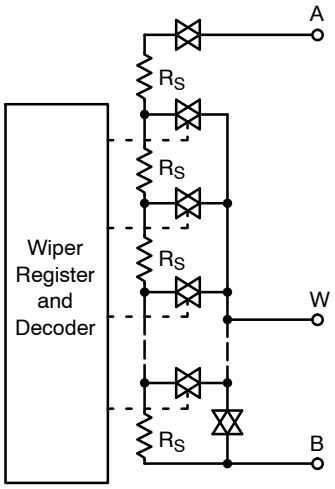



**Figure 14. CAT5271 Equivalent Digital POT Circuit**

The equation for determining the digitally programmed output resistance between W and B is

$$R_{WB} = \frac{D}{256} R_{AB} + R_W \qquad \text{(eq. 1)}$$

where D is the decimal equivalent of the binary code loaded in the 8-bit Wiper register, $R_{AB}$ is the end-to-end resistance, and $R_W$ is the wiper resistance contributed by the on resistance of the internal switch.

In summary, if $R_{AB}$ = 100 kΩ and the A terminal is open circuited, the following output resistance $R_{WB}$ will be set for the indicated Wiper register codes:

**Table 8. CODES AND CORRESPONDING $R_{WB}$ RESISTANCE FOR $R_{AB}$ = 100 kΩ, $V_{DD}$ = 5 V**

| D (Dec.) | $R_{WB}$ (Ω) | Output State |
|---|---|---|
| 255 | 99,559 | Full Scale ($R_{AB}$ – 1 LSB + $R_W$) |
| 128 | 50,050 | Midscale |
| 1 | 441 | 1 LSB |
| 0 | 50 | Zero Scale (Wiper Contact Resistance) |

Be aware that in the zero-scale position, the wiper resistance of 50 Ω is still present. Current flow between W and B in this condition should be limited to a maximum pulsed current of no more than 20 mA. Failure to heed this restriction can cause degradation or possible destruction of the internal switch contact.

Similar to the mechanical potentiometer, the resistance of the digital POT between the wiper W and terminal A also produces a digitally controlled complementary resistance $R_{WA}$. When these terminals are used, the B terminal can be opened. Setting the resistance value for $R_{WA}$ starts at a maximum value of resistance and decreases as the data loaded in the latch increases in value. The general equation for this operation is

$$R_{WA}(D) = \frac{256 - D}{256} R_{AB} + R_W \qquad \text{(eq. 2)}$$

For $R_{AB}$ = 100 kΩ and the B terminal open circuited, the following output resistance $R_{WA}$ will be set for the indicated Wiper register codes.

**Table 9. CODES AND CORRESPONDING $R_{WA}$ RESISTANCE FOR $R_{AB}$ = 100 kΩ, $V_{DD}$ = 5 V**

| D (Dec.) | $R_{WA}$ (Ω) | Output State |
|---|---|---|
| 255 | 441 | Full Scale |
| 128 | 50,050 | Midscale |
| 1 | 99,659 | 1 LSB |
| 0 | 100,050 | Zero Scale |

Typical device to device resistance matching is lot dependent and may vary by up to ±20%.

### ESD Protection

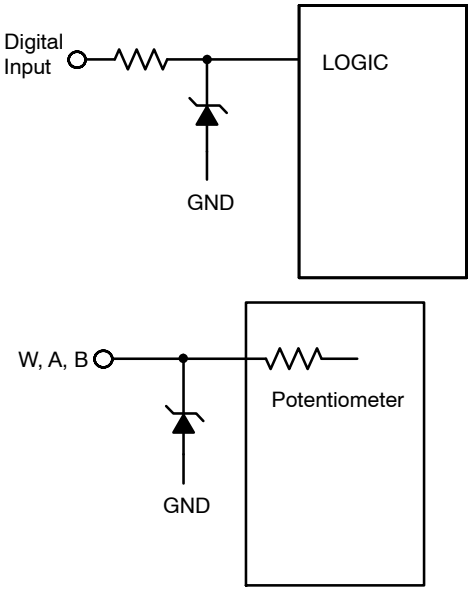



**Figure 15. ESD Protection Networks**

### Terminal Voltage Operating Range

The CAT5271/CAT5273 $V_{DD}$ and GND power supply define the limits for proper 3-terminal digital potentiometer operation. Signals or potentials applied to terminals A, B or the wiper must remain inside the span of $V_{DD}$ and GND. Signals which attempt to go outside these boundaries will be clamped by the internal forward biased diodes.

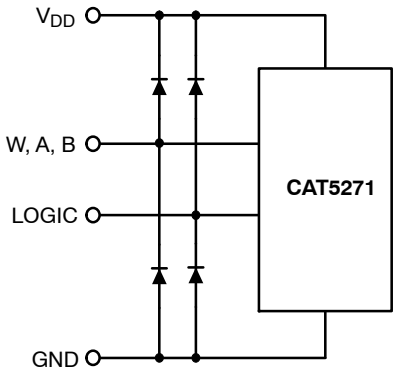



**Figure 16.**

### Power-up Sequence

Because ESD protection diodes limit the voltage compliance at terminals A, B, and W (see Figure 15), it is recommended that $V_{DD}$/GND be powered before applying any voltage to terminals A, B, and W. The ideal power-up sequence is: GND, $V_{DD}$, digital inputs, and then $V_{A/B/W}$. The order of powering $V_A$, $V_B$, $V_W$, and the digital inputs is not important as long as they are powered after $V_{DD}$/GND.

### Power Supply Bypassing

Good design practice employs compact, minimum lead length layout design. Leads should be as direct as possible. It is also recommended to bypass the power supplies with quality low ESR Ceramic chip capacitors of 0.01 μF to 0.1 μF. Low ESR 1 μF to 10 μF tantalum or electrolytic capacitors can also be applied at the supplies to suppress transient disturbances and low frequency ripple. As a further precaution digital ground should be joined remotely to the analog ground at one point to minimize the ground bounce.

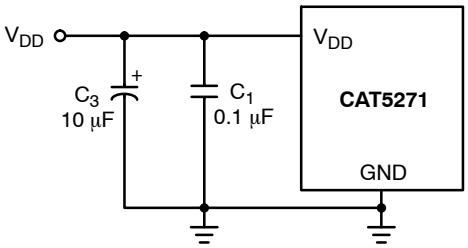



**Figure 17. Power Supply Bypassing**

## I²C BUS PROTOCOL

The following defines the features of the I²C bus protocol:

1. Data transfer may be initiated only when the bus is not busy.
2. During a data transfer, the data line must remain stable whenever the clock line is high. Any changes in the data line while the clock is high will be interpreted as a START or STOP condition.

The device controlling the transfer is a master, typically a processor or controller, and the device being controlled is the slave. The master will always initiate data transfers and provide the clock for both transmit and receive operations. Therefore, CAT5271/CAT5273 will be considered a slave device in all applications.

### START Condition

The START condition precedes all commands to the device, and is defined as a high to low transition of SDA when SCL is high. The CAT5271/CAT5273 monitors the SDA and SCL lines and will not respond until this condition is met.

### STOP Condition

A low to high transition of SDA when SCL is high determines the STOP condition. All operations must end with a STOP condition.

## DEVICE ADDRESSING

The bus Master begins a transmission by sending a START condition. The Master then sends the address of the particular slave device it is requesting. The seven most significant bits of the 8-bit slave address are fixed as 0101111 for the CAT5271. For CAT5273 the first five bits are fixed as 01011, and the next two bits are pin-programmable device address bits (AD1 and AD0). The next bit ($R/\overline{W}$) selects between the type of the instruction Read or Write. If the bit is logic high, then a Read instruction is performed. If the bit is logic low, then the Write command is executed.

After the Master sends a START condition and the slave address byte, the CAT5271/CAT5273 monitors the bus and responds with an acknowledge (on the SDA line) when its address matches the transmitted slave address.

### Acknowledge

After a successful data transfer, each receiving device is required to generate an acknowledge. The Acknowledging device pulls down the SDA line during the ninth clock cycle, signaling that it received the 8 bits of data.

The CAT5271/CAT5273 responds with an acknowledge after receiving a START condition and its slave address. If the device has been selected along with a write operation, it responds with an acknowledge after receiving each 8-bit byte.

When the CAT5271/CAT5273 is in a READ mode it transmits 8 bits of data, releases the SDA line, and monitors the line for an acknowledge. Once it receives this acknowledge, the CAT5271/CAT5273 will continue to transmit data. If no acknowledge is sent by the Master, the device terminates data transmission and waits for a STOP condition.

## WRITE OPERATION

In the Write mode, the Master device sends the START condition and the slave address information to the Slave device. After the Slave generates an acknowledge, the Master sends the instruction byte. After receiving another acknowledge from the Slave, the Master device transmits the data to be written into the wiper register. The CAT5271/CAT5273 acknowledges once more and the Master generates the STOP condition.

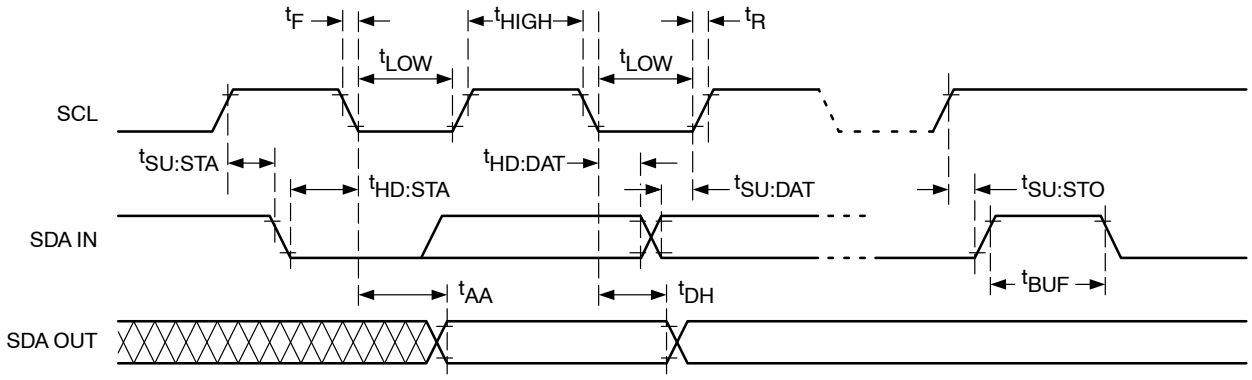



**Figure 18. Bus Timing Diagram**

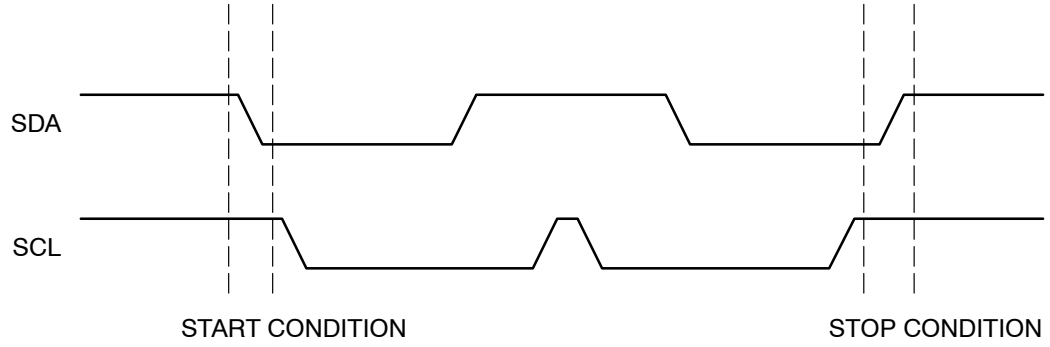



**Figure 19. Start/Stop Condition**

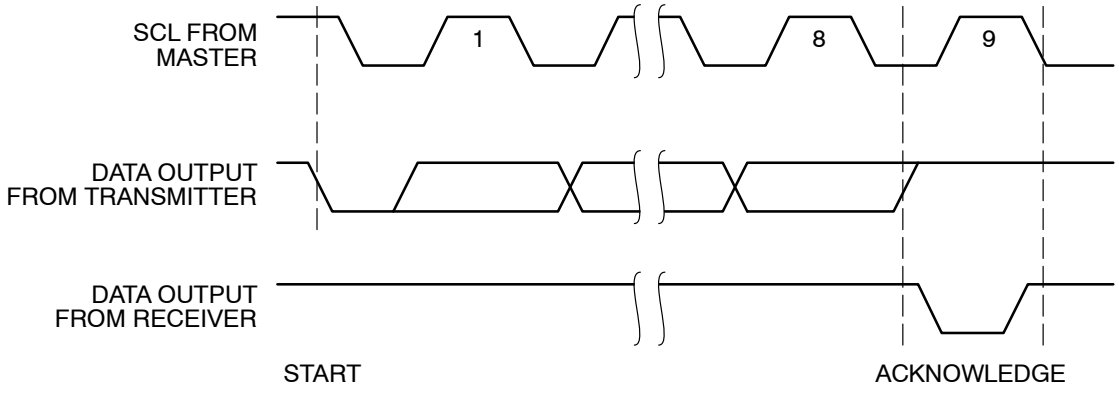



**Figure 20. Acknowledge Condition**

## INSTRUCTION AND REGISTER DESCRIPTION

### Slave Address Byte

The first byte sent to the CAT5271 from the master/processor is called the Slave Address Byte. The most significant seven bits of the slave address are a device type identifier. For the CAT5271, these bits are fixed at 0101111. For CAT5273, the first five bits are fixed as 01011, and the next two bits of the device identifier are determined by the logic levels on the AD1 and AD0 pins. The following bit ($R/\overline{W}$) selects between a Read or a Write operation. If the bit is logic high, then a Read instruction is performed. If the bit is low, then the Write command is executed.

### Instruction Byte

Write and Read instructions are respectively three and two bytes in length. The basic sequence of the two instructions is illustrated in Table 10 and 11.

### Write Operation

In the write instruction, the second byte first bit (A0) selects between the potentiometer 1 and 2: a logic low is for the potentiometer 1, and a logic high is for potentiometer 2.

The following bit (SD) is the shutdown bit. A logic high causes an open circuit at terminal A while shorting the wiper terminal W to terminal B. The “shutdown” operation does not change the contents of the wiper register. When the shutdown bit, SD, goes back to a logic low, the previous wiper position is restored. Also during shutdown, new settings can be programmed. As soon as the device is returned from shutdown, the wiper position is set according to the wiper register value.

The remainder of the bits in the instruction byte are don’t care bits.

### Read Operation

In the read mode, the data byte follows immediately after the acknowledgment of the slave address byte. Data is transmitted over the serial bus in sequences.

There is no potentiometer channel selection bit in the Read command. The addressed channel is the one that is previously selected in the write mode. If it desired to read the potentiometer wiper register values of both channels, the first potentiometer must be addressed in write mode and then change to read mode to read the first channel value. After that, the user must return the device to write mode with the second potentiometer selected and read the second potentiometer wiper register value in read mode. It is not necessary for users to issue the third data byte in write mode for subsequent read operation.

### Wiper Control

The CAT5271/CAT5273 contains two 8-bit Wiper Control Register (WCR). The Wiper Control Register output is decoded to select one of 256 switches along its resistor array. The contents of the WCR may be written by the host via Write instruction.

The Wiper Control Registers are a volatile register that loses its contents when the CAT5271/CAT5273 is powered-down. Upon power-up, the wiper is set to midscale and may be repositioned anytime after the power has become stable.

**Table 10. CAT5271 Write**

| S | 0 | 1 | 0 | 1 | 1 | 1 | 1 | $\overline{W}$ | A | A0 | SD | X | X | X | X | X | X | A | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | A | P |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Slave Address Byte | | | | | | | | | Instruction Byte | | | | | | | | | Data Byte | | | | | | | | | |

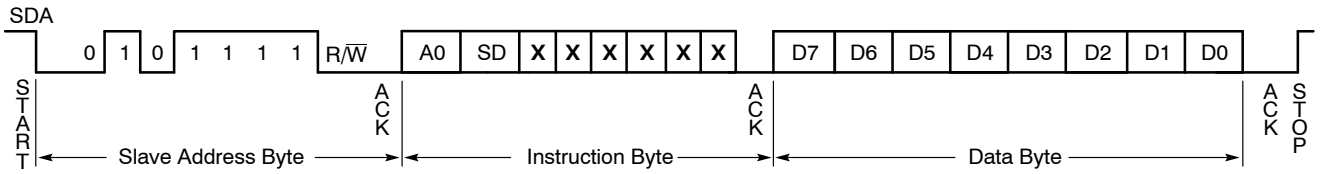
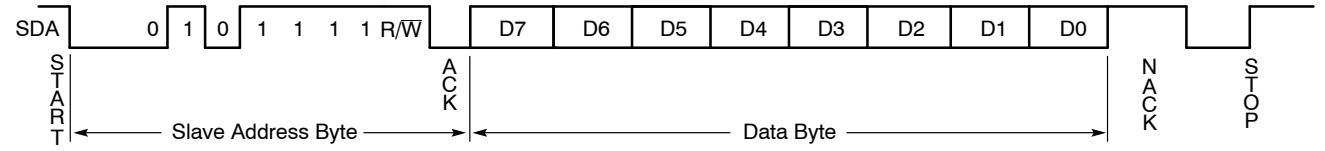



**Table 11. CAT5271 READ**

| S | 0 | 1 | 0 | 1 | 1 | 1 | 1 | R | A | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | A | P |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Slave Address Byte | | | | | | | | | Data Byte | | | | | | | | | |




**Legend**

| | | | |
|---|---|---|---|
| S = | Start | A0 = | Potentiometer Channel (1 or 2) Select Bit |
| P = | Stop | SD = | Shut Down: |
| A = | Acknowledge | | 0: normal operation |
| D = | Data bit | | 1: wiper is parked at B terminal and |
| R = | Read (bit is 1 for Read instruction) | | terminal A is open circuit. |
| $\overline{W}$ = | Write (bit is 0 for Write instruction) | X = | Don’t Care |

**Table 12. CAT5273 Write**

| S | 0 | 1 | 0 | 1 | 1 | AD1 | AD0 | $\overline{W}$ | A | A0 | SD | X | X | X | X | X | X | A | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | A | P |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Slave Address Byte | | | | | | | | | Instruction Byte | | | | | | | | | Data Byte | | | | | | | | | |

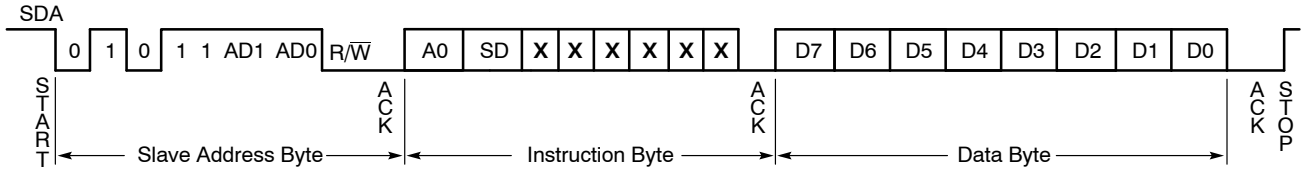
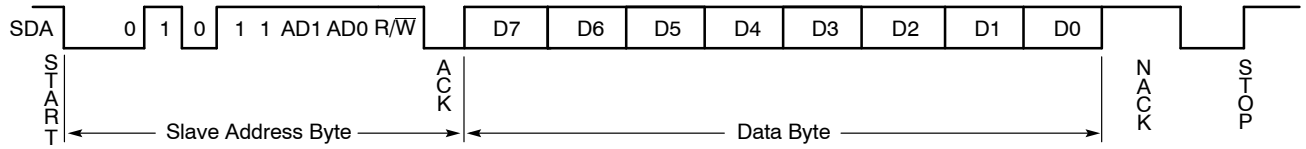



**Table 13. CAT5273 READ**

| S | 0 | 1 | 0 | 1 | 1 | AD1 | AD0 | R | A | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | A | P |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Slave Address Byte | | | | | | | | | Data Byte | | | | | | | | | |




**Legend**

| | | | |
|---|---|---|---|
| S = | Start | SD = | Shut Down: |
| P = | Stop | | 0: normal operation |
| A = | Acknowledge | | 1: wiper is parked at B terminal |
| D = | Data bit | | and terminal A is open circuit. |
| R = | Read (bit is 1 for Read instruction) | X = | Don't Care |
| $\overline{W}$ = | Write (bit is 0 for Write instruction) | AD1, AD0 = | Bits that must match the logic levels |
| A0 = | Potentiometer Channel (1 or 2) Select Bit | | on pins AD1 and AD0 |

**Table 14. ORDERING PART NUMBER**

| Part Number | Resistance | Package | Lead Finish | Shipping† |
|---|---|---|---|---|
| CAT5271ZI−50−GT3 | 50 kΩ | MSOP−10 | NiPdAu | 3000 / Tape & Reel |
| CAT5271ZI−00−GT3 | 100 kΩ | | | 3000 / Tape & Reel |
| CAT5273ZI−50−GT3 | 50 kΩ | MSOP−10 | NiPdAu | 3000 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

13. For detailed information and a breakdown of device nomenclature and numbering systems, please see the ON Semiconductor Device Nomenclature document, TND310/D, available at www.onsemi.com.
14. All packages are RoHS-compliant (Lead-free, Halogen-free).

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