CS5165A

5-Bit Synchronous CPU Buck Controller

The CS5165A synchronous 5−bit NFET buck controller is optimized to manage the power of the next generation Pentium II processors. It's V^2 ™ control architecture delivers the fastest transient response (100 ns), and best overall voltage regulation in the industry today. It's feature rich design gives end users the maximum flexibility to implement the best price/performance solutions for their end products.

The CS5165A has been carefully crafted to maximize performance and protect the processor during operation. It has a 5−bit DAC on board that holds a ±1.0% tolerance over temperature. Its on board programmable Soft−Start insures a control startup, and the FET nonoverlap circuitry ensures that both FETs do not conduct simultaneously.

The on board oscillator can be programmed up to 1.0 MHz to give the designer maximum flexibility in choosing external components and setting systems costs.

The CS5165A protects the processor during potentially catastrophic events like overvoltage (OVP) and short circuit. The OVP feature is part of the V^2 architecture and does not require any additional components. During short circuit, the controller pulses the MOSFETs in a "hiccup" mode (3.0% duty cycle) until the fault is removed. With this method, the MOSFETs do not overheat or self destruct.

The CS5165A is designed for use in both single processor desktop and multiprocessor workstation and server applications. The CS5165A's current sharing capability allows the designer to build multiple parallel and redundant power solutions for multiprocessor systems.

The CS5165A contains other control and protection features such as Power Good, ENABLE, and adaptive voltage positioning. It is available in a 16 lead SOIC wide body package.

Features

- V^2 Control Topology
- Dual N−Channel Design
- 100 ns Controller Transient Response
- Excess of 1.0 MHz Operation
- 5−Bit DAC with 1.0% Tolerance
- Power Good Output With Internal Delay
- Enable Input Provides Micropower Shutdown Mode
- 5.0 V and 12 V Operation
- Adaptive Voltage Positioning
- Remote Sense Capability
- Current Sharing Capability
- V_{CC} Monitor
- Hiccup Mode Short Circuit Protection
- Overvoltage Protection (OVP)
- Programmable Soft−Start
- 150 ns PWM Blanking
- 65 ns FET Nonoverlap Time
- 40 ns Gate Rise and Fall Times (3.3 nF Load)
- Pb−Free Packages are Available*

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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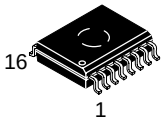
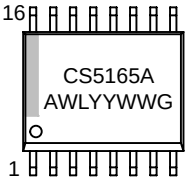
MARKING DIAGRAM

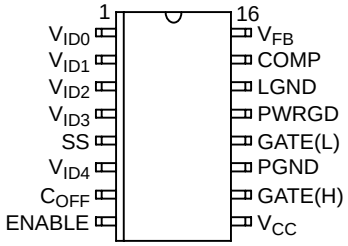


SO−16WB
DW SUFFIX
CASE 751G



CS5165A	= Device Code
A	= Assembly Location
WL	= Wafer Lot
YY	= Year
WW	= Work Week
G	= Pb−Free Package

PIN CONNECTIONS



ORDERING INFORMATION

Device	Package	Shipping†
CS5165AGDW16	SOIC−16	47 Units/Rail
CS5165AGDW16G	SOIC−16 (Pb−Free)	47 Units/Rail
CS5165AGDWR16	SOIC−16	1000/Tape & Reel
CS5165AGDWR16G	SOIC−16 (Pb−Free)	1000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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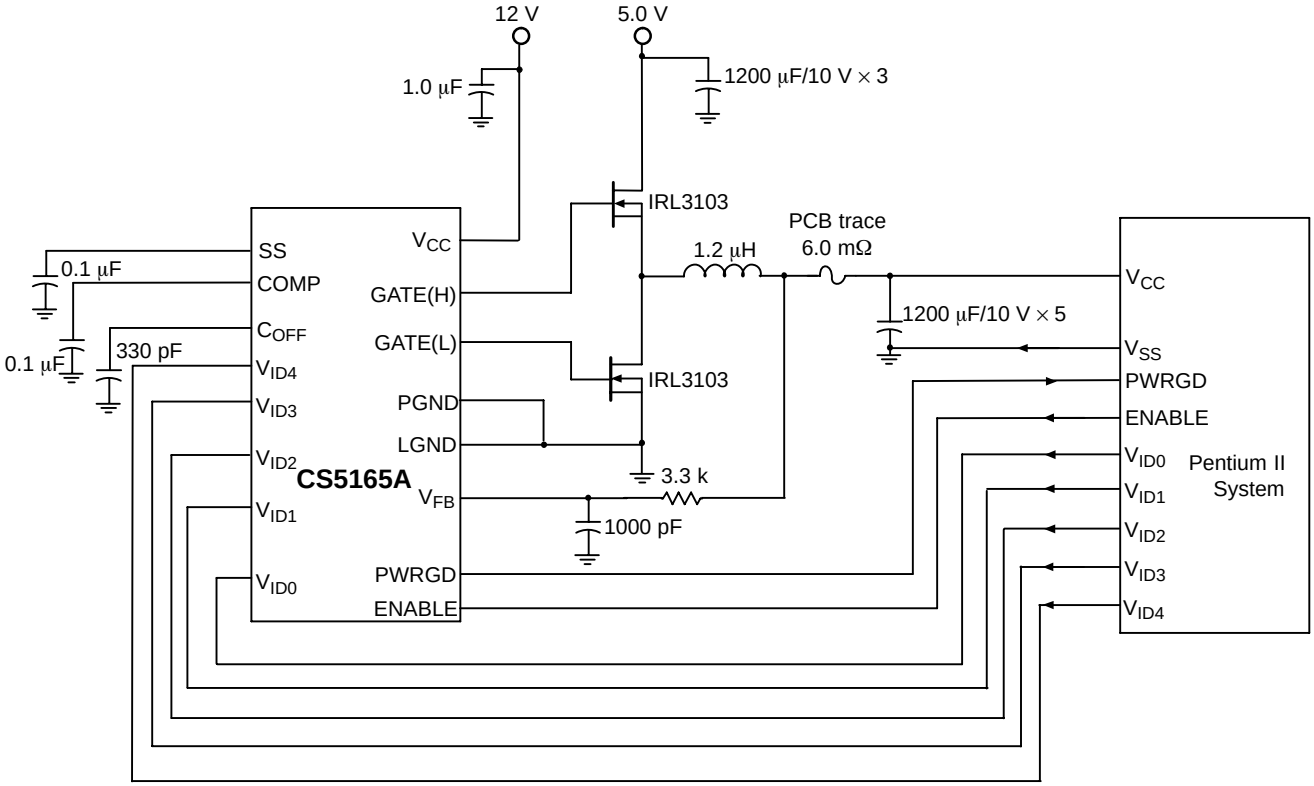


Figure 1. Application Diagram, 5.0 V to 2.8 V @ 14.2 A for 300 MHz Pentium II

MAXIMUM RATINGS

Rating		Value	Unit
Operating Junction Temperature, T_J		0 to 150	°C
Lead Temperature Soldering:	Reflow: (SMD styles only) (Note 1)	230 peak	°C
Storage Temperature Range, T_S		−65 to +150	°C
ESD Susceptibility (Human Body Model)		2.0	kV

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. 60 second maximum above 183°C.

MAXIMUM RATINGS

Pin Name	Pin Symbol	V_{MAX}	V_{MIN}	I_{SOURCE}	I_{SINK}
IC Power Input	V_{CC}	16 V	−0.3 V	N/A	1.5 A peak, 200 mA DC
Soft−Start Capacitor	SS	6.0 V	−0.3 V	200 μA	10 μA
Compensation Capacitor	COMP	6.0 V	−0.3 V	10 mA	1.0 mA
Voltage Feedback Input	V_{FB}	6.0 V	−0.3 V	10 μA	10 μA
Off−Time Capacitor	C_{OFF}	6.0 V	−0.3 V	1.0 mA	50 mA
Voltage ID DAC Inputs	V_{ID0}−V_{ID4}	6.0 V	−0.3 V	1.0 mA	10 μA
High−Side FET Driver	GATE(H)	16 V	−0.3 V	1.5 A peak, 200 mA DC	1.5 A peak, 200 mA DC
Low−Side FET Driver	GATE(L)	16 V	−0.3 V	1.5 A peak, 200 mA DC	1.5 A peak, 200 mA DC
Enable Input	ENABLE	6.0 V	−0.3 V	100 μA	1.0 mA
Power Good Output	PWRGD	6.0 V	−0.3 V	10 μA	30 mA
Power Ground	PGND	0 V	0 V	1.5 A peak, 200 mA DC	N/A
Logic Ground	LGND	0 V	0 V	100 mA	N/A

ELECTRICAL CHARACTERISTICS ($0°C < T_A < +70°C$; $0°C < T_J < +125°C$; $8.0\ V < V_{CC} < 14\ V$; 2.8 DAC Code: ($V_{ID4} = V_{ID2} = V_{ID1} = V_{ID0} = 1$; $V_{ID3} = 0$); $C_{GATE(H)}$ and $C_{GATE(L)} = 3.3$ nF; $C_{OFF} = 330$ pF; $C_{SS} = 0.1$ μF, unless otherwise specified.)

Characteristic	Test Conditions	Min	Typ	Max	Unit
V_{CC} Supply Current					
Operating	$1.0\ V < V_{FB} < V_{DAC}$ (max on−time) No Loads on GATE(H) and GATE(L)	−	12	20	mA
Sleep Mode	ENABLE = 0 V	−	300	600	μA
V_{CC} Monitor					
Start Threshold	GATE(H) switching	3.75	3.95	4.15	V
Stop Threshold	GATE(H) not switching	3.65	3.87	4.05	V
Hysteresis	Start−Stop	−	80	−	mV
Error Amplifier					
V_{FB} Bias Current	$V_{FB} = 0$ V	−	0.1	1.0	μA
COMP Source Current	COMP = 1.2 V to 3.6 V; $V_{FB} = 2.7$ V	15	30	60	μA
COMP CLAMP Voltage	$V_{FB} = 2.7$ V, Adjust COMP voltage for Comp current = 50 μA	0.85	1.0	1.15	V
COMP Clamp Current	COMP = 0 V	0.4	1.0	1.6	mA
COMP Sink Current	$V_{COMP} = 1.2$ V; $V_{FB} = 3.0$ V; $V_{SS} > 2.5$ V	180	400	800	μA
Open Loop Gain	(Note 2)	50	60	−	dB
Unity Gain Bandwidth	(Note 2)	0.5	2.0	−	MHz
PSRR @ 1.0 kHz	(Note 2)	60	85	−	dB
GATE(H) and GATE(L)					
High Voltage at 100 mA	Measure V_{CC} − GATE	−	1.2	2.0	V
Low Voltage at 100 mA	Measure GATE	−	1.0	1.5	V
Rise Time	$1.6\ V < GATE < (V_{CC} - 2.5\ V)$	−	40	80	ns
Fall Time	$(V_{CC} - 2.5\ V) > GATE > 1.6$ V	−	40	80	ns
GATE(H) to GATE(L) Delay	GATE(H) < 2.0 V; GATE(L) > 2.0 V	30	65	100	ns
GATE(L) to GATE(H) Delay	GATE(L) < 2.0 V; GATE(H) > 2.0 V	30	65	100	ns
GATE pulldown	Resistor to PGND, (Note 2)	20	50	115	kΩ
Fault Protection					
SS Charge Time	$V_{FB} = 0$ V	1.6	3.3	5.0	ms
SS Pulse Period	$V_{FB} = 0$ V	25	100	200	ms
SS Duty Cycle	(Charge Time/Period) × 100	1.0	3.3	6.0	%
SS COMP Clamp Voltage	$V_{FB} = 2.7$ V; $V_{SS} = 0$ V	0.50	0.95	1.10	V
V_{FB} Low Comparator	Increase V_{FB} till no SS pulsing and normal Off−time	0.9	1.0	1.1	V
PWM Comparator					
Transient Response	V_{FB} = 1.2 to 5.0 V. 500 ns after GATE(H) (after Blanking time) to GATE(H) = (V_{CC} −1.0 V) to 1.0 V	−	130	180	ns
Minimum Pulse Width (Blanking Time)	Drive V_{FB}. 1.2 to 5.0 V upon GATE(H) rising edge ($> V_{CC} - 1.0$ V), measure GATE(H) pulse width	50	150	250	ns
C_{OFF}					
Normal Off−Time	$V_{FB} = 2.7$ V	1.0	1.6	2.3	μs
Extended Off−Time	$V_{SS} = V_{FB} = 0$ V	5.0	8.0	12.0	μs
Time−Out Timer					
Time−Out Time	$V_{FB} = 2.7$ V, Measure GATE(H) Pulse Width	10	30	50	μs
Fault Duty Cycle	$V_{FB} = 0$V	30	50	70	%
Enable Input					
ENABLE Threshold	GATE(H) Switching	0.8	1.15	1.30	V
Shutdown delay (Note 3)	ENABLE−to−GATE(H) < 2.0 V	−	3.0	−	μs

2. Guaranteed by design, not 100% tested in production.

ELECTRICAL CHARACTERISTICS ($0°C < T_A < +70°C$; $0°C < T_J < +125°C$; $8.0\ V < V_{CC} < 14\ V$; 2.8 DAC Code: ($V_{ID4} = V_{ID2} = V_{ID1} = V_{ID0} = 1$; $V_{ID3} = 0$); $C_{GATE(H)}$ and $C_{GATE(L)} = 3.3$ nF; $C_{OFF} = 330$ pF; $C_{SS} = 0.1$ μF, unless otherwise specified.)

Characteristic	Test Conditions	Min	Typ	Max	Unit
Enable Input					
Pullup Current	ENABLE = 0 V	3.0	7.0	15	μA
Pullup Voltage	No load on ENABLE pin	1.30	1.8	3.0	V
Input Resistance	ENABLE = 5.0 V, $R = (5.0\ V - V_{PULLUP})/I_{ENABLE}$	10	20	50	kΩ
Power Good Output					
Low to High Delay	$V_{FB} = (0.8 \times V_{DAC})$ to V_{DAC}	30	65	110	μs
High to Low Delay	$V_{FB} = V_{DAC\ to}\ (0.8 \times V_{DAC})$	30	75	120	μs
Output Low Voltage	$V_{FB} = 2.4$ V, $I_{PWRGD} = 500$ μA	−	0.2	0.3	V
Sink Current Limit	$V_{FB} = 2.4$ V, PWRGD = 1.0 V	0.5	4.0	15.0	mA

3. Guaranteed by design, not 100% tested in production.

ELECTRICAL CHARACTERISTICS ($0°C < T_A < +70°C$; $0°C < T_J < +125°C$; $8.0\ V < V_{CC} < 14\ V$; 2.8 DAC Code: ($V_{ID4} = V_{ID2} = V_{ID1} = V_{ID0} = 1$; $V_{ID3} = 0$); $C_{GATE(H)}$ and $C_{GATE(L)} = 3.3$ nF; $C_{OFF} = 330$ pF; $C_{SS} = 0.1$ μF, unless otherwise specified.)

Characteristic					Test Conditions	Min	Typ	Max	Unit
Voltage Identification DAC									
Accuracy (all codes except 11111)					Measure V_{FB} = COMP ($C_{OFF} = 0$ V) $25°C \le T_J \le 125°C$; $V_{CC} = 12$ V	−1.0	−	+1.0	%
V_{ID4}	V_{ID3}	V_{ID2}	V_{ID1}	V_{ID0}					
1	0	0	0	0	−	3.505	3.540	3.575	V
1	0	0	0	1	−	3.406	3.440	3.474	V
1	0	0	1	0	−	3.307	3.340	3.373	V
1	0	0	1	1	−	3.208	3.240	3.272	V
1	0	1	0	0	−	3.109	3.140	3.171	V
1	0	1	0	1	−	3.010	3.040	3.070	V
1	0	1	1	0	−	2.911	2.940	2.969	V
1	0	1	1	1	−	2.812	2.840	2.868	V
1	1	0	0	0	−	2.713	2.740	2.767	V
1	1	0	0	1	−	2.614	2.640	2.666	V
1	1	0	1	0	−	2.515	2.540	2.565	V
1	1	0	1	1	−	2.416	2.440	2.464	V
1	1	1	0	0	−	2.317	2.340	2.363	V
1	1	1	0	1	−	2.218	2.240	2.262	V
1	1	1	1	0	−	2.119	2.140	2.161	V
0	0	0	0	0	−	2.069	2.090	2.111	V
0	0	0	0	1	−	2.020	2.040	2.060	V
0	0	0	1	0	−	1.970	1.990	2.010	V
0	0	0	1	1	−	1.921	1.940	1.959	V
0	0	1	0	0	−	1.871	1.890	1.909	V
0	0	1	0	1	−	1.822	1.840	1.858	V
0	0	1	1	0	−	1.772	1.790	1.808	V
0	0	1	1	1	−	1.723	1.740	1.757	V
0	1	0	0	0	−	1.673	1.690	1.707	V
0	1	0	0	1	−	1.624	1.640	1.656	V
0	1	0	1	0	−	1.574	1.590	1.606	V
0	1	0	1	1	−	1.525	1.540	1.555	V
0	1	1	0	0	−	1.475	1.490	1.505	V

ELECTRICAL CHARACTERISTICS ($0°C < T_A < +70°C$; $0°C < T_J < +125°C$; $8.0\ V < V_{CC} < 14\ V$; 2.8 DAC Code: ($V_{ID4} = V_{ID2} = V_{ID1} = V_{ID0} = 1$; $V_{ID3} = 0$); $C_{GATE(H)}$ and $C_{GATE(L)} = 3.3$ nF; $C_{OFF} = 330$ pF; $C_{SS} = 0.1\ \mu F$, unless otherwise specified.)

Characteristic					Test Conditions	Min	Typ	Max	Unit
Voltage Identification DAC									
0	1	1	0	1	−	1.426	1.440	1.455	V
0	1	1	1	0	−	1.376	1.390	1.405	V
0	1	1	1	1	−	1.327	1.340	1.353	V
1	1	1	1	1	−	1.223	1.247	1.273	V
Input Threshold					V_{ID4}, V_{ID3}, V_{ID2}, V_{ID1}, V_{ID0}	1.000	1.250	2.400	V
Input Pullup Resistance					V_{ID4}, V_{ID3}, V_{ID2}, V_{ID1}, V_{ID0}	25	50	100	kΩ
Input Pullup Voltage						4.85	5.00	5.15	V

Threshold Accuracy					Lower Threshold			Upper Threshold			Unit
					Min	Typ	Max	Min	Typ	Max	
DAC CODE											
% of Nominal DAC Output					−12	−8.5	−5.0	5.0	8.5	12	%
V_{ID4}	V_{ID3}	V_{ID2}	V_{ID1}	V_{ID0}							
1	0	0	0	0	3.115	3.239	3.363	3.717	3.841	3.965	V
1	0	0	0	1	3.027	3.148	3.268	3.612	3.732	3.853	V
1	0	0	1	0	2.939	3.056	3.173	3.507	3.624	3.741	V
1	0	0	1	1	2.851	2.965	3.078	3.402	3.515	3.629	V
1	0	1	0	0	2.763	2.873	2.983	3.297	3.407	3.517	V
1	0	1	0	1	2.675	2.782	2.888	3.192	3.298	3.405	V
1	0	1	1	0	2.587	2.690	2.793	3.087	3.190	3.293	V
1	0	1	1	1	2.499	2.599	2.698	2.982	3.081	3.181	V
1	1	0	0	0	2.411	2.507	2.603	2.877	2.973	3.069	V
1	1	0	0	1	2.323	2.416	2.508	2.772	2.864	2.957	V
1	1	0	1	0	2.235	2.324	2.413	2.667	2.756	2.845	V
1	1	0	1	1	2.147	2.233	2.318	2.562	2.647	2.733	V
1	1	1	0	0	2.059	2.141	2.223	2.457	2.539	2.621	V
1	1	1	0	1	1.971	2.050	2.128	2.352	2.430	2.509	V
1	1	1	1	0	1.883	1.958	2.033	2.250	2.322	2.397	V
0	0	0	0	0	1.839	1.912	1.986	2.195	2.268	2.341	V
0	0	0	0	1	1.795	1.867	1.938	2.142	2.213	2.285	V
0	0	0	1	0	1.751	1.821	1.810	2.090	2.159	2.229	V
0	0	0	1	1	1.707	1.775	1.843	2.037	2.105	2.173	V
0	0	1	0	0	1.663	1.729	1.796	1.985	2.051	2.117	V
0	0	1	0	1	1.619	1.684	1.748	1.932	1.996	2.061	V
0	0	1	1	0	1.575	1.638	1.701	1.880	1.942	2.005	V
0	0	1	1	1	1.531	1.592	1.653	1.827	1.888	1.949	V
0	1	0	0	0	1.487	1.546	1.606	1.775	1.834	1.893	V
0	1	0	0	1	1.443	1.501	1.558	1.722	1.779	1.837	V
0	1	0	1	0	1.399	1.455	1.511	1.670	1.725	1.781	V
0	1	0	1	1	1.355	1.409	1.463	1.617	1.671	1.724	V
0	1	1	0	0	1.311	1.363	1.416	1.565	1.617	1.669	V
0	1	1	0	1	1.267	1.318	1.368	1.512	1.562	1.613	V
0	1	1	1	0	1.223	1.272	1.321	1.460	1.508	1.557	V
0	1	1	1	1	1.179	1.226	1.273	1.407	1.454	1.501	V
1	1	1	1	1	1.097	1.141	1.185	1.309	1.353	1.397	V

PACKAGE PIN DESCRIPTION

PACKAGE PIN # SOIC−16	PIN SYMBOL	FUNCTION
1, 2, 3, 4, 6	V_{ID0}−V_{ID4}	Voltage ID DAC input pins. These pins are internally pulled up to 5.0 V if left open. V_{ID4} selects the DAC range. When V_{ID4} is high (logic one), the Error Amp reference range is 2.14 V to 3.45 V with 100 mV increments. When V_{ID4} is low (logic zero), the Error Amp reference voltage 1.34 V to 2.09 V with 50 mV increments.
5	SS	Soft−Start Pin. A capacitor from this pin to LGND sets the Soft−Start and fault timing.
7	C_{OFF}	Off−Time Capacitor Pin. A capacitor from this pin to LGND sets both the normal and extended off time.
8	ENABLE	Output Enable Input. This pin is internally pulled up to 1.8 V. A logic Low (< 0.8) on this pin disables operation and places the CS5165A into a low current sleep mode.
9	V_{CC}	Input Power Supply Pin.
10	GATE(H)	High Side Switch FET driver pin.
11	PGND	High current ground for the GATE(H) and GATE(L) pins.
12	GATE(L)	Low Side Synchronous FET driver pin.
13	PWRGD	Power Good Output. Open collector output drives low when V_{FB} is out of regulation. Active when ENABLE input is low.
14	LGND	Reference ground. All control circuits are referenced to this pin.
15	COMP	Error Amp output. PWM Comparator reference input. A capacitor to LGND provides Error Amp compensation.
16	V_{FB}	Error Amp, PWM Comparator, and Low V_{FB} Comparator feedback input.

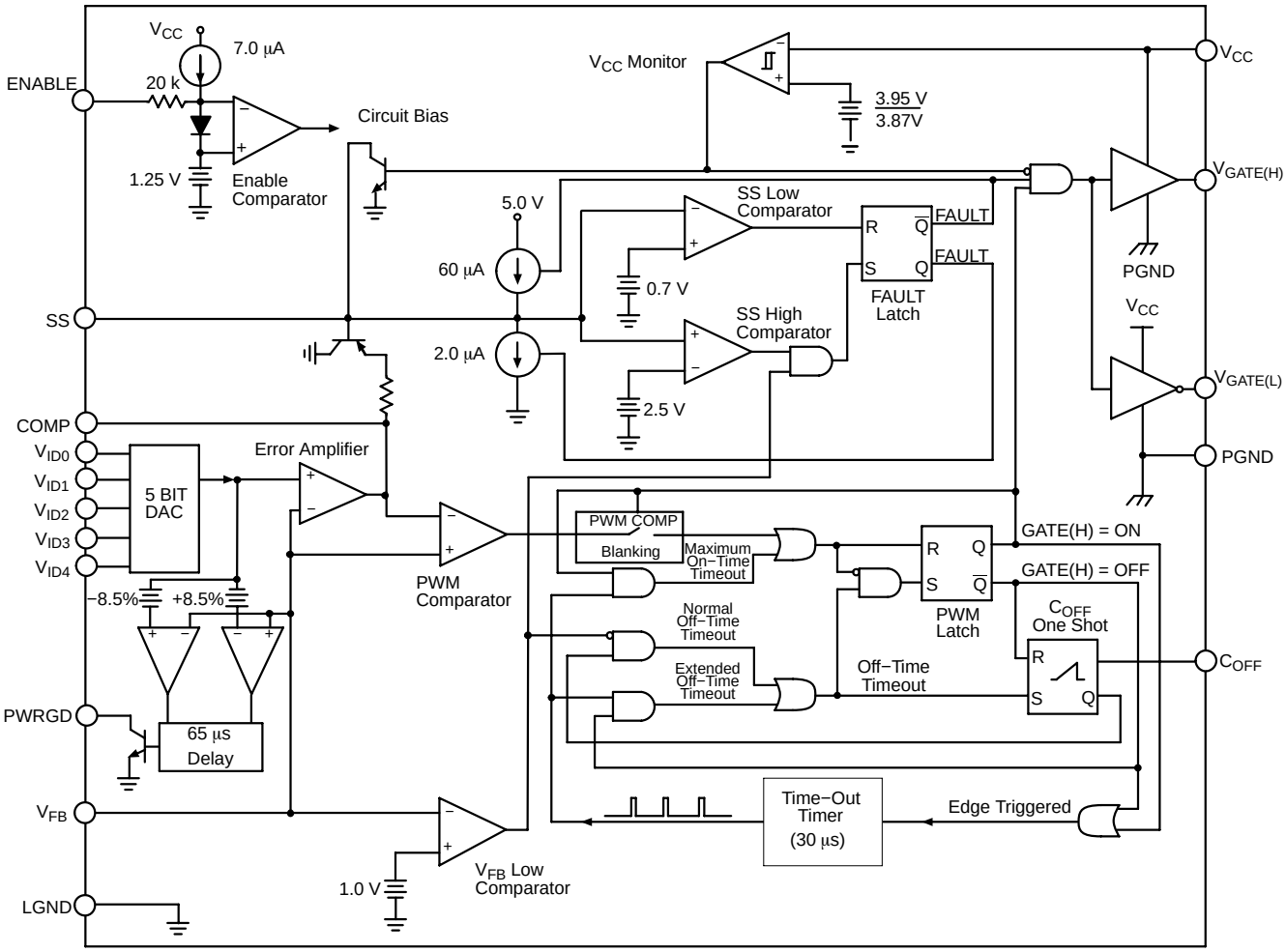


Figure 2. Block Diagram

TYPICAL PERFORMANCE CHARACTERISTICS

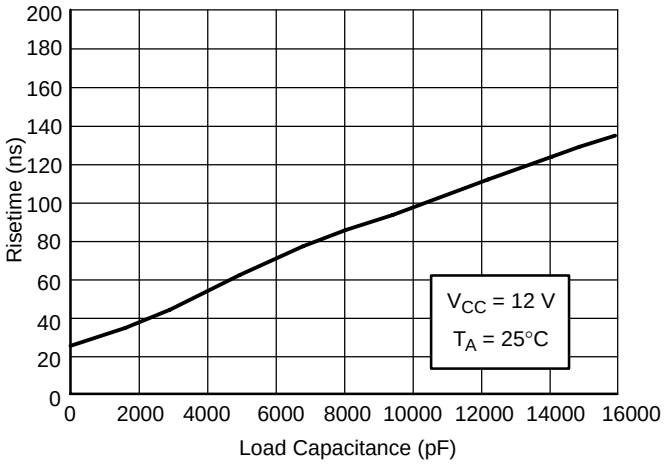


Figure 3. GATE(L) Risetime vs. Load Capacitance

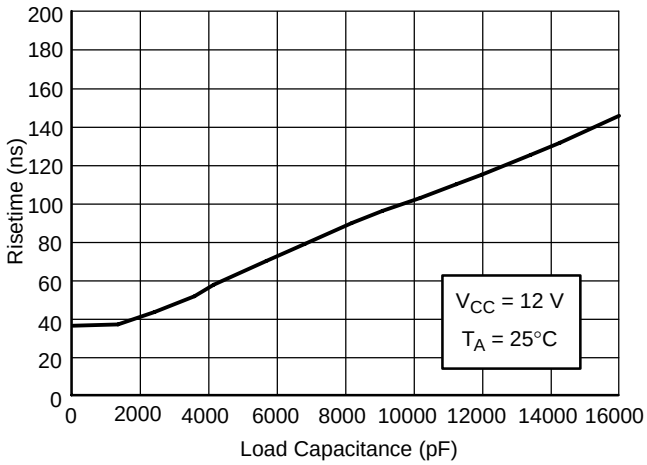


Figure 4. GATE(H) Risetime vs. Load Capacitance

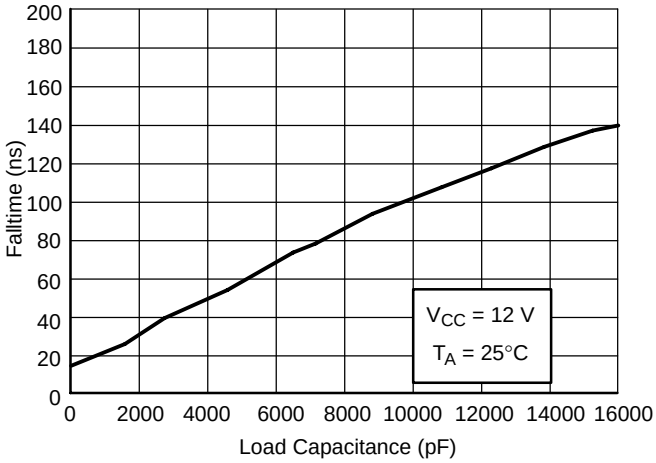


Figure 5. GATE(H) & GATE(L) Falltime vs. Load Capacitance

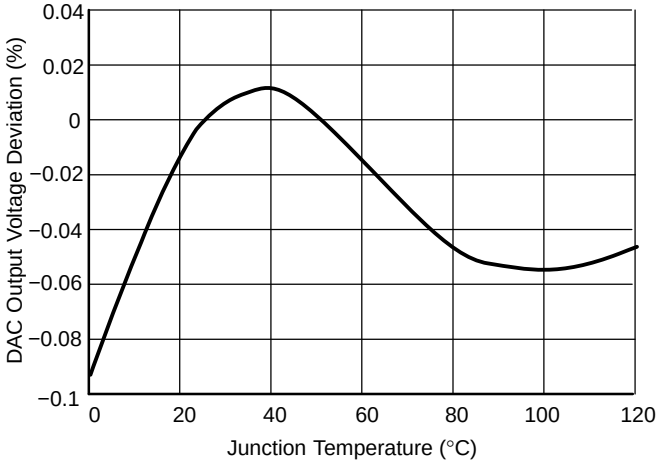


Figure 6. DAC Output Voltage vs. Temperature, DAC Code = 10111, V_{CC} = 12 V

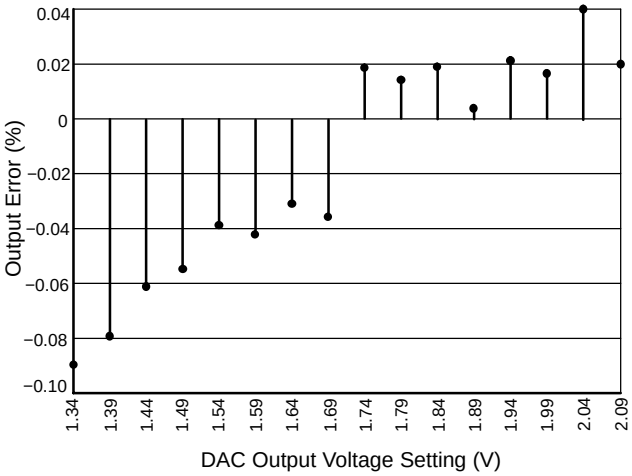


Figure 7. Percent Output Error vs. DAC Voltage Setting, V_{CC} = 12 V, T_A = 25°C, V_{ID4} = 0

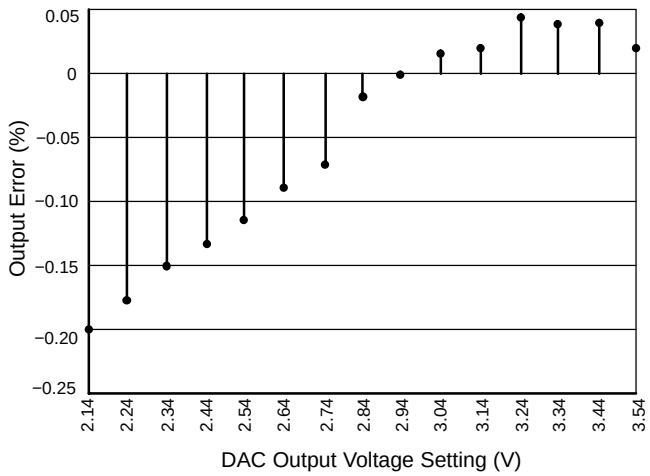


Figure 8. Percent Output Error vs. DAC Output Voltage Setting V_{CC} = 12 V, T_A = 25°C, V_{ID4} = 1

APPLICATIONS INFORMATION

THEORY OF OPERATION

V^2 Control Method

The V^2 method of control uses a ramp signal that is generated by the ESR of the output capacitors. This ramp is proportional to the AC current through the main inductor and is offset by the value of the DC output voltage. This control scheme inherently compensates for variation in either line or load conditions, since the ramp signal is generated from the output voltage itself. This control scheme differs from traditional techniques such as voltage mode, which generates an artificial ramp, and current mode, which generates a ramp from inductor current.

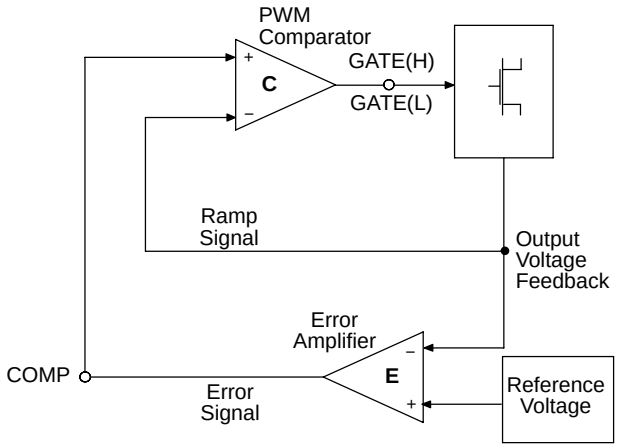


Figure 9. V^2 Control Diagram

The V^2 control method is illustrated in Figure 9. The output voltage is used to generate both the error signal and the ramp signal. Since the ramp signal is simply the output voltage, it is affected by any change in the output regardless of the origin of that change. The ramp signal also contains the DC portion of the output voltage, which allows the control circuit to drive the main switch to 0% or 100% duty cycle as required.

A change in line voltage changes the current ramp in the inductor, affecting the ramp signal, which causes the V^2 control scheme to compensate the duty cycle. Since the change in inductor current modifies the ramp signal, as in current mode control, the V^2 control scheme has the same advantages in line transient response.

A change in load current will have an affect on the output voltage, altering the ramp signal. A load step immediately changes the state of the comparator output, which controls the main switch. Load transient response is determined only by the comparator response time and the transition speed of the main switch. The reaction time to an output load step has no relation to the crossover frequency of the error signal loop, as in traditional control methods.

The error signal loop can have a low crossover frequency, since transient response is handled by the ramp signal loop. The main purpose of this ‘slow’ feedback loop is to provide DC accuracy. Noise immunity is significantly improved, since the error amplifier bandwidth can be rolled off at a low frequency. Enhanced noise immunity improves remote sensing of the output voltage, since the noise associated with long feedback traces can be effectively filtered.

Line and load regulation are drastically improved because there are two independent voltage loops. A voltage mode controller relies on a change in the error signal to compensate for a deviation in either line or load voltage. This change in the error signal causes the output voltage to change corresponding to the gain of the error amplifier, which is normally specified as line and load regulation. A current mode controller maintains fixed error signal under deviation in the line voltage, since the slope of the ramp signal changes, but still relies on a change in the error signal for a deviation in load. The V^2 method of control maintains a fixed error signal for both line and load variation, since the ramp signal is affected by both line and load.

Constant Off Time

To maximize transient response, the CS5165A uses a constant off time method to control the rate of output pulses. During normal operation, the off time of the high side switch is terminated after a fixed period, set by the C_{OFF} capacitor. To maintain regulation, the V^2 control loop varies switch on time. The PWM comparator monitors the output voltage ramp, and terminates the switch on time.

Constant off time provides a number of advantages. Switch duty cycle can be adjusted from 0 to 100% on a pulse by pulse basis when responding to transient conditions. Both 0% and 100% duty cycle operation can be maintained for extended periods of time in response to load or line transients. PWM slope compensation to avoid sub−harmonic oscillations at high duty cycles is avoided.

Switch on time is limited by an internal 30 μs (typical) timer, minimizing stress to the power components.

Programmable Output

The CS5165A is designed to provide two methods for programming the output voltage of the power supply. A 5−bit on board digital to analog converter (DAC) is used to program the output voltage within two different ranges. The first range is 2.14 V to 3.54 V in 100 mV steps, the second is 1.34 V to 2.09 V in 50 mV steps, depending on the digital input code. If all five bits are left open, the CS5165A enters adjust mode. In adjust mode, the designer can choose any output voltage by using resistor divider feedback to the V_{FB} pin, as in traditional controllers. The CS5165A is specifically designed to meet or exceed Intel’s Pentium II specifications.

Startup

Until the voltage on the V_{CC} supply pin exceeds the 3.95 V monitor threshold, the Soft−Start and GATE pins are held low. The FAULT latch is reset (no Fault condition). The output of the error amplifier (COMP) is pulled up to 1.0 V by the comparator clamp. When the V_{CC} pin exceeds the monitor threshold, the GATE(H) output is activated, and the Soft−Start

capacitor begins charging. The GATE(H) output will remain on, enabling the NFET switch, until terminated by either the PWM comparator, or the maximum on time timer.

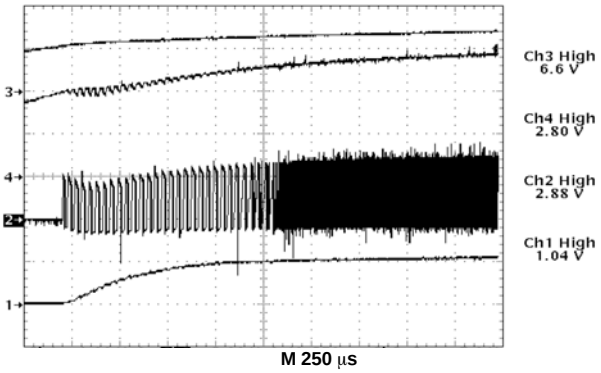
If the maximum on time is exceeded before the regulator output voltage achieves the 1.0 V level, the pulse is terminated. The GATE(H) pin drives low, and the GATE(L) pin drives high for the duration of the extended off time. This time is set by the time out timer and is approximately equal to the maximum on time, resulting in a 50% duty cycle. The GATE(L) pin will then drive low, the GATE(H) pin will drive high, and the cycle repeats.

When regulator output voltage achieves the 1.0 V level present at the COMP pin, regulation has been achieved and normal off time will ensue. The PWM comparator terminates the switch on time, with off time set by the C_{OFF} capacitor. The V^2 control loop will adjust switch duty cycle as required to ensure the regulator output voltage tracks the output of the error amplifier.

The Soft−Start and COMP capacitors will charge to their final levels, providing a controlled turn on of the regulator output. Regulator turn on time is determined by the COMP capacitor charging to its final value. Its voltage is limited by the Soft−Start COMP clamp and the voltage on the Soft−Start pin.

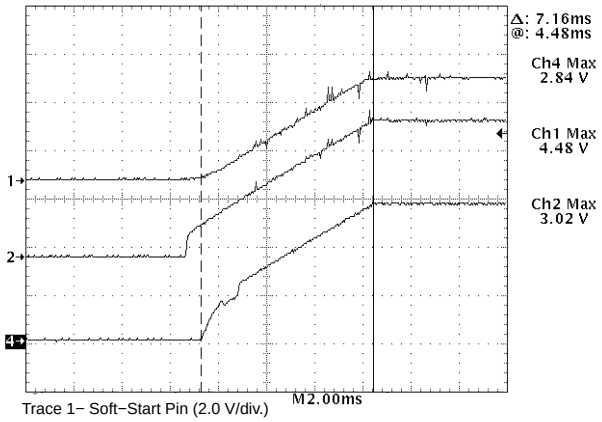
Power Supply Sequencing

The CS5165A offers inherent protection from undefined startup conditions, regardless of the 12 V and 5.0 V supply power up sequencing. The turn on slew rates of the 12 V and 5.0 V power supplies can be varied over wide ranges without affecting the output voltage or causing detrimental effects to the buck regulator.



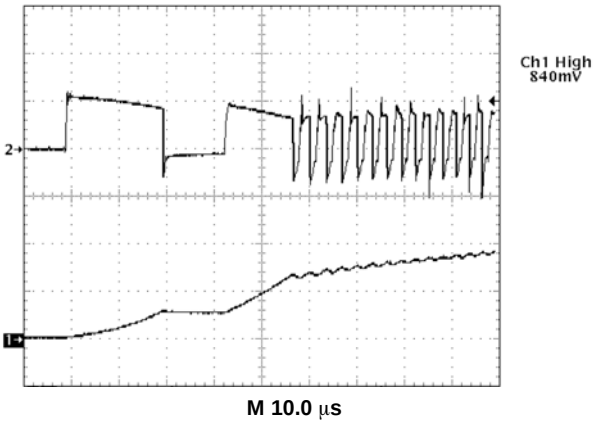
Trace 1− Regulator Output Voltage (1.0 V/div.)
Trace 2− Inductor Switching Node (2.0 V/div.)
Trace 3− 12 V Input (V_{CC}) (5.0 V/div.)
Trace 4− 5.0 V Input (1.0 V/div.)

Figure 10. Demonstration Board Startup in Response to Increasing 12 V and 5.0 V Input Voltages. Extended Off Time is Followed by Normal Off Time Operation when Output Voltage Achieves Regulation to the Error Amplifier Output.



Trace 1− Soft−Start Pin (2.0 V/div.)
Trace 2− COMP PIn (error amplifier output) (1.0 V/div.)
Trace 4− Regulator Output Voltage (1.0 V/div.)

Figure 11. Demonstration Board Startup Waveforms

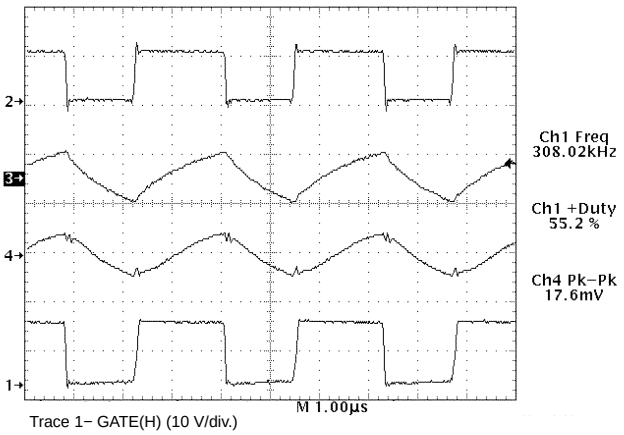


Trace 1− Regulator Output Voltage (1.0 V/div.)
Trace 2− Inductor Switching Node (5.0 V/div.)

Figure 12. Demonstration Board Enable Startup Waveforms

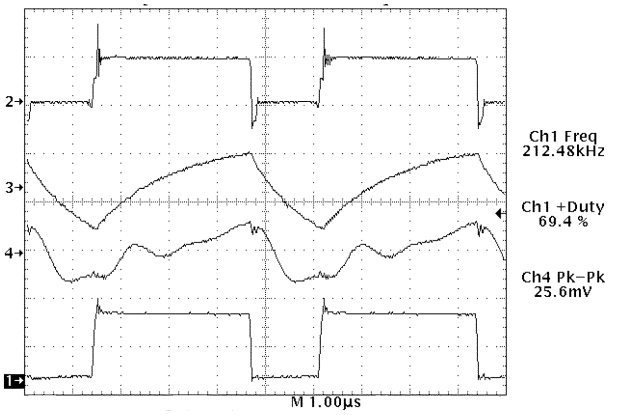
Normal Operation

During normal operation, switch off time is constant and set by the C_{OFF} capacitor. Switch on time is adjusted by the V^2 control loop to maintain regulation. This results in changes in regulator switching frequency, duty cycle, and output ripple in response to changes in load and line. Output voltage ripple will be determined by inductor ripple current working and the ESR of the output capacitors (see Figures 13 and 14).



Trace 1− GATE(H) (10 V/div.)
Trace 2− Inductor Switching Node (5.0 V/div.)
Trace 3− Output Inductor Ripple Current (2.0 A/div.)
Trace 4− V_{OUT} ripple (20 mV/div.)

Figure 13. Normal Operation Showing Output Inductor Ripple Current and Output Voltage Ripple, 0.5 A Load, V_{OUT} = +2.84 V (DAC = 10111)



Trace 1− GATE(H) (10 V/div.)
Trace 2− Inductor Switching Node (5.0 V/div.)
Trace 3− Output Inductor Ripple Current (2.0 A/div.)
Trace 4− V_{OUT} ripple (20 mV/div.)

Figure 14. Normal Operation Showing Output Inductor Ripple Current and Output Voltage Ripple, I_{LOAD} = 14 A, V_{OUT} = +2.84 V (DAC = 10111)

Transient Response

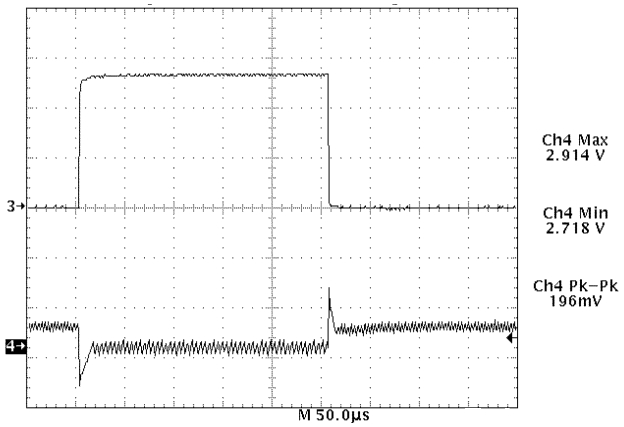
The CS5165A V^2 control loop's 100 ns reaction time provides unprecedented transient response to changes in input voltage or output current. Pulse by pulse adjustment of duty cycle is provided to quickly ramp the inductor current to the required level. Since the inductor current cannot be changed instantaneously, regulation is maintained by the output capacitor(s) during the time required to slew the inductor current.

Overall load transient response is further improved through a feature called "Adaptive Voltage Positioning". This technique pre−positions the output capacitors voltage to reduce total output voltage excursions during changes in load.

Holding tolerance to 1.0% allows the error amplifiers reference voltage to be targeted +40 mV high without compromising DC accuracy. A "Droop Resistor", implemented through a PC board trace, connects the Error Amps feedback pin (V_{FB}) to the output capacitors and load and carries the output current. With no load, there is no DC drop across this resistor, producing an output voltage tracking the Error amps, including the +40 mV offset. When the full load current is delivered, an 80 mV drop is developed across this resistor. This results in output voltage being offset −40 mV low.

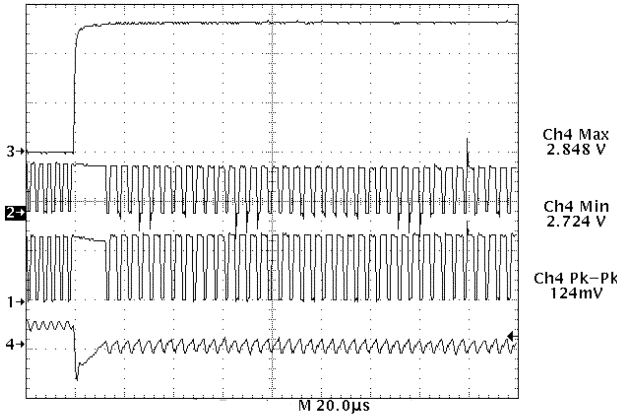
The result of Adaptive Voltage Positioning is that additional margin is provided for a load transient before reaching the output voltage specification limits. When load current suddenly increases from its minimum level, the output capacitor is pre−positioned +40 mV. Conversely, when load current suddenly decreases from its maximum level, the output capacitor is pre−positioned −40 mV (see Figures 15, 16, and 17). For best Transient Response, a combination of a number of high frequency and bulk output capacitors are usually used.

If the Maximum On−Time is exceeded while responding to a sudden increase in Load current, a normal off−time occurs to prevent saturation of the output inductor.



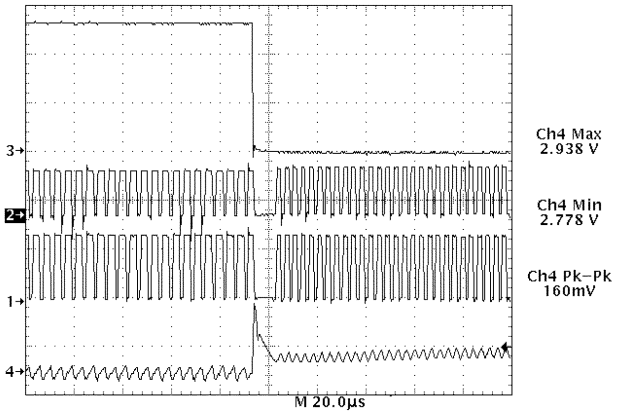
Trace 3− Load Current (5.0 A/10 mV/div.)
Trace 4− V_{OUT} (100 mV/div.)

Figure 15. Output Voltage Transient Response to a 14 A Load Pulse, V_{OUT} = +2.84 V (DAC = 10111)



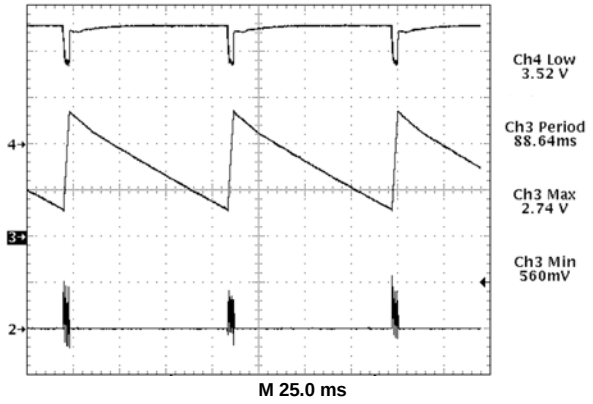
Trace 1− GATE(H) (10 V/div.)
Trace 2− Inductor Switching Node (5.0 V/div.)
Trace 3− Load Current (5.0 A/div)
Trace 4− V_{OUT} (100 mV/div.)

Figure 16. Output Voltage Transient Response to a 14 A Load Step, V_{OUT} = +2.84 V (DAC = 10111)



Trace 1− GATE(H) (10 V/div.)
Trace 2− Inductor Switching Node (5.0 V/div.)
Trace 3− Load Current (5.0 A/div)
Trace 4− V_{OUT} (100 mV/div.)

Figure 17. Output Voltage Transient Response to a 14 A Load Turn−Off, V_{OUT} = +2.84 V (DAC = 10111)



Trace 4− 5.0 V Supply Voltage (2.0 V/div.)
Trace 3− Soft−Start Timing Capacitor (1.0 V/div.)
Trace 2− Inductor Switching Node (2.0 V/div.)

Figure 18. Demonstration Board Hiccup Mode Short Circuit Protection. Gate Pulses are Delivered While the Soft−Start Capacitor Charges, and Cease During Discharge

PROTECTION AND MONITORING FEATURES

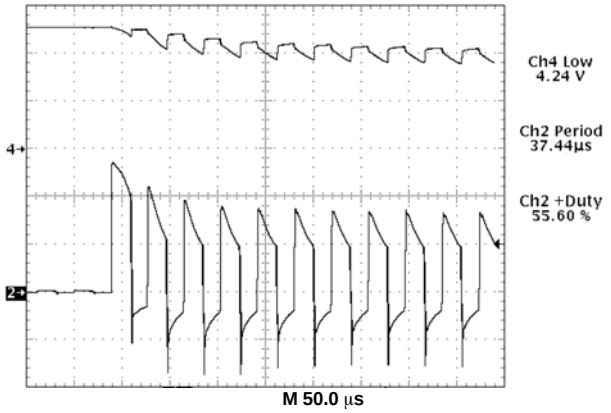
Short Circuit Protection

A lossless hiccup mode short circuit protection feature is provided, requiring only the Soft−Start capacitor to implement. If a short circuit condition occurs the V_{FB} low comparator sets the FAULT latch. This causes the top FET to shut off, disconnecting the regulator from it's input voltage. The Soft−Start capacitor is then slowly discharged by a 2.0 μA current source until it reaches it's lower 0.7 V threshold. The regulator will then attempt to restart normally, operating in it's extended off time mode with a 50% duty cycle, while the Soft−Start capacitor is charged with a 60 μA charge current.

If the short circuit condition persists, the regulator output will not achieve the 1.0 V low V_{FB} comparator threshold before the Soft−Start capacitor is charged to it's upper 2.5 V threshold. If this happens the cycle will repeat itself until the short is removed. The Soft−Start charge/discharge current ratio sets the duty cycle for the pulses (2.0 μA/60 μA = 3.3%), while actual duty cycle is half that due to the extended off time mode (1.65%).

This protection feature results in less stress to the regulator components, input power supply, and PC board traces than occurs with constant current limit protection (see Figures 18 and 19).

If the short circuit condition is removed, output voltage will rise above the 1.0 V level, preventing the FAULT latch from being set, allowing normal operation to resume.



Trace 4− 5.0 V from PC Power Supply (2.0 V/div.)
Trace 2− Inductor Switching Node (2.0 V/div.)

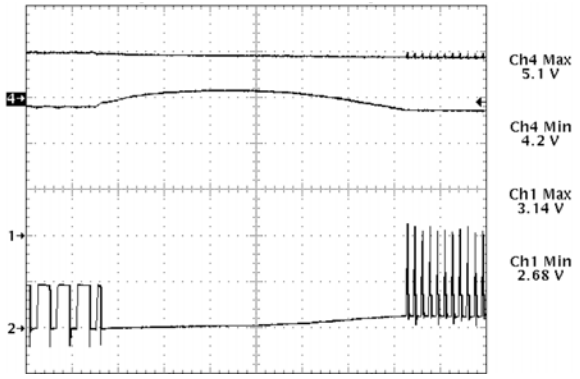
Figure 19. Demonstration Board Startup with Regulator Output Shorted To Ground

Overvoltage Protection

Overvoltage protection (OVP) is provided as result of the normal operation of the V^2 control topology and requires no additional external components. The control loop responds to an overvoltage condition within 100 ns, causing the top MOSFET to shut off, disconnecting the regulator from it's input voltage. The bottom MOSFET is then activated, resulting in a "crowbar" action to clamp the output voltage and prevent damage to the load (see Figures 20 and 21). The regulator will

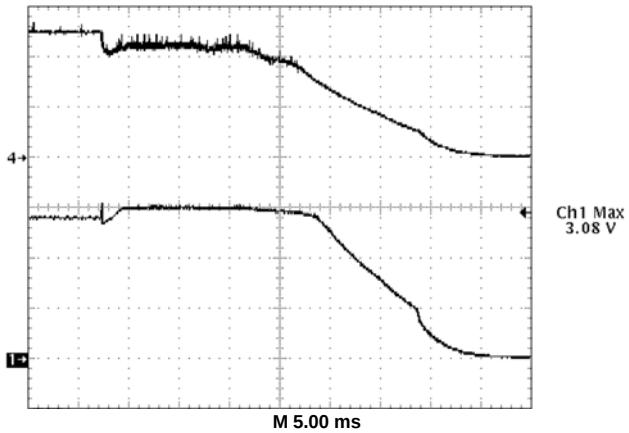
remain in this state until the overvoltage condition ceases or the input voltage is pulled low. The bottom FET and board trace must be properly designed to implement the OVP function.If a dedicated OVP output is required, it can be implemented using the circuit in Figure 22. In this figure the OVP signal will go high (overvoltage condition), if the output voltage (V_{CORE}) exceeds 20% of the voltage set by the particular DAC code and provided that PWRGD is low. It is also required that the overvoltage condition be present for at least the PWRGD delay time for the OVP signal to be activated. The resistor values shown in Figure 22 are for V_{DAC} = +2.8 V (DAC = 10111). The V_{OVP} (overvoltage trip−point) can be set using the following equation:

$$V_{OVP} = V_{BEQ3}\left(1 + \frac{R2}{R1}\right)$$



Trace 4− 5.0 V from PC Power Supply (5.0 V/div.)
Trace 1− Regulator Output Voltage (1.0 V/div.)
Trace 2− Inductor Switching Node 5.0 V/div.)

Figure 20. OVP Response to an Input−to−Output Short Circuit by Immediately Providing 0% Duty Cycle, Crow−Barring the Input Voltage to Ground



Trace 4− 5.0 V from PC Power Supply (2.0 V/div.)
Trace 1− Regulator Output Voltage (1.0 V/div.)

Figure 21. OVP Response to an Input−to−Output Short Circuit by Pulling the Input Voltage to Ground

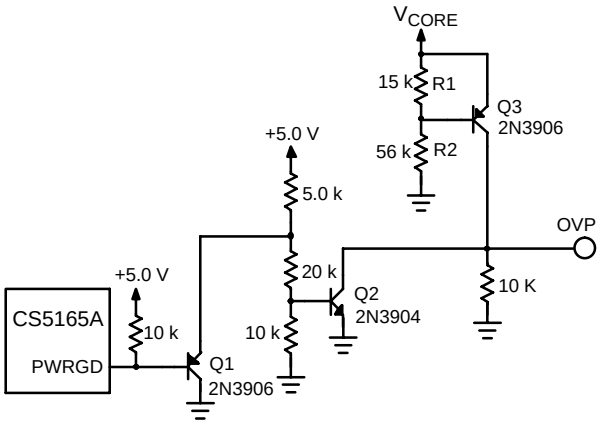


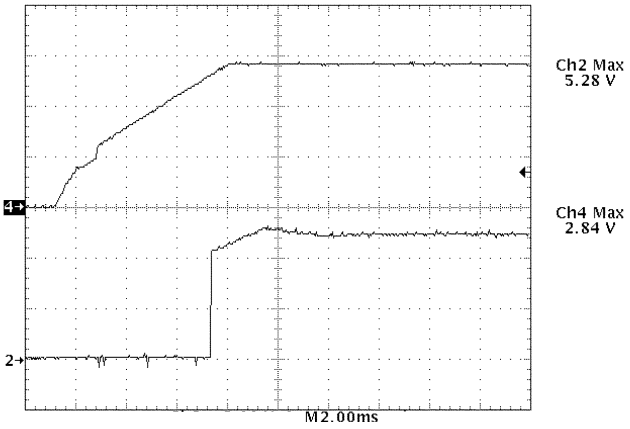
Figure 22. Circuit To Implement A Dedicated OVP Output Using The CS5165A

Output Enable Circuit

The Enable pin (pin 8) is used to enable or disable the regulator output voltage, and is consistent with TTL DC specifications. It is internally pulled−up. If pulled low (below 0.8 V), the output voltage is disabled. At the same time the Power Good and Soft−Start pins are pulled low, so that when normal operation resumes power−up of the CS5165A goes through the Soft−Start sequence. Upon pulling the Enable pin low, the internal IC bias is completely shut off, resulting in total shutdown of the Controller IC.

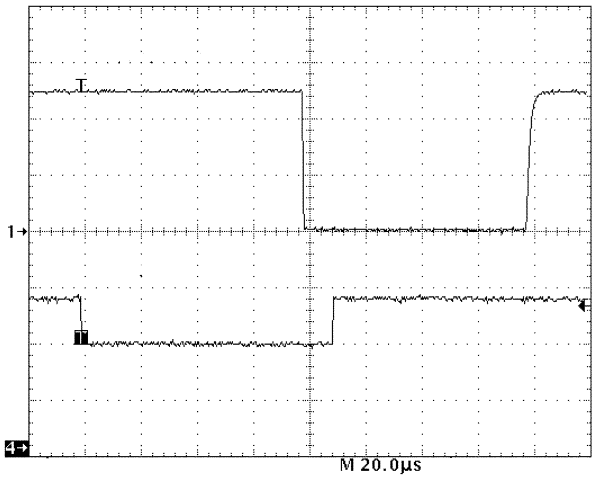
Power Good Circuit

The Power Good pin (pin 13) is an open−collector signal consistent with TTL DC specifications. It is externally pulled−up, and is pulled low (below 0.3 V) when the regulator output voltage typically exceeds ± 8.5% of the nominal output voltage. Maximum output voltage deviation before Power Good is pulled low is ± 12%.



Trace 2− PWRGD (2.0 V/div.)
Trace 4− V_{OUT} (1.0 V/div.)

Figure 23. PWRGD Signal Becomes Logic High as V_{OUT} Enters −8.5% of Lower PWRGD Threshold, V_{OUT} = +2.84 V (DAC = 10111)

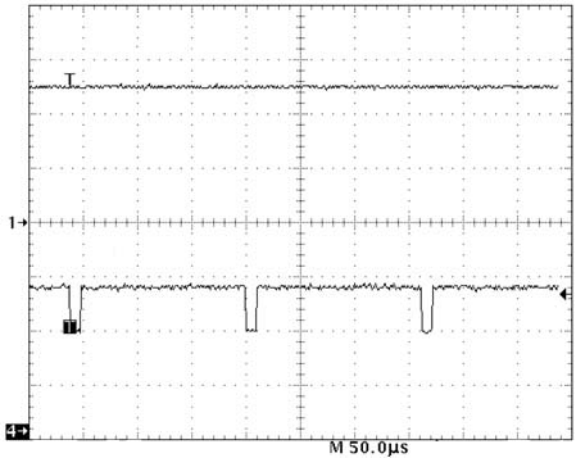


Trace 2− PWRGD (2.0 V/div.)
Trace 4− V_{FB} (1.0 V/div.)

Figure 24. Power Good Response to an Out of Regulation Condition

Figure 24 shows the relationship between the regulated output voltage V_{FB} and the Power Good signal. To prevent Power Good from interrupting the CPU unnecessarily, the CS5165A has a built−in delay to prevent noise at the V_{FB} pin from toggling Power Good. The internal time delay is designed to take about 75 µs for Power Good to go low and 65 µs for it to recover. This allows the Power Good signal to be completely insensitive to out of regulation conditions that are present for a duration less than the built in delay (see Figure 25).

It is therefore required that the output voltage attains an out of regulation or in regulation level for at least the built−in delay time duration before the Power Good signal can change state.



Trace 2− PWRGD (2.0 V/div.)
Trace 4− V_{FB} (1.0 V/div.)

Figure 25. Power Good is Insensitive to Out of Regulation Conditions that are Present for a Duration Less Than the Built In Delay

Selecting External Components

The CS5165A buck regulator can be used with a wide range of external power components to optimize the cost and performance of a particular design. The following information can be used as general guidelines to assist in their selection.

NFET Power Transistors

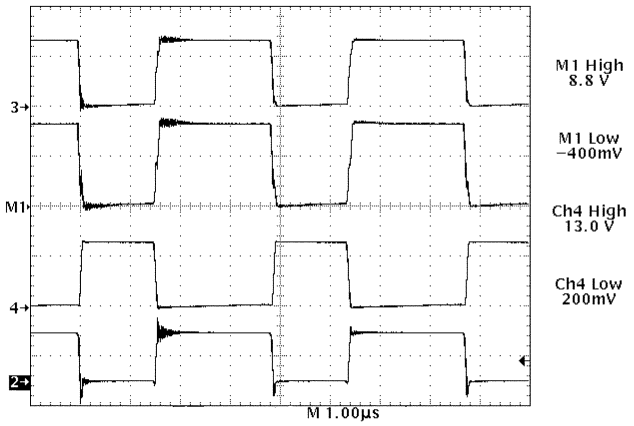
Both logic level and standard FETs can be used. The reference designs derive gate drive from the 12 V supply which is generally available in most computer systems and utilize logic level FETs. A charge pump may be easily implemented to support 5.0 V only systems. Multiple FET's may be paralleled to reduce losses and improve efficiency and thermal management.

Voltage applied to the FET gates depends on the application circuit used. Both upper and lower gate driver outputs are specified to drive to within 1.5 V of ground when in the low state and to within 2.0 V of their respective bias supplies when in the high state. In practice, the FET gates will be driven rail to rail due to overshoot caused by the capacitive load they present to the controller IC. For the typical application where V_{CC} = 12 V and 5.0 V is used as the source for the regulator output current, the following gate drive is provided:

$$V_{GS(TOP)} = 12\ V - 5.0\ V = 7.0\ V$$

$$V_{GS(BOTTOM)} = 12\ V$$

(see Figure 26)



Trace 3− GATE(H) (10 V/div.)
Trace 1− GATE(H) − 5.0 V_{IN}
Trace 4− GATE(L) (10 V/div.)
Trace 2− Inductor Switching Node (5.0 V/div.)

Figure 26. Gate Drive Waveforms Depicting Rail to Rail Swing

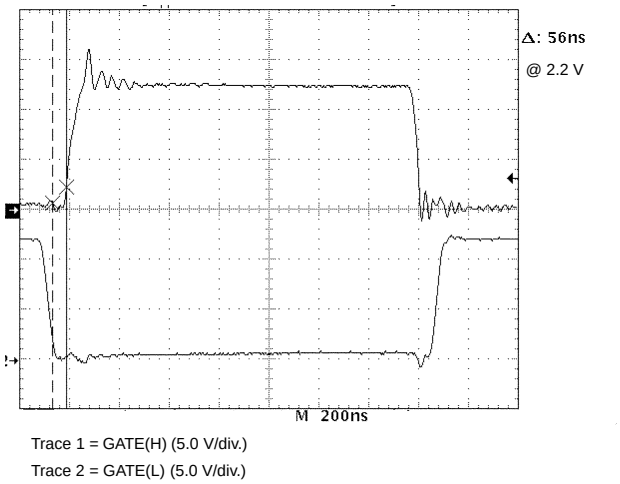


Figure 27. Normal Operation Showing the Guaranteed Non−Overlap Time Between the High and Low−Side MOSFET Gate Drives, I_{LOAD} = 14 A

The CS5165A provides adaptive control of the external NFET conduction times by guaranteeing a typical 65 ns non−overlap between the upper and lower MOSFET gate drive pulses. This feature eliminates the potentially catastrophic effect of "shoot−through current", a condition during which both FETs conduct causing them to overheat, self−destruct, and possibly inflict irreversible damage to the processor.

The most important aspect of FET performance is RDS_{ON}, which effects regulator efficiency and FET thermal management requirements.

The power dissipated by the MOSFETs may be estimated as follows:

Switching MOSFET:

$$\text{Power} = I_{LOAD}^2 \times RDS_{ON} \times \text{duty cycle}$$

Synchronous MOSFET:

$$\text{Power} = I_{LOAD}^2 \times RDS_{ON} \times (1 - \text{duty cycle})$$

Duty Cycle =

$$\frac{V_{OUT} + (I_{LOAD} \times RDS_{ON\ OF\ SYNCH\ FET})}{\left[\begin{array}{l} V_{IN} + (I_{LOAD} \times RDS_{ON\ OF\ SYNCH\ FET}) \\ - (I_{LOAD} \times RDS_{ON\ OF\ SWITCH\ FET}) \end{array}\right]}$$

Off Time Capacitor (C_{OFF})

The C_{OFF} timing capacitor sets the regulator off time:

$$T_{OFF} = C_{OFF} \times 4848.5$$

The preceding equations for duty cycle can also be used to calculate the regulator switching frequency and select the C_{OFF} timing capacitor:

$$C_{OFF} = \frac{\text{Perioid} \times (1 - \text{duty cycle})}{4848.5}$$

where:

$$\text{Period} = \frac{1}{\text{switching frequency}}$$

Schottky Diode for Synchronous FET

For synchronous operation, a Schottky diode may be placed in parallel with the synchronous FET to conduct the inductor current upon turn off of the switching FET to improve efficiency. The CS5165A reference circuit does not use this device due to it's excellent design. Instead, the body diode of the synchronous FET is utilized to reduce cost and conducts the inductor current. For a design operating at 200 kHz or so, the low non−overlap time combined with Schottky forward recovery time may make the benefits of this device not worth the additional expense. The power dissipation in the synchronous MOSFET due to body diode conduction can be estimated by the following equation:

$$\text{Power} = V_{BD} \times I_{LOAD} \times \text{conduction time} \times \text{switching frequency}$$

Where V_{BD} = the forward drop of the MOSFET body diode. For the CS5165A demonstration board:

$$\text{Power} = 1.6\ V \times 14.2\ A \times 100\ ns \times 200\ kHz = 0.45\ W$$

This is only 1.1% of the 40 W being delivered to the load.

"Droop" Resistor for Adaptive Voltage Positioning

Adaptive voltage positioning is used to help keep the output voltage within specification during load transients. To implement adaptive voltage positioning a "Droop Resistor" must be connected between the output inductor and output capacitors and load. This resistor carries the full load current and should be chosen so that both DC and AC tolerance limits are met. An embedded PC trace resistor has the distinct advantage of near zero cost implementation. However, this droop resistor can vary due to three reasons: 1) the sheet resistivity variation causes the thickness of the PCB layer to vary. 2) the mismatch of L/W, and 3) temperature variation.

1. **Sheet Resistivity** for one ounce copper, the thickness variation typically 1.15 mil to 1.35 mil. Therefore the error due to sheet resistivity is:
$$\frac{1.35 - 1.15}{1.25} = 16\%$$
2. **Mismatch due to L/W.** The variation in L/W is governed by variations due to the PCB manufacturing process that affect the geometry and the power dissipation capability of the droop resistor. The error due to L/W mismatch is typically 1.0%.
3. **Thermal Considerations.** Due to $I^2 \times R$ power losses the surface temperature of the droop resistor will increase causing the resistance to increase. Also, the ambient temperature variation will contribute to the increase of the resistance, according to the formula:
$$R = R_{20}[1 + \alpha_{20}(T - 20)]$$

where:

R_{20} = resistance at 20°C

$\alpha = \frac{0.00393}{^\circ C}$

T = operating temperature

R = desired droop resistor value

For temperature T = 50°C, the % R change = 12%

Droop Resistor Tolerance

Tolerance due to sheet resistivity variation	16%
Tolerance due to L/W error	1.0%
Tolerance due to temperature variation	12%
Total tolerance for droop resistor	29%

In order to determine the droop resistor value the nominal voltage drop across it at full load has to be calculated. This voltage drop has to be such that the output voltage full load is above the minimum DC tolerance spec.

$$V_{DROOP(TYP)} = \frac{[V_{DAC(MIN)} - V_{DC(MIN)}]}{1 + R_{DROOP(TOLERANCE)}}$$

Example: for a 300 MHz Pentium II, the DC accuracy spec is $2.74 < V_{CC(CORE)} < 2.9$ V, and the AC accuracy spec is $2.67\ V < V_{CC(CORE)} < 2.9$ 3V. The CS5165A DAC output voltage is $+2.812\ V < V_{DAC} < +2.868$ V. In order not to exceed the DC accuracy spec, the voltage drop developed across the resistor must be calculated as follows:

$$V_{DROOP(TYP)} = \frac{[V_{DAC(MIN)} - V_{DC\ PENTIUMII(MIN)}]}{1 + R_{DROOP(TOLERANCE)}}$$

$$= \frac{2.812\ V - 2.74\ V}{1.3} = 56\ mV$$

With the CS5165A DAC accuracy being 1.0%, the internal error amplifier's reference voltage is trimmed so that the output voltage will be 40 mV high at no load. With no load, there is no DC drop across the resistor, producing an output voltage tracking the error amplifier output voltage, including the offset. When the full load current is delivered, a drop of −56 mV is developed across the resistor. Therefore, the regulator output is pre−positioned at 40 mV above the nominal output voltage before a load turn−on. The total voltage drop due to a load step is ΔV−40 mV and the deviation from the nominal output voltage is 40 mV smaller than it would be if there was no droop resistor. Similarly at full load the regulator output is pre−positioned at 16 mV below the nominal voltage before a load turn−off. The total voltage increase due to a load turn−off is ΔV−16 mV and the deviation from the nominal output voltage is 16 mV smaller than it would be if there was no droop resistor. This is because the output capacitors are pre−charged to value that is either 40 mV above the nominal output voltage before a load turn−on or, 16 mV below the nominal output voltage before a load turn−off (see Figure 15).

Obviously, the larger the voltage drop across the droop resistor (the larger the resistance), the worse the DC and load regulation, but the better the AC transient response.

Design Rules for Using a Droop Resistor

The basic equation for laying an embedded resistor is:

$$R_{AR} = \rho \times \frac{L}{A} \text{ or } R = \rho \times \frac{L}{(W \times t)}$$

where:

A = W × t = cross−sectional area
ρ = the copper resistivity (μΩ − mil)
L = length (mils)
W = width (mils)
t = thickness (mils)

For most PCBs the copper thickness, t, is 35 μm (1.37 mils) for one ounce copper. ρ = 717.86 μΩ−mil

For a Pentium II load of 14.2 A the resistance needed to create a 56 mV drop at full load is:

$$\text{Response Droop} = \frac{56\ mV}{I_{OUT}} = \frac{56\ mV}{14.2\ A} = 3.9\ m\Omega$$

The resistivity of the copper will drift with the temperature according to the following guidelines:

$$\Delta R = 12\%\ @\ T_A = +50^{\circ}C$$
$$\Delta R = 34\%\ @\ T_A = +100^{\circ}C$$

Droop Resistor Width Calculations

The droop resistor must have the ability to handle the load current and therefore requires a minimum width which is calculated as follows (assume one ounce copper thickness):

$$W = \frac{I_{LOAD}}{0.05}$$

where:

W = minimum width (in mils) required for proper power dissipation, and I_{LOAD} Load Current Amps.

The Pentium®II maximum load current is 14.2 A. Therefore:

$$W = \frac{14.2\ A}{0.05} = 284\ mils = 0.7213\ cm$$

Droop Resistor Length Calculation

$$L = \frac{R_{DROOP} \times W \times t}{\rho}$$

$$= \frac{0.0039 \times 284 \times 1.37}{717.86} = 2113\ mil = 5.36\ cm$$

Output Inductor

The inductor should be selected based on its inductance, current capability, and DC resistance. Increasing the inductor value will decrease output voltage ripple, but degrade transient response.

Inductor Ripple Current

$$\text{Ripple Current} = \frac{[(V_{IN} - V_{OUT}) \times V_{OUT}]}{(\text{Switching Frequency} \times L \times V_{IN})}$$

Example: V_{IN} = +5.0 V, V_{OUT} = +2.8 V, I_{LOAD} = 14.2 A, L = 1.2 μH, Freq = 200 kHz

$$\text{Ripple Current} = \frac{[(5.0\ V - 2.8\ V) \times 2.8\ V]}{[200\ kHz \times 1.2\ \mu H \times 5.0\ V]} = 5.1\ A$$

Output Ripple Voltage

V_{RIPPLE} = Inductor Ripple Current × Output Capacitor ESR

Example:

V_{IN} = +5.0 V, V_{OUT} = +2.8 V, I_{LOAD} = 14.2 A, L = 1.2 μH, Switching Frequency = 200 kHz

Output Ripple Voltage = 5.1 A × Output Capacitor ESR (from manufacturer's specs)

ESR of Output Capacitors to limit Output Voltage Spikes

$$ESR = \frac{\Delta V_{OUT}}{\Delta I_{OUT}}$$

This applies for current spikes that are faster than regulator response time. Printed Circuit Board resistance will add to the ESR of the output capacitors.

In order to limit spikes to 100 mV for a 14.2 A Load Step, ESR = 0.1/14.2 = 0.007 Ω

Inductor Peak Current

$$\text{Peak Current} = \text{Maximum Load Current} + \left(\frac{\text{Ripple Current}}{2}\right)$$

Example: V_{IN} = +5.0 V, V_{OUT} = +2.8 V, I_{LOAD} = 14.2 A, L = 1.2 μH, Freq = 200 kHz

$$\text{Peak Current} = 14.2\ \text{A} + (5.1/2) = 16.75\ \text{A}$$

A key consideration is that the inductor must be able to deliver the Peak Current at the switching frequency without saturating.

Response Time to Load Increase

(limited by Inductor value unless Maximum On−Time is exceeded)

$$\text{Response Time} = \frac{L \times \Delta I_{OUT}}{(V_{IN} - V_{OUT})}$$

Example: V_{IN} = +5.0 V, V_{OUT} = +2.8 V, L = 1.2 μH, 14.2 A change in Load Current

$$\text{Response Time} = \frac{1.2\ \mu\text{H} \times 14.2\ \text{A}}{(5.0\ \text{V} - 2.8\ \text{V})} = 7.7\ \mu\text{s}$$

Response Time to Load Decrease

(limited by Inductor value)

$$\text{Response Time} = \frac{L \times \text{Change in } I_{OUT}}{V_{OUT}}$$

Example: V_{OUT} = +2.8 V, 14.2 A change in Load Current, L = 1.2 μH

$$\text{Response Time} = \frac{1.2\ \mu\text{H} \times 14.2\ \text{A}}{2.8\ \text{V}} = 6.1\ \mu\text{s}$$

Input and Output Capacitors

These components must be selected and placed carefully to yield optimal results. Capacitors should be chosen to provide acceptable ripple on the input supply lines and regulator output voltage. Key specifications for input capacitors are their ripple rating, while ESR is important for output capacitors. For best transient response, a combination of low value/high frequency and bulk capacitors placed close to the load will be required.

THERMAL MANAGEMENT

Thermal Considerations for Power MOSFETs and Diodes

In order to maintain good reliability, the junction temperature of the semiconductor components should be kept to a maximum of 150°C or lower. The thermal impedance (junction to ambient) required to meet this requirement can be calculated as follows:

$$\text{Thermal Impedance} = \frac{T_{JUNCTION(MAX)} - T_{AMBIENT}}{\text{Power}}$$

A heatsink may be added to TO−220 components to reduce their thermal impedance. A number of PC board layout techniques such as thermal vias and additional copper foil area can be used to improve the power handling capability of surface mount components.

EMI Management

As a consequence of large currents being turned on and off at high frequency, switching regulators generate noise as a consequence of their normal operation. When designing for compliance with EMI/EMC regulations, additional components may be added to reduce noise emissions. These components are not required for regulator operation and experimental results may allow them to be eliminated. The input filter inductor may not be required because bulk filter and bypass capacitors, as well as other loads located on the board will tend to reduce regulator di/dt effects on the circuit board and input power supply. Placement of the power component to minimize routing distance will also help to reduce emissions.

Layout Guidelines

When laying out the CPU buck regulator on a printed circuit board, the following checklist should be used to ensure proper operation of the CS5165A.

1. Rapid changes in voltage across parasitic capacitors and abrupt changes in current in parasitic inductors are major concerns for a good layout.
2. Keep high currents out of logic grounds.
3. Avoid ground loops as they pick up noise. Use star or single point grounding. The source of the lower (synchronous FET) is an ideal point where the input and output GND planes can be connected.
4. For double−sided PCBs a single large ground plane is not recommended, since there is little control of where currents flow and the large surface area can act as an antenna.
5. Even though double sided PCBs are usually sufficient for a good layout, four−layer PCBs are the optimum approach to reducing susceptibility to noise. Use the two internal layers as the +5.0 V and GND planes, and the top and bottom layers for the vias.
6. Keep the inductor switching node small by placing the output inductor, switching and synchronous FETs close together.
7. The FET gate traces to the IC must be as short, straight, and wide as possible. Ideally, the IC has to be placed right next to the FETs.
8. Use fewer, but larger output capacitors, keep the capacitors clustered, and use multiple layer traces with heavy copper to keep the parasitic resistance low.
9. Place the switching FET as close to the +5.0 V input capacitors as possible.
10. Place the output capacitors as close to the load as possible.
11. Place the V_{FB} filter resistor in series with theV_{FB} pin (pin 16) right at the pin.
12. Place the V_{FB} filter capacitor right at the V_{FB} pin (pin 16).
13. The “Droop” Resistor (embedded PCB trace) has to be wide enough to carry the full load current.
14. Place the V_{CC} bypass capacitor as close as possible to the V_{CC} pin.

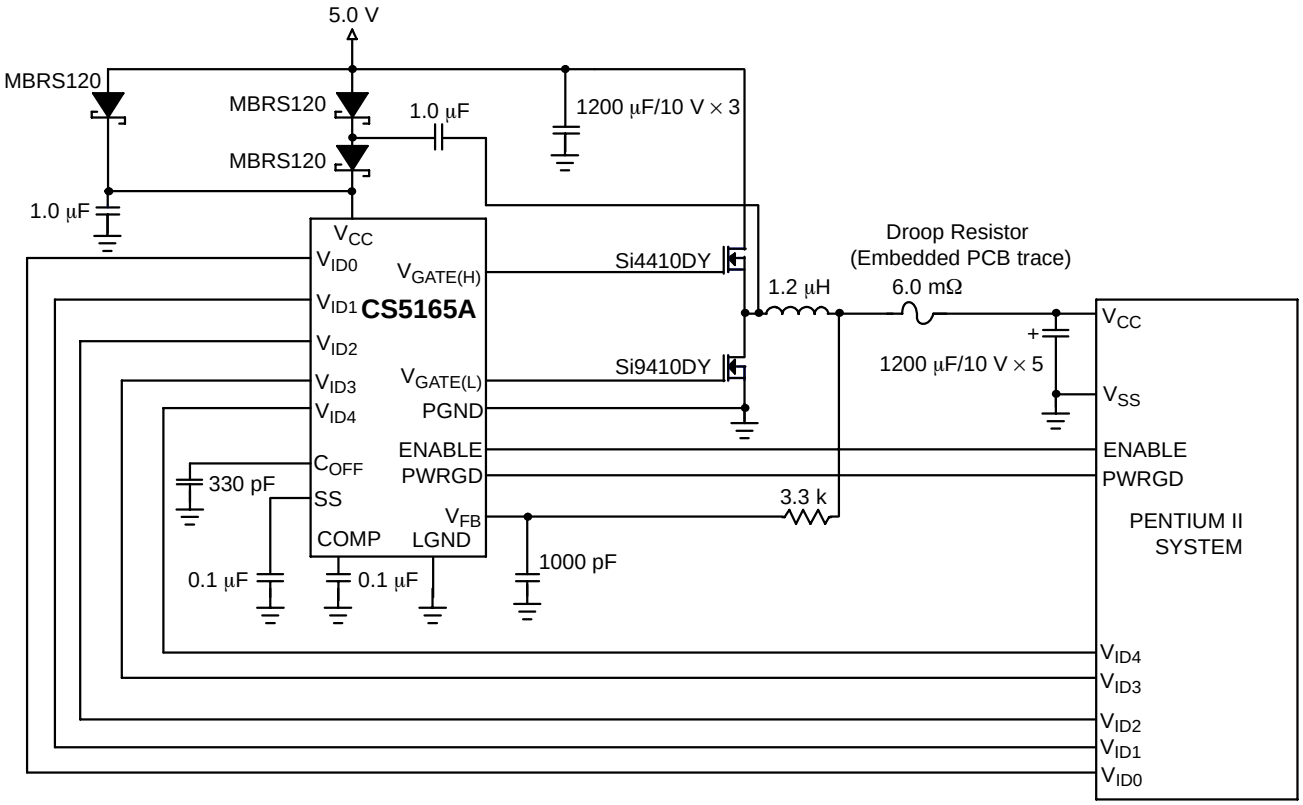


Figure 28. Additional Application Diagram, +5.0 V to +2.8 V @ 14.2 A for 300 MHz Pentium II

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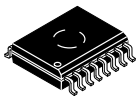

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SCALE 1:1

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ISSUE E

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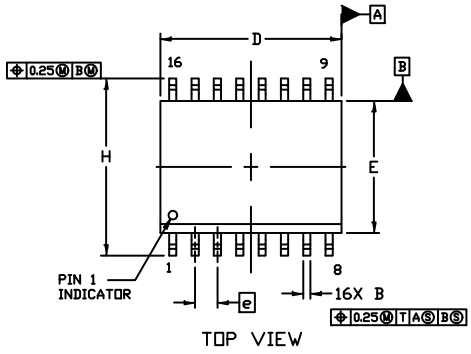
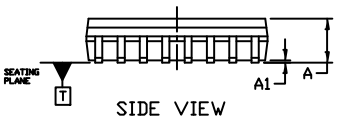
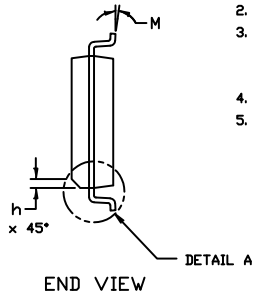


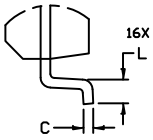
TOP VIEW



SIDE VIEW



END VIEW

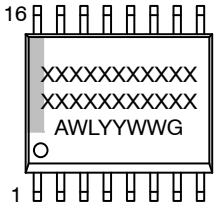


DETAIL A
2X SCALE

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION OR FLASH TO BE 0.15 PER SIDE.

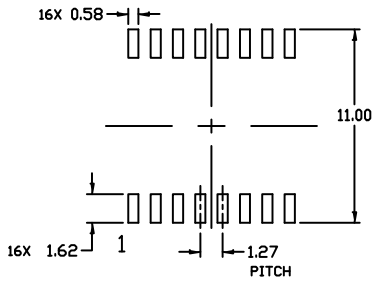
	MILLIMETERS	
DIM	MIN.	MAX.
A	2.35	2.65
A1	0.10	0.25
B	0.35	0.49
C	0.23	0.32
D	10.15	10.45
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.53 REF	
L	0.50	0.90
M	0°	7°

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.



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