DATA SHEET
www.onsemi.com

Dual PNP Bias Resistor Transistors R1 = 47 kΩ, R2 = 47 kΩ

PNP Transistors with Monolithic Bias Resistor Network

MUN5113DW1, NSBA144EDXV6, NSBA144EDP6

This series of digital transistors is designed to replace a single device and its external resistor bias network. The Bias Resistor Transistor (BRT) contains a single transistor with a monolithic bias network consisting of two resistors; a series base resistor and a base−emitter resistor. The BRT eliminates these individual components by integrating them into a single device. The use of a BRT can reduce both system cost and board space.

Features

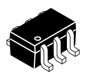
- Simplifies Circuit Design
- Reduces Board Space
- Reduces Component Count
- S and NSV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable*
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

MAXIMUM RATINGS

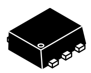
(T_A = 25°C, common for Q1 and Q2, unless otherwise noted)

Symbol	Rating	Max	Unit
V_{CBO}	Collector−Base Voltage	50	Vdc
V_{CEO}	Collector−Emitter Voltage	50	Vdc
I_C	Collector Current − Continuous	100	mAdc
$V_{IN(fwd)}$	Input Forward Voltage	40	Vdc
$V_{IN(rev)}$	Input Reverse Voltage	10	Vdc

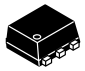
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.



SOT−363
CASE 419B

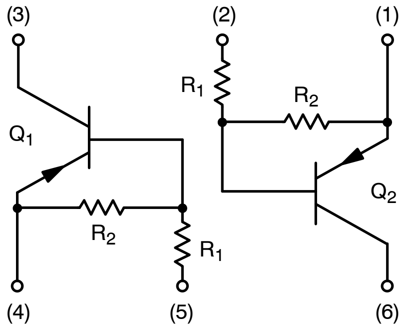


SOT−563
CASE 463A

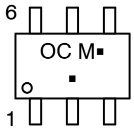


SOT−963
CASE 527AD

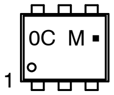
PIN CONNECTIONS



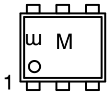
MARKING DIAGRAMS



SOT−363
CASE 419B



SOT−563
CASE 463A



SOT−963
CASE 527AD

0C/m = Specific Device Code
M = Date Code*
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*Date Code orientation may vary depending upon manufacturing location.

ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 6 of this data sheet.

NOTE: Some of the devices on this data sheet have been **DISCONTINUED**. Please refer to the table on page 6.

November, 2024 − Rev. 3

THERMAL CHARACTERISTICS

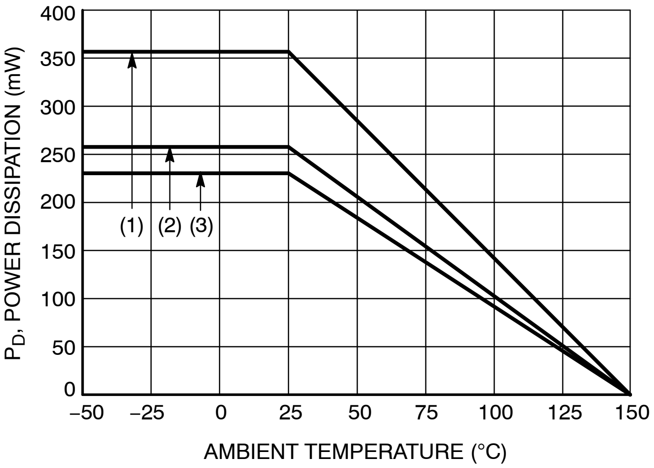
Symbol	Characteristic	Max	Unit
MUN5113DW1 (SOT−363) One Junction Heated			
P_D	Total Device Dissipation		
	T_A = 25°C (Note 1)	187	mW
	(Note 2)	256	
	Derate above 25°C (Note 1)	1.5	mW/°C
	(Note 2)	2.0	
$R_{\theta JA}$	Thermal Resistance, (Note 1)	670	°C/W
	Junction to Ambient (Note 2)	490	
MUN5113DW1 (SOT−363) Both Junction Heated (Note 3)			
P_D	Total Device Dissipation		
	T_A = 25°C (Note 1)	250	mW
	(Note 2)	385	
	Derate above 25°C (Note 1)	2.0	mW/°C
	(Note 2)	3.0	
$R_{\theta JA}$	Thermal Resistance, (Note 1)	493	°C/W
	Junction to Ambient (Note 2)	325	
$R_{\theta JL}$	Thermal Resistance, (Note 1)	188	°C/W
	Junction to Lead (Note 2)	208	
T_J, T_{stg}	Junction and Storage Temperature Range	−55 to +150	°C
NSBA144EDXV6 (SOT−563) One Junction Heated			
P_D	Total Device Dissipation		
	T_A = 25°C (Note 1)	357	mW
	Derate above 25°C (Note 1)	2.9	mW/°C
$R_{\theta JA}$	Thermal Resistance,		°C/W
	Junction to Ambient (Note 1)	350	
NSBA144EDXV6 (SOT−563) Both Junction Heated (Note 3)			
P_D	Total Device Dissipation		
	T_A = 25°C (Note 1)	500	mW
	Derate above 25°C (Note 1)	4.0	mW/°C
$R_{\theta JA}$	Thermal Resistance,		°C/W
	Junction to Ambient (Note 1)	250	
T_J, T_{stg}	Junction and Storage Temperature Range	−55 to +150	°C
NSBA144EDP6 (SOT−963) One Junction Heated			
P_D	Total Device Dissipation		
	T_A = 25°C (Note 4)	231	mW
	(Note 5)	269	
	Derate above 25°C (Note 4)	1.9	mW/°C
	(Note 5)	2.2	
$R_{\theta JA}$	Thermal Resistance, (Note 4)	540	°C/W
	Junction to Ambient (Note 5)	464	
NSBA144EDP6 (SOT−963) Both Junction Heated (Note 3)			
P_D	Total Device Dissipation		
	T_A = 25°C (Note 4)	339	mW
	(Note 5)	408	
	Derate above 25°C (Note 4)	2.7	mW/°C
	(Note 5)	3.3	
$R_{\theta JA}$	Thermal Resistance, (Note 4)	369	°C/W
	Junction to Ambient (Note 5)	306	
T_J, T_{stg}	Junction and Storage Temperature Range	−55 to +150	°C

1. FR−4 @ Minimum Pad.
2. FR−4 @ 1.0 x 1.0 Inch Pad.
3. Both junction heated values assume total power is sum of two equally powered channels.
4. FR−4 @ 100 mm^2, 1 oz. copper traces, still air.
5. FR−4 @ 500 mm^2, 1 oz. copper traces, still air.

ELECTRICAL CHARACTERISTICS (T_A = 25°C, common for Q_1 and Q_2, unless otherwise noted)

Symbol	Characteristic	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
I_{CBO}	Collector−Base Cutoff Current (V_{CB} = 50 V, I_E = 0)	–	–	100	nAdc
I_{CEO}	Collector−Emitter Cutoff Current (V_{CE} = 50 V, I_B = 0)	–	–	500	nAdc
I_{EBO}	Emitter−Base Cutoff Current (V_{EB} = 6.0 V, I_C = 0)	–	–	0.1	mAdc
$V_{(BR)CBO}$	Collector−Base Breakdown Voltage (I_C = 10 μA, I_E = 0)	50	–	–	Vdc
$V_{(BR)CEO}$	Collector−Emitter Breakdown Voltage (Note 6) (I_C = 2.0 mA, I_B = 0)	50	–	–	Vdc
ON CHARACTERISTICS					
h_{FE}	DC Current Gain (Note 6) (I_C = 5.0 mA, V_{CE} = 10 V)	80	140	–	
$V_{CE(sat)}$	Collector−Emitter Saturation Voltage (Note 6) (I_C = 10 mA, I_B = 0.3 mA)	–	–	0.25	Vdc
$V_{i(off)}$	Input Voltage (off) (V_{CE} = 5.0 V, I_C = 100 μA)	–	1.2	–	Vdc
$V_{i(on)}$	Input Voltage (on) (V_{CE} = 0.2 V, I_C = 3.0 mA)	–	2.0	–	Vdc
V_{OL}	Output Voltage (on) (V_{CC} = 5.0 V, V_B = 3.5 V, R_L = 1.0 kΩ)	–	–	0.2	Vdc
V_{OH}	Output Voltage (off) (V_{CC} = 5.0 V, V_B = 0.5 V, R_L = 1.0 kΩ)	4.9	–	–	Vdc
R1	Input Resistor	32.9	47	61.1	kΩ
R_1/R_2	Resistor Ratio	0.8	1.0	1.2	

6. Pulsed Condition: Pulse Width = 300 msec, Duty Cycle ≤ 2%.



(1) SOT−363; 1.0 x 1.0 inch Pad
(2) SOT−563; Minimum Pad
(3) SOT−963; 100 mm^2, 1 oz. copper trace

Figure 1. Derating Curve

TYPICAL CHARACTERISTICS
MUN5113DW1, NSBA144EDXV6

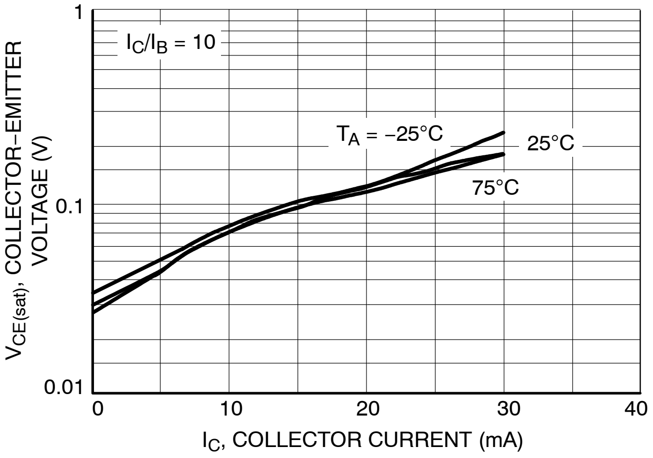


Figure 2. $V_{CE(sat)}$ vs. I_C

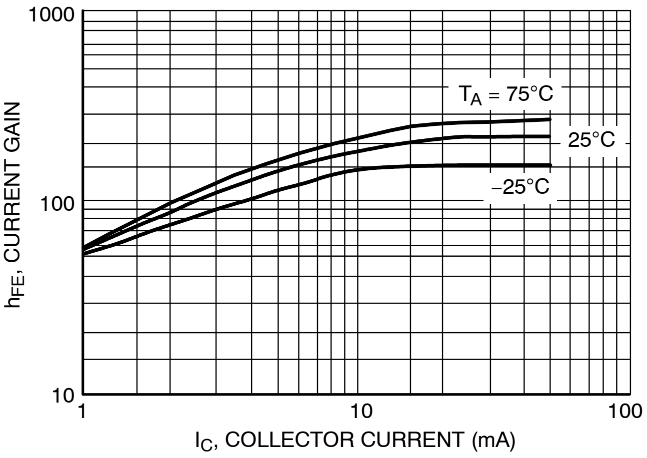


Figure 3. DC Current Gain

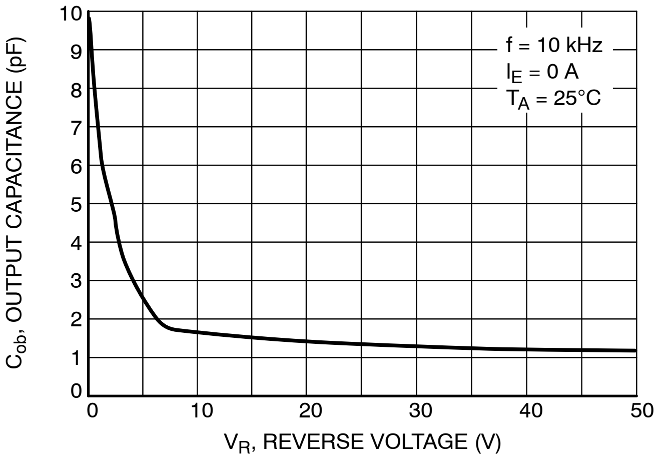


Figure 4. Output Capacitance

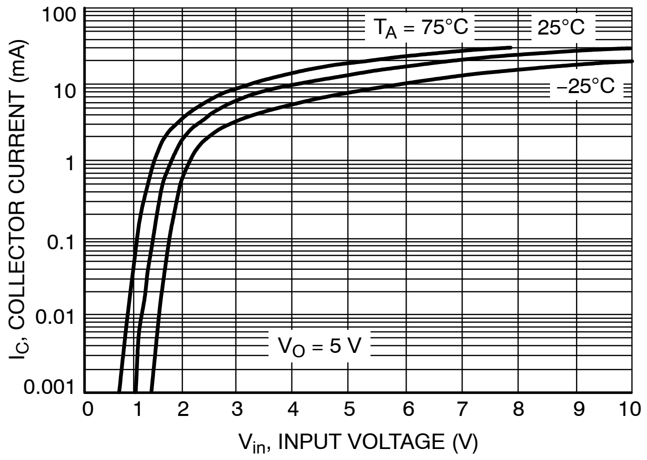


Figure 5. Output Current vs. Input Voltage

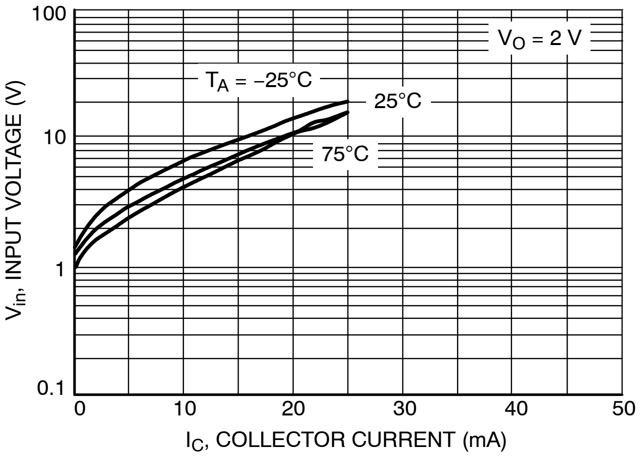


Figure 6. Input Voltage vs. Output Current

TYPICAL CHARACTERISTICS
NSBA144EDP6

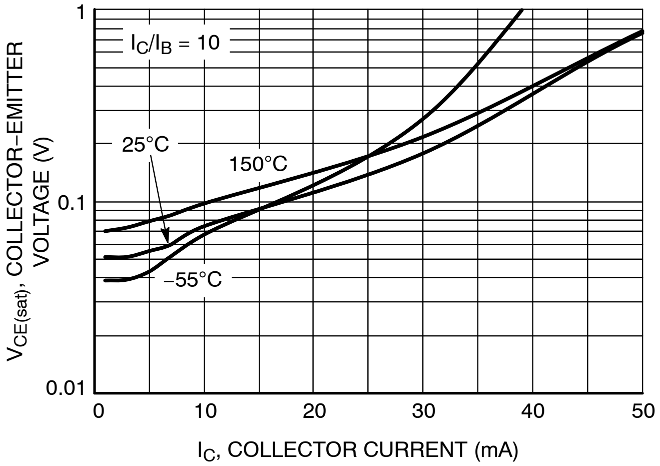


Figure 7. $V_{CE(sat)}$ vs. I_C

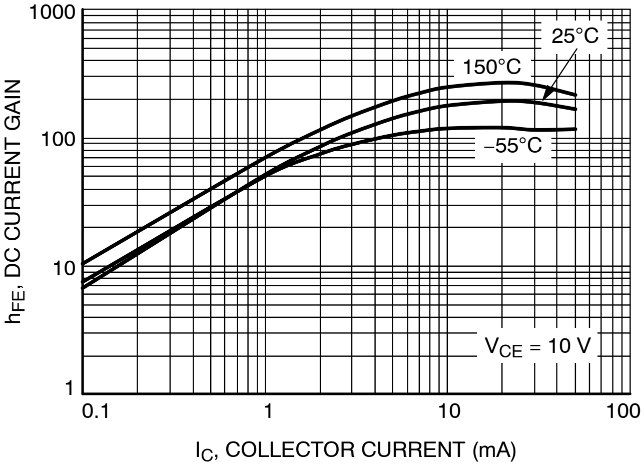


Figure 8. DC Current Gain

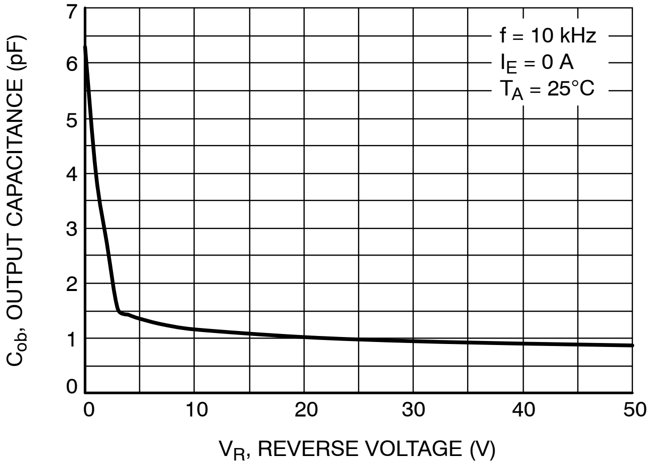


Figure 9. Output Capacitance

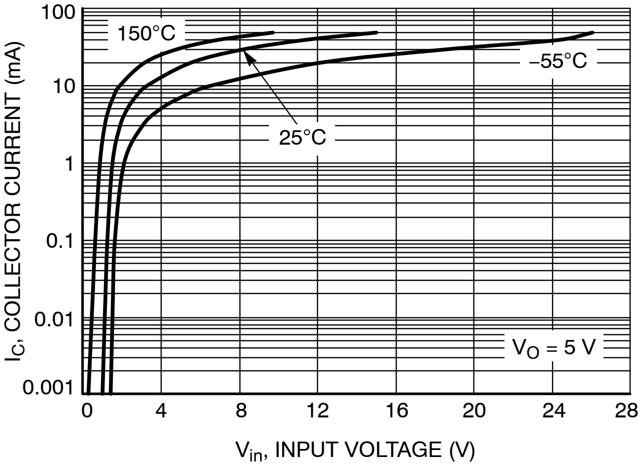


Figure 10. Output Current vs. Input Voltage

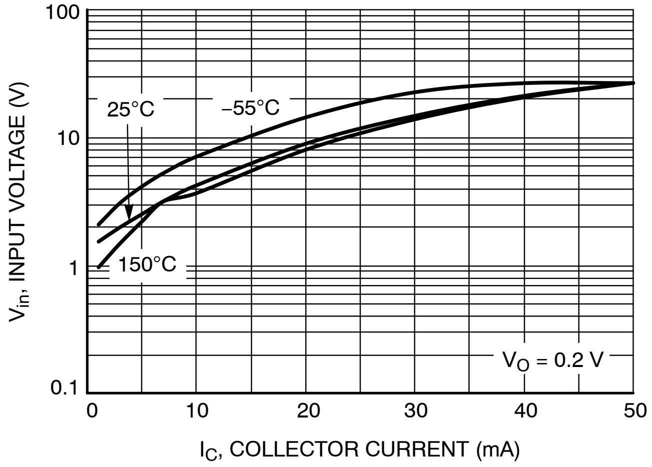


Figure 11. Input Voltage vs. Output Current

ORDERING INFORMATION

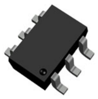
Device	Package	Shipping†
MUN5113DW1T1G, SMUN5113DW1T1G*	SOT−363	3,000 / Tape & Reel
NSVMUN5113DW1T3G*	SOT−363	10,000 / Tape & Reel
NSBA144EDXV6T1G	SOT−563	4,000 / Tape & Reel
NSBA144EDP6T5G	SOT−963	8,000 / Tape & Reel

DISCONTINUED (Note 7)

NSBA144EDXV6T5G	SOT−563	8,000 / Tape & Reel

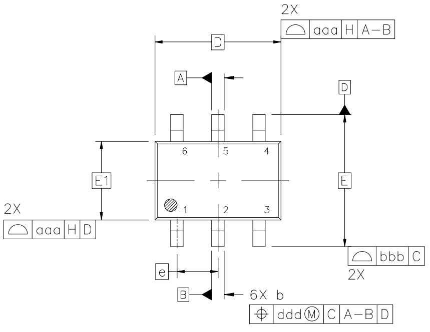
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

7. **DISCONTINUED:** This device is not recommended for new design. Please contact your **onsemi** representative for information. The most current information on this device may be available on www.onsemi.com.



SC−88 2.00x1.25x0.90, 0.65P
CASE 419B−02
ISSUE Z

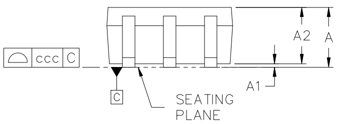
DATE 18 APR 2024



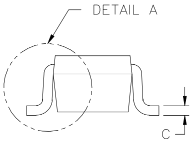
TOP VIEW

NOTES:

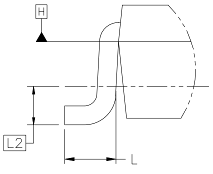
1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5−2018.
2. ALL DIMENSION ARE IN MILLIMETERS.
3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.20 PER END.
4. DIMENSIONS D AND E1 AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY AND DATUM H.
5. DATUMS A AND B ARE DETERMINED AT DATUM H.
6. DIMENSIONS b AND c APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.08 AND 0.15 FROM THE TIP.
7. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 TOTAL IN EXCESS OF DIMENSION b AT MAXIMUM MATERIAL CONDITION. THE DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT.



SIDE VIEW

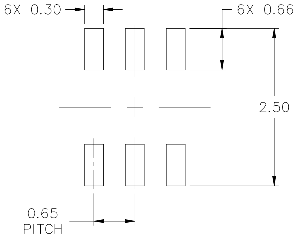


END VIEW



DETAIL A
SCALE 2:1

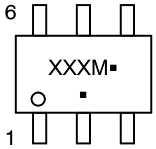
DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	−−−	−−−	1.10
A1	0.00	−−−	0.10
A2	0.70	0.90	1.00
b	0.15	0.20	0.25
c	0.08	0.15	0.22
D	2.00 BSC		
E	2.10 BSC		
E1	1.25 BSC		
e	0.65 BSC		
L	0.26	0.36	0.46
L2	0.15 BSC		
aaa	0.15		
bbb	0.30		
ccc	0.10		
ddd	0.10		



RECOMMENDED MOUNTING FOOTPRINT*

* FOR ADDITIONAL INFORMATION ON OUR Pb−FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ONSEMI SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXX = Specific Device Code
M = Date Code*
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*Date Code orientation and/or position may vary depending upon manufacturing location.

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

DOCUMENT NUMBER:	**98ASB42985B**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	**SC−88 2.00x1.25x0.90, 0.65P**	**PAGE 1 OF 2**

SC−88 2.00x1.25x0.90, 0.65P
CASE 419B−02
ISSUE Z

DATE 18 APR 2024

STYLE 1:
PIN 1. EMITTER 2
2. BASE 2
3. COLLECTOR 1
4. EMITTER 1
5. BASE 1
6. COLLECTOR 2

STYLE 2:
CANCELLED

STYLE 3:
CANCELLED

STYLE 4:
PIN 1. CATHODE
2. CATHODE
3. COLLECTOR
4. EMITTER
5. BASE
6. ANODE

STYLE 5:
PIN 1. ANODE
2. ANODE
3. COLLECTOR
4. EMITTER
5. BASE
6. CATHODE

STYLE 6:
PIN 1. ANODE 2
2. N/C
3. CATHODE 1
4. ANODE 1
5. N/C
6. CATHODE 2

STYLE 7:
PIN 1. SOURCE 2
2. DRAIN 2
3. GATE 1
4. SOURCE 1
5. DRAIN 1
6. GATE 2

STYLE 8:
CANCELLED

STYLE 9:
PIN 1. EMITTER 2
2. EMITTER 1
3. COLLECTOR 1
4. BASE 1
5. BASE 2
6. COLLECTOR 2

STYLE 10:
PIN 1. SOURCE 2
2. SOURCE 1
3. GATE 1
4. DRAIN 1
5. DRAIN 2
6. GATE 2

STYLE 11:
PIN 1. CATHODE 2
2. CATHODE 2
3. ANODE 1
4. CATHODE 1
5. CATHODE 1
6. ANODE 2

STYLE 12:
PIN 1. ANODE 2
2. ANODE 2
3. CATHODE 1
4. ANODE 1
5. ANODE 1
6. CATHODE 2

STYLE 13:
PIN 1. ANODE
2. N/C
3. COLLECTOR
4. EMITTER
5. BASE
6. CATHODE

STYLE 14:
PIN 1. VREF
2. GND
3. GND
4. IOUT
5. VEN
6. VCC

STYLE 15:
PIN 1. ANODE 1
2. ANODE 2
3. ANODE 3
4. CATHODE 3
5. CATHODE 2
6. CATHODE 1

STYLE 16:
PIN 1. BASE 1
2. EMITTER 2
3. COLLECTOR 2
4. BASE 2
5. EMITTER 1
6. COLLECTOR 1

STYLE 17:
PIN 1. BASE 1
2. EMITTER 1
3. COLLECTOR 2
4. BASE 2
5. EMITTER 2
6. COLLECTOR 1

STYLE 18:
PIN 1. VIN1
2. VCC
3. VOUT2
4. VIN2
5. GND
6. VOUT1

STYLE 19:
PIN 1. I OUT
2. GND
3. GND
4. V CC
5. V EN
6. V REF

STYLE 20:
PIN 1. COLLECTOR
2. COLLECTOR
3. BASE
4. EMITTER
5. COLLECTOR
6. COLLECTOR

STYLE 21:
PIN 1. ANODE 1
2. N/C
3. ANODE 2
4. CATHODE 2
5. N/C
6. CATHODE 1

STYLE 22:
PIN 1. D1 (i)
2. GND
3. D2 (i)
4. D2 (c)
5. VBUS
6. D1 (c)

STYLE 23:
PIN 1. Vn
2. CH1
3. Vp
4. N/C
5. CH2
6. N/C

STYLE 24:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE

STYLE 25:
PIN 1. BASE 1
2. CATHODE
3. COLLECTOR 2
4. BASE 2
5. EMITTER
6. COLLECTOR 1

STYLE 26:
PIN 1. SOURCE 1
2. GATE 1
3. DRAIN 2
4. SOURCE 2
5. GATE 2
6. DRAIN 1

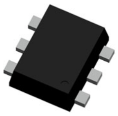
STYLE 27:
PIN 1. BASE 2
2. BASE 1
3. COLLECTOR 1
4. EMITTER 1
5. EMITTER 2
6. COLLECTOR 2

STYLE 28:
PIN 1. DRAIN
2. DRAIN
3. GATE
4. SOURCE
5. DRAIN
6. DRAIN

STYLE 29:
PIN 1. ANODE
2. ANODE
3. COLLECTOR
4. EMITTER
5. BASE/ANODE
6. CATHODE

STYLE 30:
PIN 1. SOURCE 1
2. DRAIN 2
3. DRAIN 2
4. SOURCE 2
5. GATE 1
6. DRAIN 1

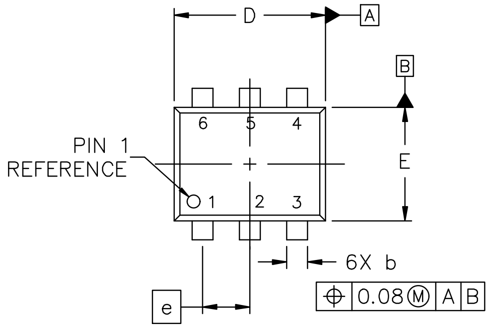
Note: Please refer to datasheet for style callout. If style type is not called out in the datasheet refer to the device datasheet pinout or pin assignment.



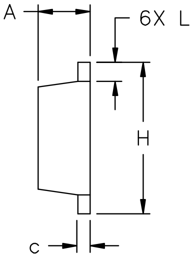
SOT-563-6 1.60x1.20x0.55, 0.50P
CASE 463A
ISSUE J

DATE 15 FEB 2024

NOTES:
1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5-2018.
2. ALL DIMENSION ARE IN MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.

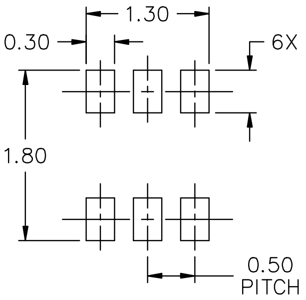


TOP VIEW



SIDE VIEW

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.50	0.55	0.60
b	0.17	0.22	0.27
c	0.08	0.13	0.18
D	1.50	1.60	1.70
E	1.10	1.20	1.30
e	0.50 BSC		
H	1.50	1.60	1.70
L	0.10	0.20	0.30



RECOMMENDED MOUNTING FOOTPRINT*

* FOR ADDITIONAL INFORMATION ON OUR Pb-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

STYLE 1:
PIN 1. EMITTER 1
2. BASE 1
3. COLLECTOR 2
4. EMITTER 2
5. BASE 2
6. COLLECTOR 1

STYLE 2:
PIN 1. EMITTER 1
2. EMITTER 2
3. BASE 2
4. COLLECTOR 2
5. BASE 1
6. COLLECTOR 1

STYLE 3:
PIN 1. CATHODE 1
2. CATHODE 1
3. ANODE/ANODE 2
4. CATHODE 2
5. CATHODE 2
6. ANODE/ANODE 1

STYLE 4:
PIN 1. COLLECTOR
2. COLLECTOR
3. BASE
4. EMITTER
5. COLLECTOR
6. COLLECTOR

STYLE 5:
PIN 1. CATHODE
2. CATHODE
3. ANODE
4. ANODE
5. CATHODE
6. CATHODE

STYLE 6:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE

STYLE 7:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. CATHODE
5. ANODE
6. CATHODE

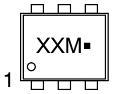
STYLE 8:
PIN 1. DRAIN
2. DRAIN
3. GATE
4. SOURCE
5. DRAIN
6. DRAIN

STYLE 9:
PIN 1. SOURCE 1
2. GATE 1
3. DRAIN 2
4. SOURCE 2
5. GATE 2
6. DRAIN 1

STYLE 10:
PIN 1. CATHODE 1
2. N/C
3. CATHODE 2
4. ANODE 2
5. N/C
6. ANODE 1

STYLE 11:
PIN 1. EMITTER 2
2. BASE 2
3. COLLECTOR 1
4. EMITTER 1
5. BASE 1
6. COLLECTOR 2

GENERIC
MARKING DIAGRAM*



XX = Specific Device Code
M = Month Code
▪ = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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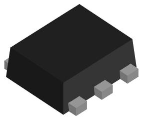
DESCRIPTION:	**SOT-563-6 1.60x1.20x0.55, 0.50P**	**PAGE 1 OF 1**

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

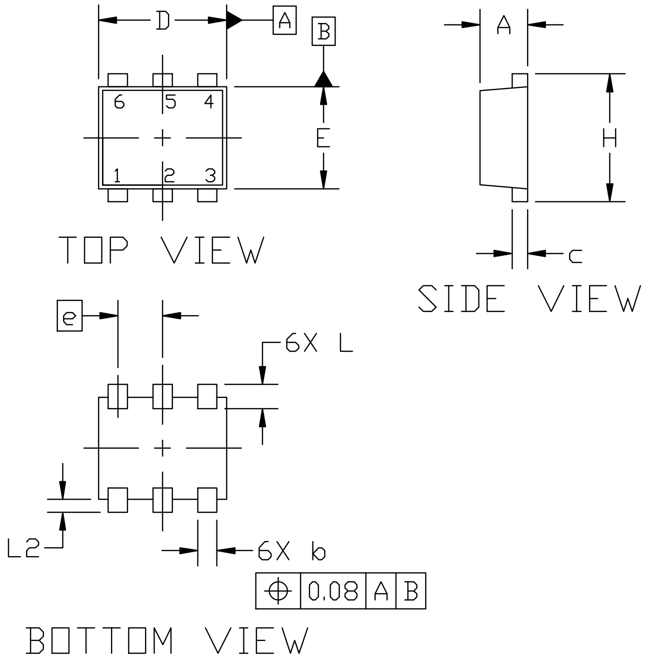


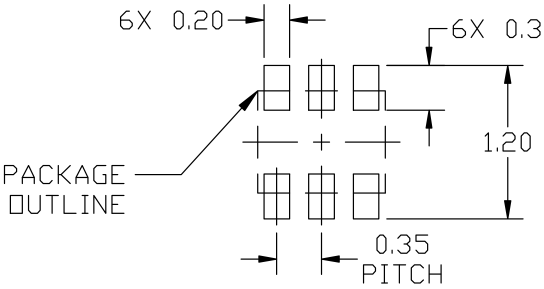
SOT−963 1.00x1.00x0.37, 0.35P
CASE 527AD
ISSUE F

DATE 20 FEB 2024

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

	MILLIMETERS		
DIM	MIN.	NOM.	MAX.
A	0.34	0.37	0.40
b	0.10	0.15	0.20
c	0.07	0.12	0.17
D	0.95	1.00	1.05
E	0.75	0.80	0.85
e	0.35 BSC		
H	0.95	1.00	1.05
L	0.19 REF		
L2	0.05	0.10	0.15





RECOMMENDED MOUNTING FOOTPRINT

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference manual, SOLDERRM/D.

STYLE 1:
- PIN 1. EMITTER 1
- 2. BASE 1
- 3. COLLECTOR 2
- 4. EMITTER 2
- 5. BASE 2
- 6. COLLECTOR 1

STYLE 2:
- PIN 1. EMITTER 1
- 2. EMITTER2
- 3. BASE 2
- 4. COLLECTOR 2
- 5. BASE 1
- 6. COLLECTOR 1

STYLE 3:
- PIN 1. CATHODE 1
- 2. CATHODE 1
- 3. ANODE/ANODE 2
- 4. CATHODE 2
- 5. CATHODE 2
- 6. ANODE/ANODE 1

STYLE 4:
- PIN 1. COLLECTOR
- 2. COLLECTOR
- 3. BASE
- 4. EMITTER
- 5. COLLECTOR
- 6. COLLECTOR

STYLE 5:
- PIN 1. CATHODE
- 2. CATHODE
- 3. ANODE
- 4. ANODE
- 5. CATHODE
- 6. CATHODE

STYLE 6:
- PIN 1. CATHODE
- 2. ANODE
- 3. CATHODE
- 4. CATHODE
- 5. CATHODE
- 6. CATHODE

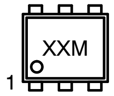
STYLE 7:
- PIN 1. CATHODE
- 2. ANODE
- 3. CATHODE
- 4. CATHODE
- 5. ANODE
- 6. CATHODE

STYLE 8:
- PIN 1. DRAIN
- 2. DRAIN
- 3. GATE
- 4. SOURCE
- 5. DRAIN
- 6. DRAIN

STYLE 9:
- PIN 1. SOURCE 1
- 2. GATE 1
- 3. DRAIN 2
- 4. SOURCE 2
- 5. GATE 2
- 6. DRAIN 1

STYLE 10:
- PIN 1. CATHODE 1
- 2. N/C
- 3. CATHODE 2
- 4. ANODE 2
- 5. N/C
- 6. ANODE 1

GENERIC MARKING DIAGRAM*



XX = Specific Device Code
M = Month Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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