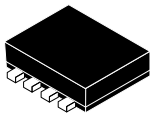
MOSFET – Power, P-Channel, Dual ECH8

-20 V, -5 A, 38 mΩ

ECH8654



SOT−28FL / ECH8
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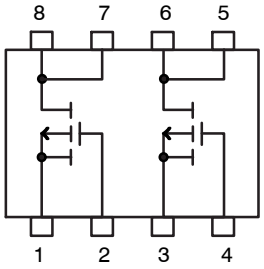
Features

- Low ON−resistance
- 1.8 V Drive
- Halogen Free Compliance
- Protection Diode in

MARKING DIAGRAM

ELECTRICAL CONNECTION



1: Source 1
2: Gate 1
3: Source 2
4: Gate 2
5: Drain 2
6: Drain 2
7: Drain 1
8: Drain 1

ABSOLUTE MAXIMUM RATINGS (at Ta = 25°C)

Parameter	Symbol	Conditions	Ratings	Unit
Drain−to−Source Voltage	V_{DSS}		−20	V
Gate−to−Source Voltage	V_{GSS}		±10	V
Drain Current (DC)	I_D		−5	A
Drain Current (Pulse)	I_{DP}	PW ≤ 10 μs, duty cycle ≤ 1%	−40	A
Allowable Power Dissipation	P_D	When mounted on ceramic substrate (900 mm^2 × 0.8 mm) 1 unit	1.3	W
Total Power Dissipation	P_T	When mounted on ceramic substrate (900 mm^2 × 0.8 mm)	1.5	W
Channel Temperature	Tch		150	°C
Storage Temperature	Tstg		−55 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

ORDERING INFORMATION

Device	Package	Shipping†
ECH8654−TL−H	SOT−28FL / ECH8 (Pb−Free and Halide Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

ELECTRICAL CHARACTERISTICS (at Ta = 25°C)

Parameter	Symbol	Conditions	Ratings			Unit
			Min	Typ	Max	
Drain−to−Source Breakdown Voltage	$V_{(BR)DSS}$	I_D = −1 mA, V_{GS} = 0 V	−20	–	–	V
Zero−Gate Voltage Drain Current	I_{DSS}	V_{DS} = −20 V, V_{GS} = 0 V	–	–	−1	μA
Gate−to−Source Leakage Current	I_{GSS}	V_{GS} = ±8 V, V_{DS} = 0 V	–	–	±10	μA
Cutoff Voltage	V_{GS}(off)	V_{DS} = −10 V, I_D = −1 mA	−0.4	–	−1.3	V
Forward Transfer Admittance	| yfs |	V_{DS} = −10 V, I_D = −3 A	4.9	8.3	–	S
Static Drain−to−Source On−State Resistance	R_{DS}(on)1	I_D = −3 A, V_{GS} = −4.5 V	–	29	38	mΩ
	R_{DS}(on)2	I_D = −1.5 A, V_{GS} = −2.5 V	–	41	58	mΩ
	R_{DS}(on)3	I_D = −0.5 A, V_{GS} = −1.8 V	–	64	98	mΩ
Input Capacitance	Ciss	V_{DS} = −10 V, f = 1 MHz	–	960	–	pF
Output Capacitance	Coss		–	180	–	pF
Reverse Transfer Capacitance	Crss		–	140	–	pF
Turn−ON Delay Time	t_d(on)	See specified Test Circuit.	–	14	–	ns
Rise Time	t_r		–	55	–	ns
Turn−OFF Delay Time	t_d(off)		–	92	–	ns
Fall Time	t_f		–	68	–	ns
Total Gate Charge	Qg	V_{DS} = −10 V, V_{GS} = −4.5 V, I_D = −5 A	–	11	–	nC
Gate−to−Source Charge	Qgs		–	2.0	–	nC
Gate−to−Drain “Miller” Charge	Qgd		–	2.8	–	nC
Diode Forward Voltage	V_{SD}	I_S = −5 A, V_{GS} = 0 V	–	−0.82	−1.2	V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

Switching Time Test Circuit

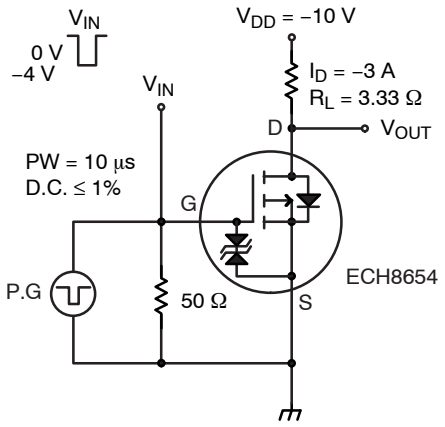


Figure 1. Switching Time Test Circuit

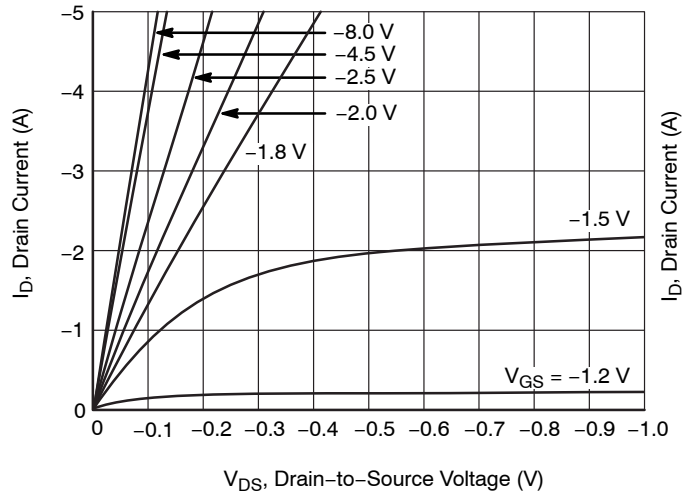


Figure 2. I_D – V_{DS}

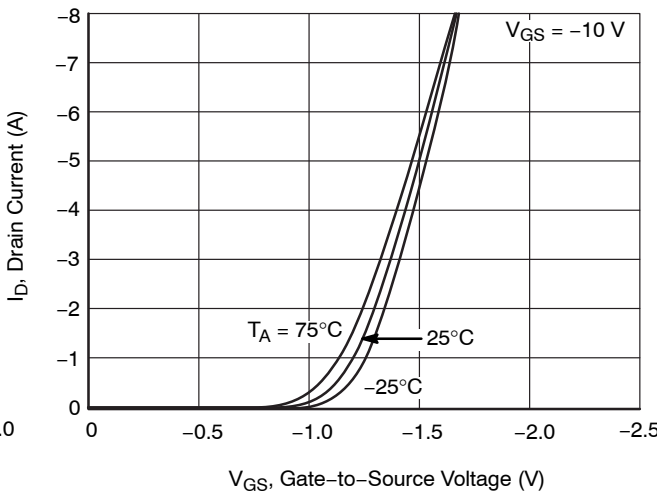


Figure 3. I_D – V_{GS}

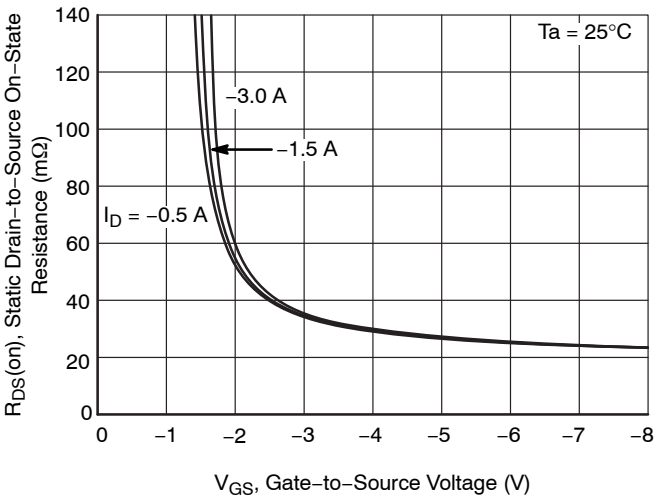


Figure 4. $R_{DS(on)}$ – V_{GS}

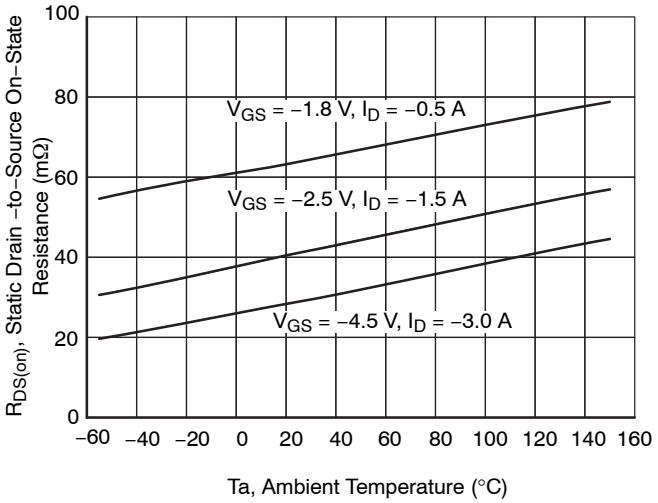


Figure 5. $R_{DS(on)}$ – Ta

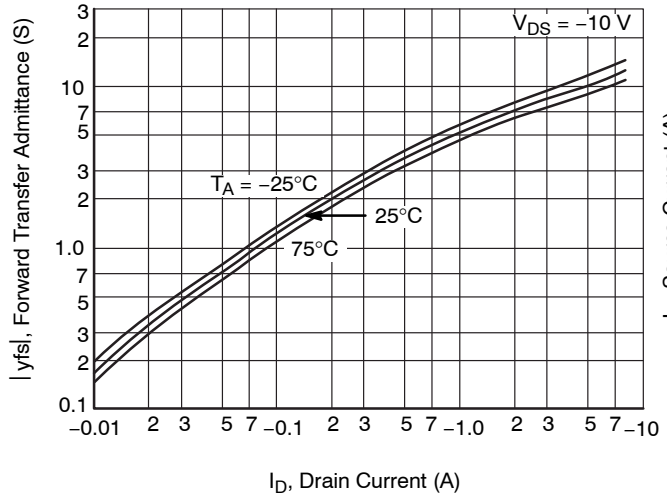


Figure 6. $|yfs|$ – I_D

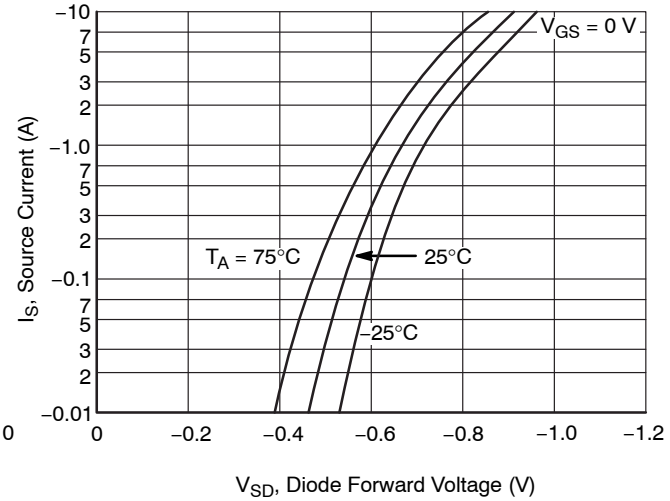


Figure 7. I_S – V_{SD}

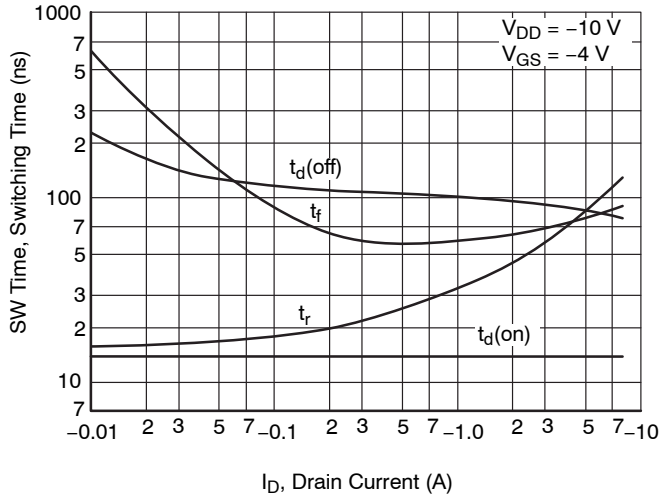


Figure 8. SW Time – I_D

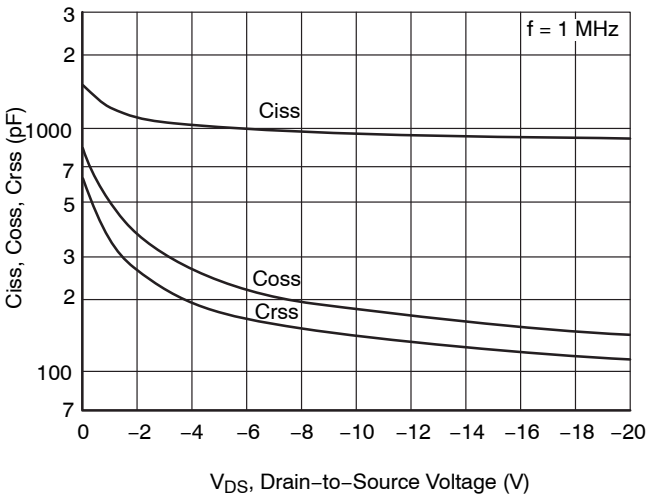


Figure 9. Ciss, Coss, Crss – V_{DS}

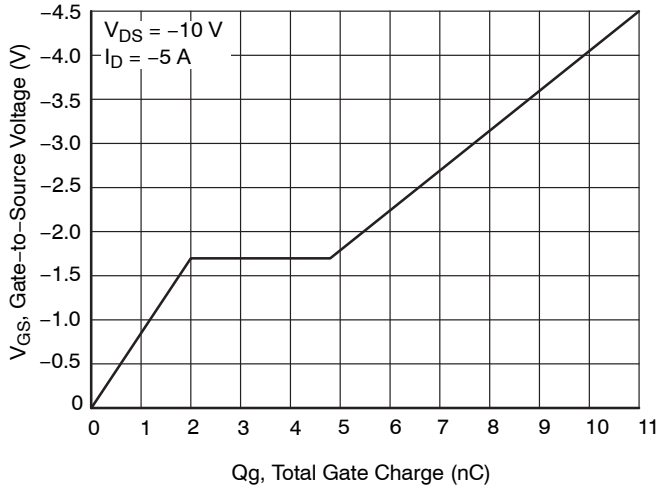


Figure 10. V_{GS} – Qg

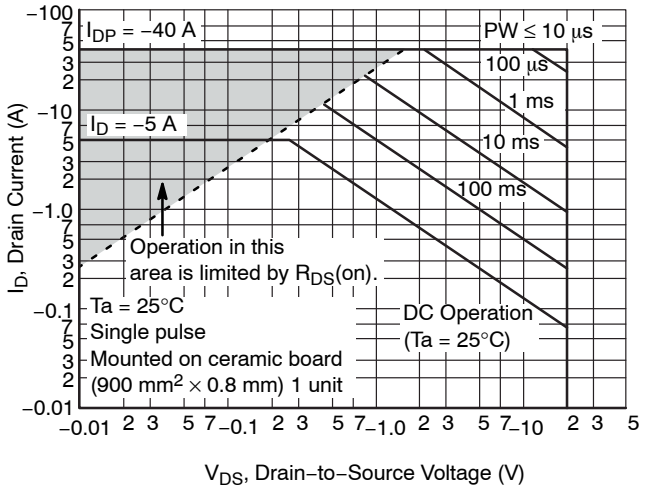


Figure 11. ASO

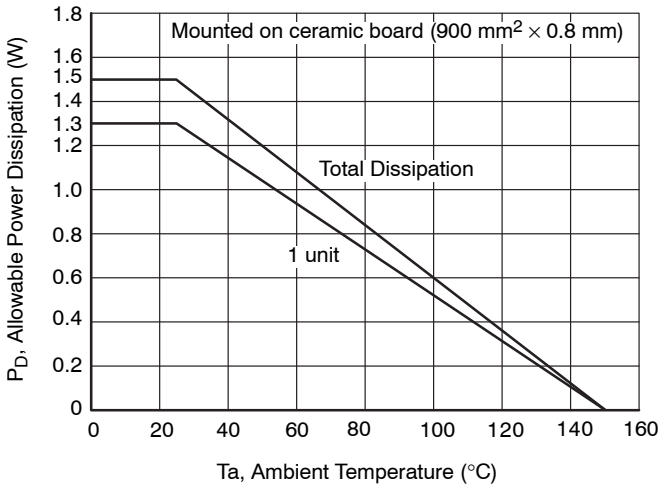


Figure 12. P_D – Ta

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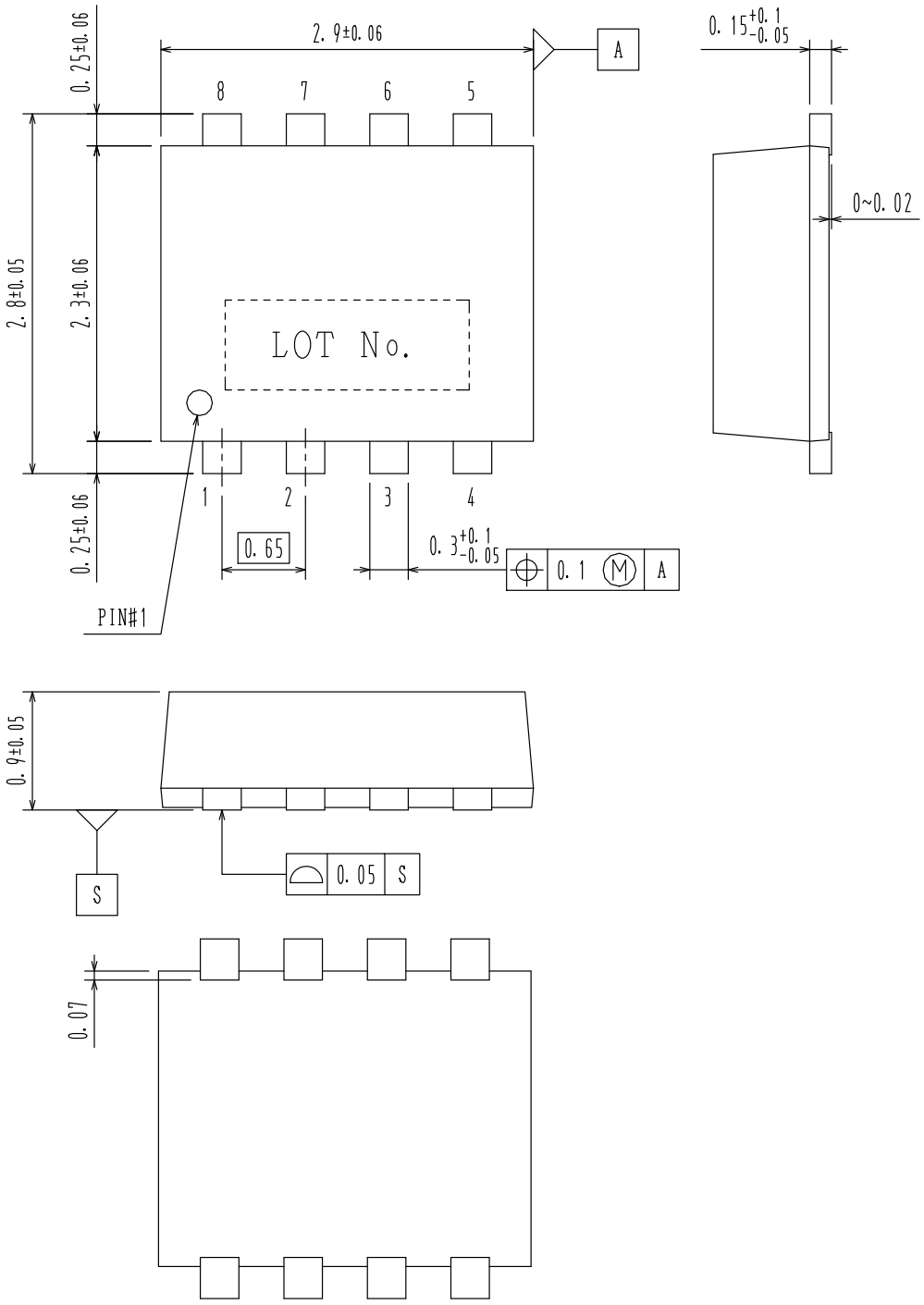
DATE 31 MAR 2012



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