Boost Converter Stage in APM16 Series for Multiphase and Semi-Bridgeless PFC

FAM65CR51XZ1, FAM65CR51XZ2

ON Semiconductor®

www.onsemi.com

Features

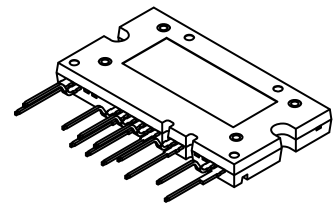
- Integrated SIP or DIP Boost Converter Stage Power Module for On−board Charger (OBC) in EV or PHEV
- 5 kV/1 sec Electrically Isolated Substrate for Easy Assembly
- Creepage and Clearance per IEC60664−1, IEC 60950−1
- Compact Design for Low Total Module Resistance
- Module Serialization for Full Traceability
- Low Thermal Resistance Due to the Used ALN Substrate
- AEC−Q101 & AQG324 Qualified and PPAP Capable
- UL94V−0 Compliant
- These Devices are Pb−Free and are RoHS Compliant

Applications

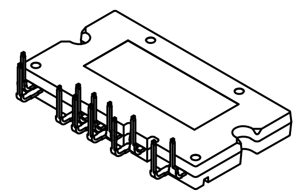
- PFC Stage of an On−board Charger in PHEV or EV

Benefits

- Enable Design of Small, Efficient and Reliable System for Reduced Vehicle Fuel Consumption and CO_2 Emission
- Simplified Assembly, Optimized Layout, High Level of Integration, and Improved Thermal Performance



APMCD−A16 / 12LD, AUTOMOTIVE MODULE CASE MODGG



APMCD−B16 / 12LD, AUTOMOTIVE MODULE CASE MODGK

MARKING DIAGRAM

```
XXXXXXXXXXX
ZZZ ATYWW
NNNNNNN
```

XXXX	= Specific Device Code
ZZZ	= Lot ID
AT	= Assembly & Test Location
Y	= Year
WW	= Work Week
NNN	= Serial Number

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

ORDERING INFORMATION

Part Number	Package	Lead Forming	DBC Material	Pb−Free and RoHS Compliant	Operating Temperature (Ta)	Shipping
FAM65CR51XZ1	APMCD−A16	Y−Shape	AlN	Yes	−40°C~125°C	72 Units / Tube
FAM65CR51XZ2	APMCD−B16	L−Shape	AlN	Yes	−40°C~125°C	72 Units / Tube

Pin Configuration and Block Description

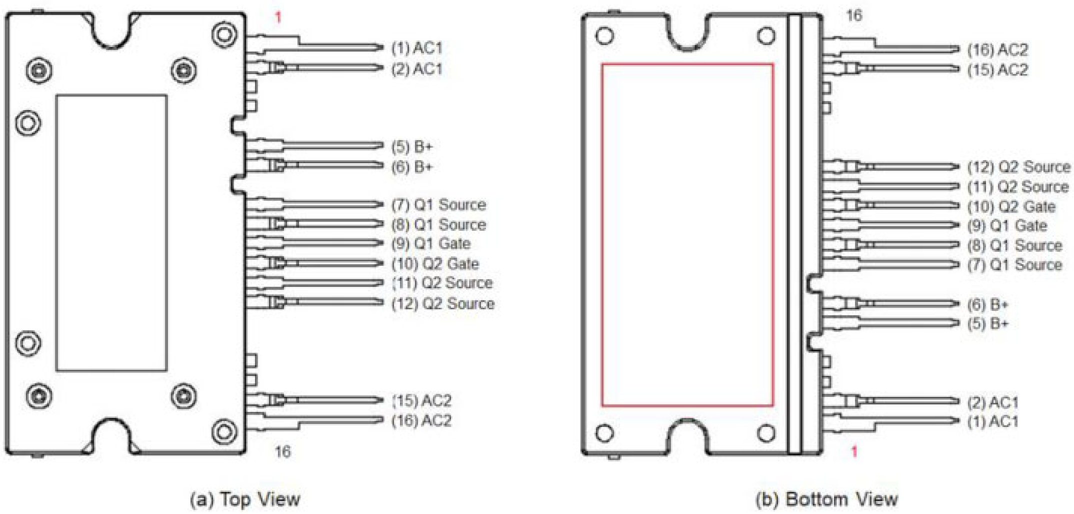


Figure 1. Pin Configuration

Table 1. PIN DESCRIPTION

Pin No.	Name	Description
1, 2	AC1	Phase 1 Leg of the PFC Bridge
3	NC	Not Connected
4	NC	Not Connected
5, 6	B+	Positive Battery Terminal
7, 8	Q1 Source	Source Terminal of Q1
9	Q1 Gate	Gate Terminal of Q1
10	Q2 Gate	Gate Terminal of Q2
11, 12	Q2 Source	Source Terminal of Q2
13	NC	Not Connected
14	NC	Not Connected
15, 16	AC2	Phase 2 Leg of the PFC Bridge

INTERNAL EQUIVALENT CIRCUIT

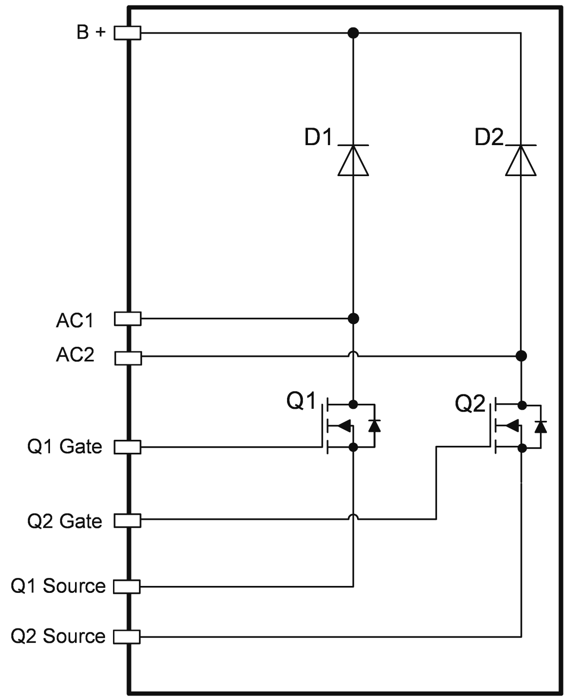


Figure 2. Internal Block Diagram

Table 2. ABSOLUTE MAXIMUM RATINGS OF MOSFET (T_J = 25°C unless otherwise noted)

Symbol	Parameter	Max	Unit
V_{DS} (Q1~Q2)	Drain−to−Source Voltage	650	V
V_{GS} (Q1~Q2)	Gate−to−Source Voltage	±20	V
I_D (Q1~Q2)	Drain Current Continuous (T_C = 25°C, V_{GS} = 10 V) (Note 1)	64	A
	Drain Current Continuous (T_C = 100°C, V_{GS} = 10 V) (Note 1)	40	A
E_{AS} (Q1~Q2)	Single Pulse Avalanche Energy (Note 2)	623	mJ
P_D	Power Dissipation (T_C = 25°C, V_{GS} = 10 V) (Note 1)	463	W
T_J	Maximum Junction Temperature	−55 to +150	°C
T_C	Maximum Case Temperature	−40 to +125	°C
T_{STG}	Storage Temperature	−40 to +125	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Maximum continuous current and power, without switching losses, to reach T_J = 150°C respectively at T_C = 25°C and T_C = 100°C; defined by design based on MOSFET $R_{DS(ON)}$ and max. $R_{\theta JC}$ and not subject to production test
2. Starting T_J = 25°C, I_{AS} = 6.5 A, R_G = 25 Ω

DBC Substrate

0.63 mm AlN with 0.3 mm copper on both sides. DBC substrate is NOT nickel plated.

Lead Frame

OFC copper alloy, 0.50 mm thick. Plated with 8 μm to 25.4 μm thick Matte Tin.

Flammability Information

All materials present in the power module meet UL flammability rating class 94V−0.

Compliance to RoHS Directives

The power module is 100% lead free and RoHS compliant 2000/53/C directive.

Solder

Solder used is a lead free SnAgCu alloy. Solder presents high risk to melt at temperature beyond 210°C. Base of the leads, at the interface with the package body, should not be exposed to more than 200°C during mounting on the PCB or during welding to prevent the re−melting of the solder joints

Table 3. ELECTRICAL SPECIFICATIONS OF MOSFET (T_J = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
BV_{DSS}	Drain−to−Source Breakdown Voltage	I_D = 1 mA, V_{GS} = 0 V	650	–	–	V
$V_{GS(th)}$	Gate−to−Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 3.3 mA	3.0	–	5.0	V
$R_{DS(ON)}$ Q1	Q1 Low Side MOSFET	V_{GS} = 10 V, I_D = 20 A	–	44	51	mΩ
$R_{DS(ON)}$ Q2	Q2 Low Side MOSFET		–	44	51	mΩ
$R_{DS(ON)}$ Q1	Q1 Low Side MOSFET	V_{GS} = 10 V, I_D = 20 A, T_J = 125°C (Note 3)	–	79	–	mΩ
$R_{DS(ON)}$ Q2	Q2 Low Side MOSFET		–	79	–	mΩ
g_{FS}	Forward Transconductance	V_{DS} = 20 V, I_D = 20 A (Note 3)	–	30	–	S
I_{GSS}	Gate−to−Source Leakage Current	V_{GS} = ±20 V, V_{DS} = 0 V	−100	–	+100	nA
I_{DSS}	Drain−to−Source Leakage Current	V_{DS} = 650 V, V_{GS} = 0 V	–	–	10	μA
DYNAMIC CHARACTERISTICS (Note 3)						
C_{iss}	Input Capacitance	V_{DS} = 400 V, V_{GS} = 0 V, f = 1 MHz	–	4864	–	pF
C_{oss}	Output Capacitance		–	109	–	pF
C_{rss}	Reverse Transfer Capacitance		–	16	–	pF
$C_{oss(eff)}$	Effective Output Capacitance	V_{DS} = 0 to 520 V, V_{GS} = 0 V	–	652	–	pF
R_g	Gate Resistance	f = 1 MHz	–	2	–	Ω
$Q_{g(tot)}$	Total Gate Charge	V_{DS} = 380 V, I_D = 20 A, V_{GS} = 0 to 10 V	–	123	–	nC
Q_{gs}	Gate−to−Source Gate Charge		–	37.5	–	nC
Q_{gd}	Gate−to−Drain “Miller” Charge		–	49	–	nC
SWITCHING CHARACTERISTICS (Note 3)						
t_{on}	Turn−on Time	V_{DS} = 400 V, I_D = 20 A, V_{GS} = 10 V, R_G = 4.7 Ω	–	87	–	ns
$t_{d(on)}$	Turn−on Delay Time		–	47	–	ns
t_r	Turn−on Rise Time		–	43	–	ns
t_{off}	Turn−off Time		–	146	–	ns
$t_{d(off)}$	Turn−off Delay Time		–	118	–	ns
t_f	Turn−off Fall Time		–	29	–	ns
BODY DIODE CHARACTERISTICS						
V_{SD}	Source−to−Drain Diode Voltage	I_{SD} = 20 A, V_{GS} = 0 V	–	0.95	–	V
T_{rr}	Reverse Recovery Time	V_{DS} = 520 V, I_D = 20 A, d_I/d_t = 100 A/μs (Note 3)	–	133	–	ns
Q_{rr}	Reverse Recovery Charge		–	669	–	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Defined by design, not subject to production test

Table 4. ABSOLUTE MAXIMUM RATINGS OF THE BOOST DIODE (T_J = 25°C unless otherwise noted) (Note 4)

Symbol	Parameter	Max	Unit
V_{RRM}	Peak Repetitive Reverse Voltage (Note 5)	600	V
V_{RWM}	Working Peak Reverse Voltage (Note 5)	600	V
V_R	DC Blocking Voltage	600	V
$I_{F(AV)}$	Average Rectified Forward Current T_C = 25°C	15	A
I_{FSM}	Non−Repetitive Peak Surge Current (Half Wave 1 Phase 60 Hz)	45	A
T_J	Maximum Junction Temperature	−55 to +175	°C
T_C	Maximum Case Temperature	−40 to +125	°C
T_{STG}	Storage Temperature	−40 to +125	°C
E_{AVL}	Avalanche Energy (2.85 A, 1 mH)	4	mJ

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
4. Defined by design, not subject to production test
5. V_{RRM} and $I_{F(AV)}$ value referenced to TO220−2L Auto Qualified Package Device ISL9R1560P_F085

Table 5. ELECTRICAL SPECIFICATIONS OF THE BOOST DIODE (T_J = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions		Min	Typ	Max	Unit
I_R	Instantaneous Reverse Current	V_R = 600 V	T_C = 25°C	–	–	100	µA
			T_C = 125°C	–	–	1	mA
V_{FM}	Instantaneous Forward Voltage (Note 7)	I_F = 15 A	T_C = 25°C	–	1.65	2.2	V
			T_C = 125°C	–	1.24	1.7	V
t_{rr}	Reverse Recovery Time	I_F = 15 A d_{IF}/dt = 200 A/µs V_R = 390 V (Note 6)	T_C = 25°C	–	29	–	ns
t_a	Time to reach peak reverse current		T_C = 25°C	–	16	–	ns
t_b	Time from peak I_{RRM} to projected zero crossing of I_{RRM} based on a straight line from peak I_{RRM} through 25% of I_{RRM}		T_C = 25°C	–	13	–	ns
Q_{rr}	Reverse Recovered Charge		T_C = 25°C	–	43	–	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
6. Defined by design, not subject to production test
7. Test pulse width = 300 µs, Duty Cycle = 2%

Table 6. THERMAL RESISTANCE

Parameters		Min	Typ	Max	Unit
$R_{\theta JC}$ (per MOSFET chip)	Q1, Q2 Thermal Resistance Junction−to−Case (Note 8)	–	0.19	0.27	°C/W
$R_{\theta JS}$ (per MOSFET chip)	Q1, Q2 Thermal Resistance Junction−to−Sink (Note 9)	–	0.62	–	°C/W
$R_{\theta JC}$ (per DIODE chip)	D1, D2 Thermal Resistance Junction−to−Case (Note 8)	–	0.74	1.1	°C/W
$R_{\theta JS}$ (per DIODE chip)	D1, D2 Thermal Resistance Junction−to−Sink (Note 9)	–	1.65	–	°C/W

8. $R_{\theta JC\ (junction\ to\ case)}$ Test method compliant with MIL STD 883−1012.1, from case temperature under the chip to case temperature measured below the package at the chip center, Cosmetic oxidation and discoloration on the DBC surface allowed
9. $R_{\theta JS\ (junction\ to\ heat\ sink)}$ Defined by thermal simulation assuming the module is mounted on a 5 mm Al−360 die casting material with 30 µm of 1.8 W/mK thermal interface material

Table 7. ISOLATION (Isolation resistance at tested voltage between the base plate and to control pins or power terminals.)

Test	Test Conditions	Isolation Resistance	Unit
Leakage @ Isolation Voltage (Hi−Pot)	V_{AC} = 5 kV, 50 Hz	100 M <	Ω

PARAMETER DEFINITIONS

Table 8. REFERENCE TO TABLE 3: PARAMETER OF MOSFET ELECTRICAL SPECIFICATIONS

BV_{DSS}	*Q1, Q2 MOSFET Drain−to−Source Breakdown Voltage* The maximum drain−to−source voltage the MOSFET can endure without the avalanche breakdown of the body−drain P−N junction in off state. The measurement conditions are to be found in table 3. The typ. Temperature behavior is described in Figure 14
$V_{GS(th)}$	*Q1, Q2 MOSFET Gate to Source Threshold Voltage* The gate−to−source voltage measurement is triggered by a threshold ID current given in conditions at table 4 The typ. Temperature behavior can be found in Figure 11
$R_{DS(ON)}$	*Q1, Q2 MOSFET On Resistance* RDS(on) is the total resistance between the source and the drain during the on state. The measurement conditions are to be found in table 3. The typ behavior can be found in Figure 12 and Figure 13 as well as Figure 18
g_{FS}	*Q1, Q2 MOSFET Forward Transconductance* Transconductance is the gain in the MOSFET, expressed in the Equation below. It describes the change in drain current by the change in the gate−source bias voltage: $$g_{fs} = \left[\frac{\Delta I_{DS}}{\Delta V_{GS}}\right]_{V_{DS}}$$
I_{GSS}	*Q1, Q2 MOSFET Gate−to−Source Leakage Current* The current flowing from Gate to Source at the maximum allowed VGS The measurement conditions are described in the table 3.
I_{DSS}	*Q1, Q2 MOSFET Drain−to−Source Leakage Current* Drain – Source current is measured in off state while providing the maximum allowed drain−to−source voltage and the gate is shorted to the source. IDSS has a positive temperature coefficient.

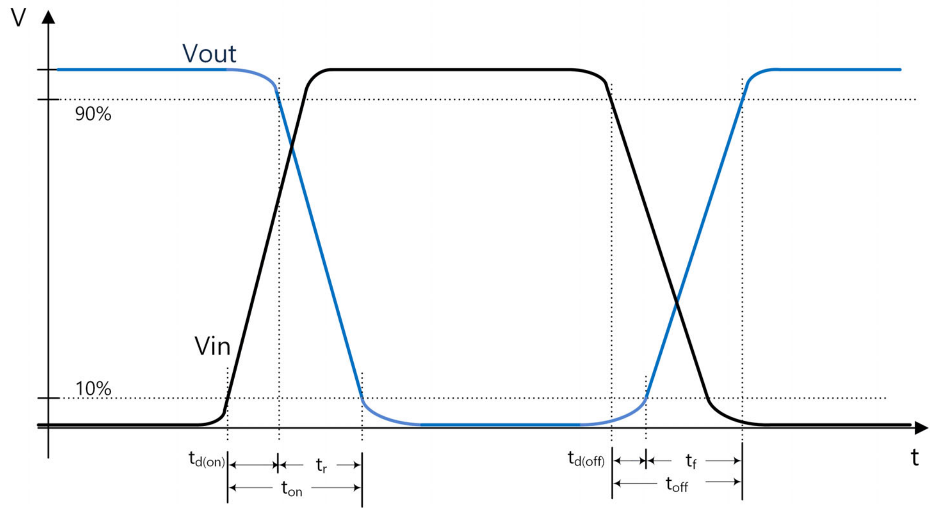


Figure 3. Timing Measurement Variable Definition

Table 9. PARAMETER OF SWITCHING CHARACTERISTICS

Turn−On Delay ($t_{d(on)}$)	This is the time needed to charge the input capacitance, Ciss, before the load current ID starts flowing. The measurement conditions are described in the table 3. For signal definition please check Figure 3 above.
Rise Time (t_r)	The rise time is the time to discharge output capacitance, Coss. After that time the MOSFET conducts the given load current ID. The measurement conditions are described in the table 3. For signal definition please check Figure 3 above.
Turn−On Time (t_{on})	Is the sum of turn−on−delay and rise time
Turn−Off Delay ($t_{d(off)}$)	td(off) is the time to discharge Ciss after the MOSFET is turned off. During this time the load current ID is still flowing The measurement conditions are described in the table 3. For signal definition please check Figure 3 above.
Fall Time (t_f)	The fall time, tf, is the time to charge the output capacitance, Coss. During this time the load current drops down and the voltage VDS rises accordingly. The measurement conditions are described in the table 3. For signal definition please check Figure 3 above.
Turn−Off Time (t_{off})	Is the sum of turn−off−delay and fall time

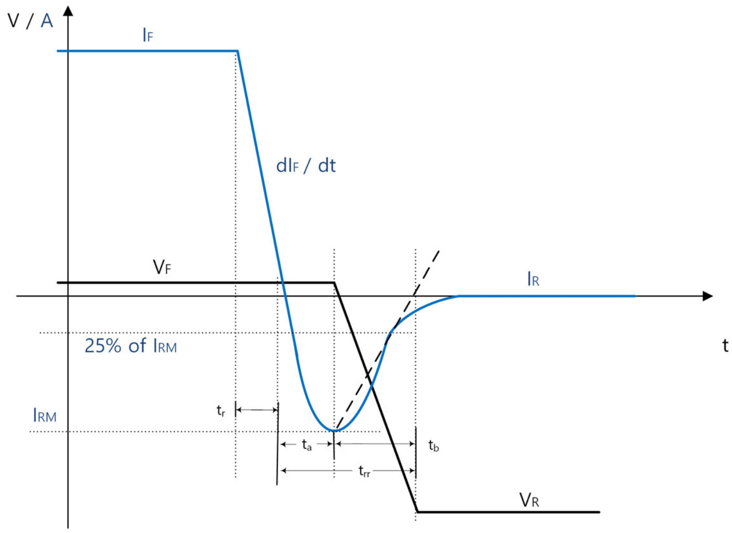


Figure 4. Dynamic Parameters of Silicon Diode (Not in Scale)

Table 10. REFERENCE TO TABLE 5: PARAMETER OF DIODE ELECTRICAL SPECIFICATIONS

Instantaneous Reverse Current (I_R)	Current flowing in reverse after the reverse recovery time t_{rr}. I_R is shown in Figure 4 above The behavior over voltage can be seen in Figure 23
Instantaneous Forward Voltage V_{FM}	Voltage drop over the diode in a dynamic condition given in Note 7. The voltage is measured after the given test pulse width. To avoid self heating effects a small duty cycle is used The behavior over voltage can be seen in Figure 22
Reverse Recovery Time t_{rr}	During this transition time,from conduction to blocking, the current is flowing in reverse direction and diode generates switching losses. The time is characterized on the scope by using the ta and tb approximation method ta + tb = trr parameter result in table 3 The parameter is dependent on temperature and initial dI/dt Figure 25 shows the dependency on dI/dt
Time to reach peak reverse current t_a	ta is the transition time from the moment the current starts to flow in reverse direction until the diode voltage drops (also the reverse current peak)
Time from peak IRRM to zero crossing t_b	tb is defined by using a linear approximation from the peak IRM to a projected zero crossing of IR by crossing IR at 25% of IRRM
Reverse Recovered Charge Q_{rr}	The reverse recovery charge is defined as $Q_{rr} = \int^{t_{rr}} I_r\,(t)\,dt$ This parameter is highly depend on temperature and dI/dt See Figure 27

TYPICAL CHARACTERISTICS – MOSFETS

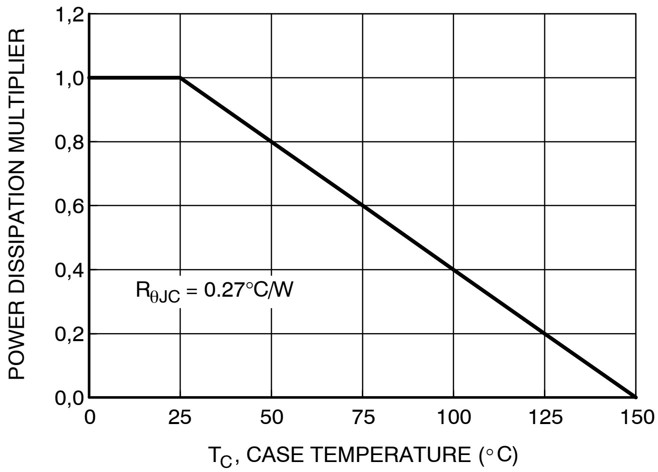


Figure 5. Normalized Power Dissipation vs. Case Temperature

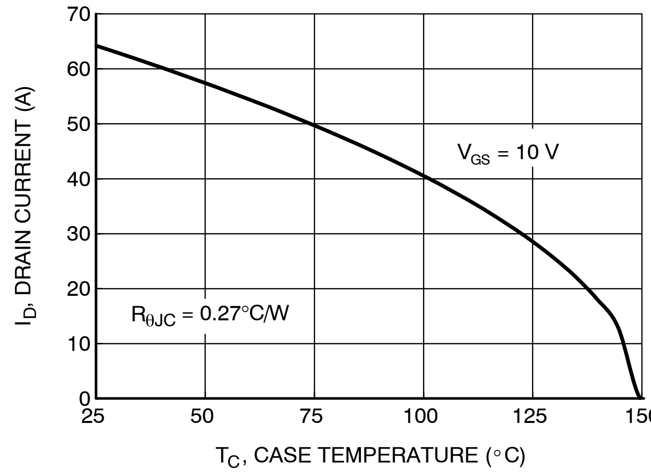


Figure 6. Maximum Continuous I_D vs. Case Temperature

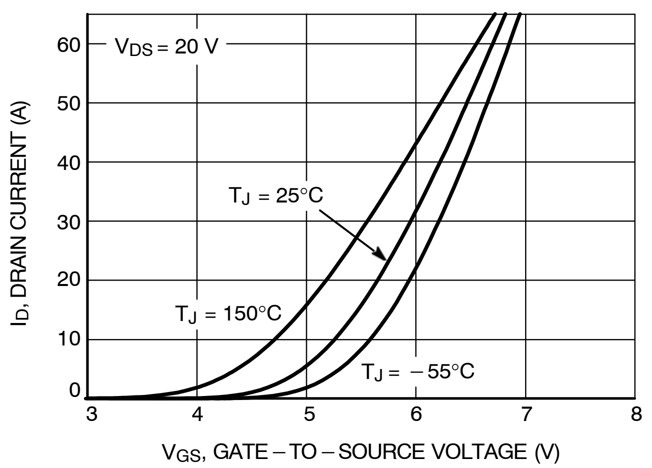


Figure 7. Transfer Characteristics

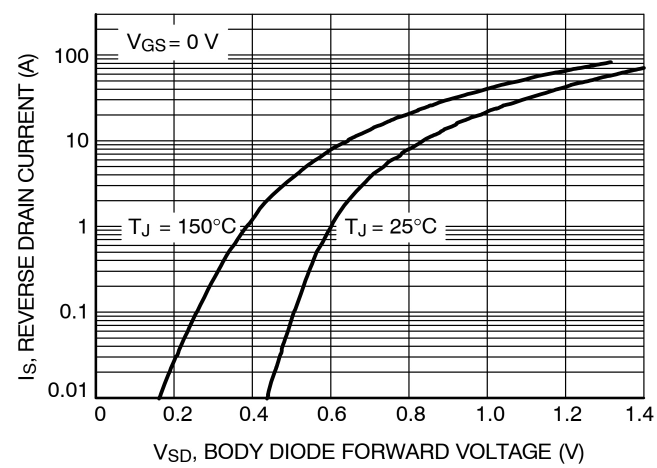


Figure 8. Forward Diode

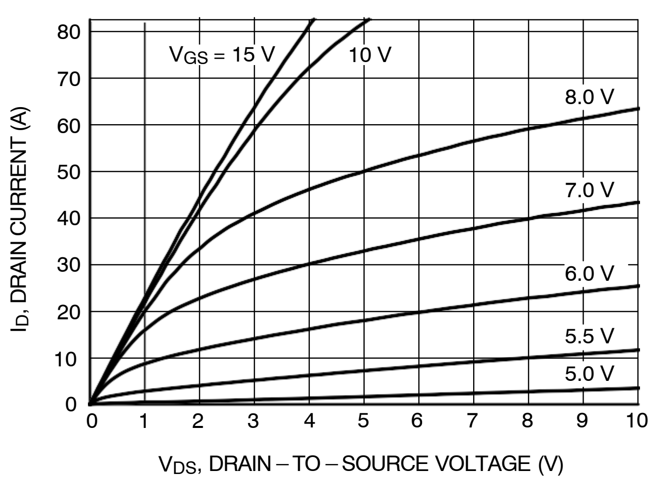


Figure 9. On Region Characteristics (25°C)

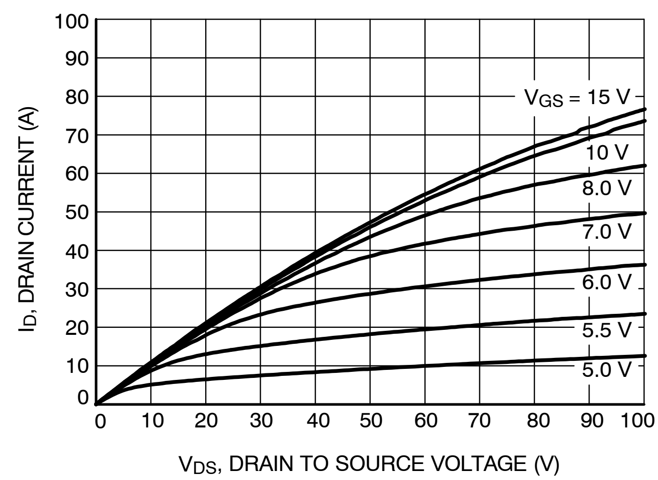


Figure 10. On Region Characteristics (150°C)

TYPICAL CHARACTERISTICS – MOSFETS (continued)

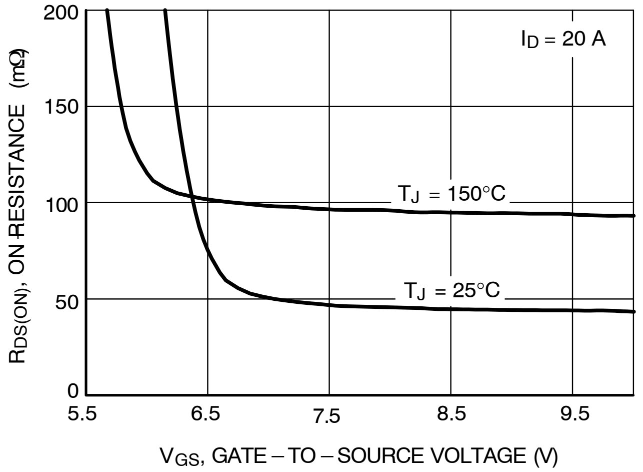


Figure 11. On−Resistance vs. Gate−to−Source Voltage

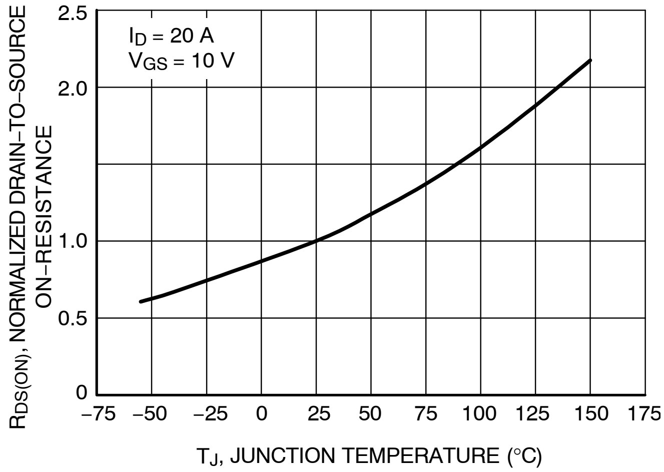


Figure 12. $R_{DS(norm)}$ vs. Junction Temperature

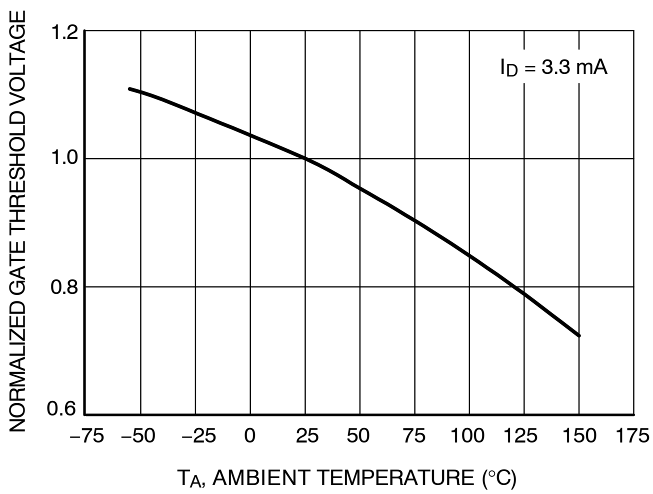


Figure 13. Normazlied Gate Threshold Voltage vs. Temperature

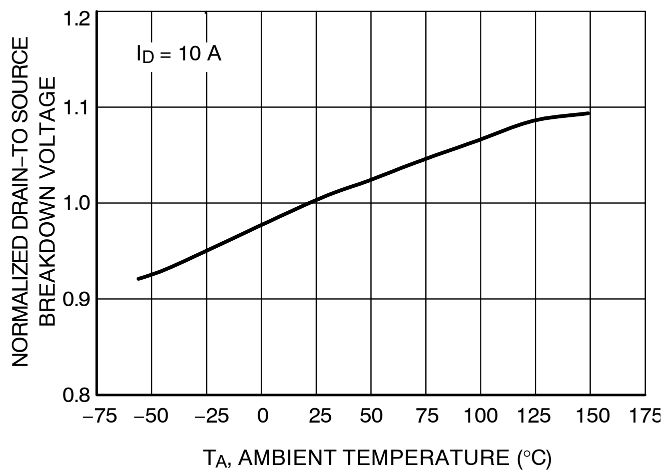


Figure 14. Normalized Breakdown Voltage vs. Temperature

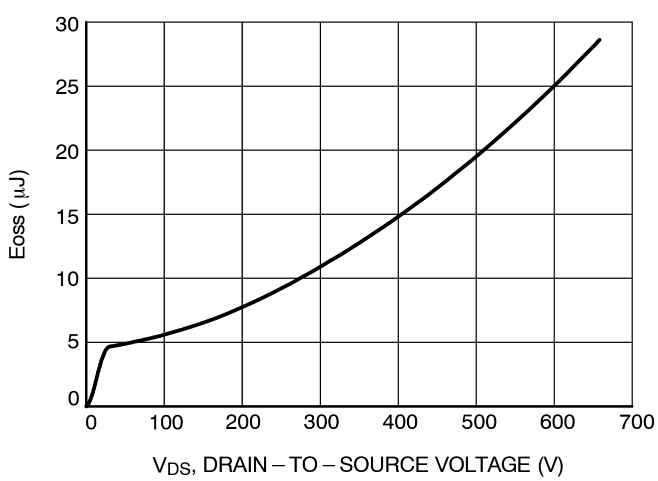


Figure 15. Eoss vs. Drain−to−Source Voltage

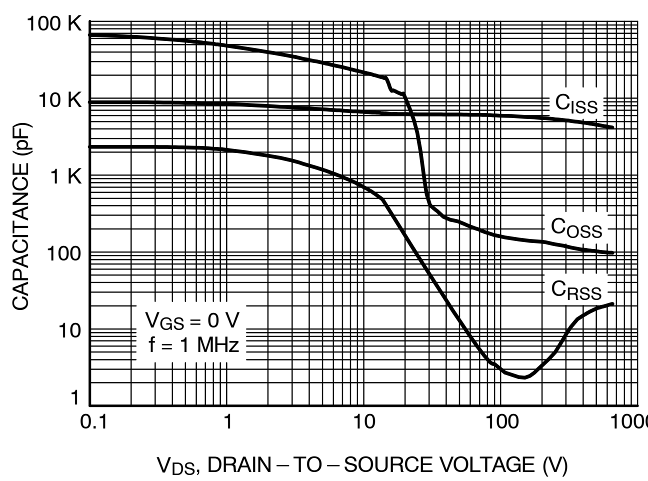


Figure 16. Capacitance Variation

TYPICAL CHARACTERISTICS – MOSFETS (continued)

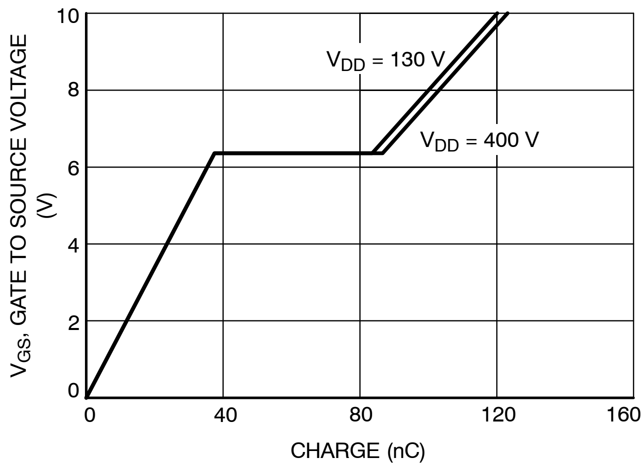


Figure 17. Gate Charge Characteristics

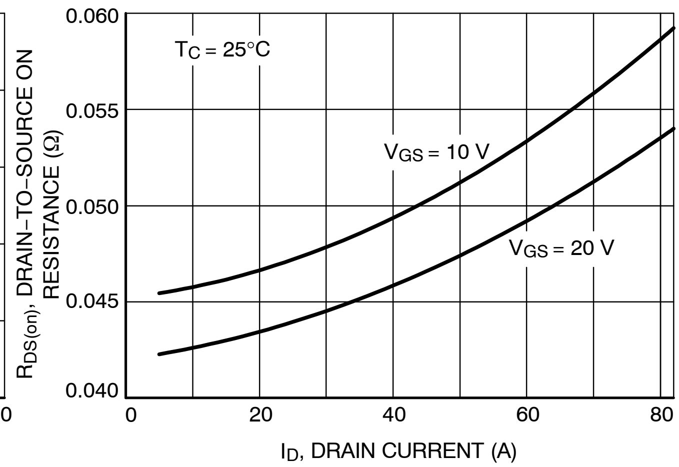


Figure 18. ON−Resistance Variation with Drain Current and Gate Voltage

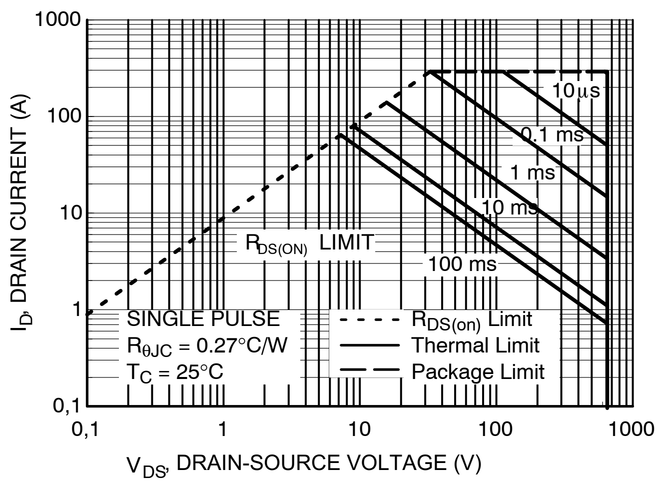


Figure 19. Safe Operating Area

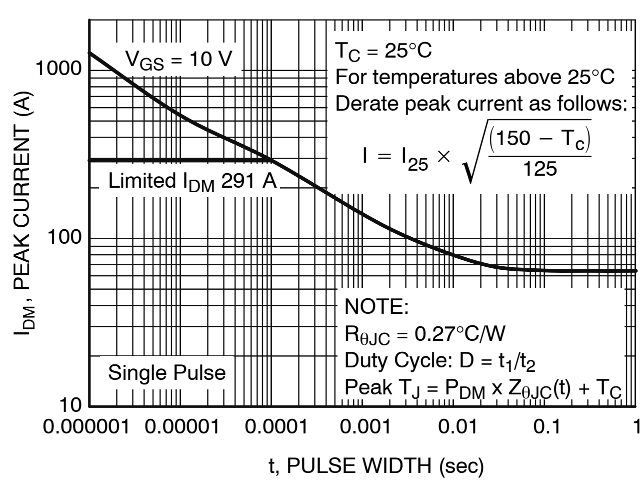


Figure 20. Peak Current Capability

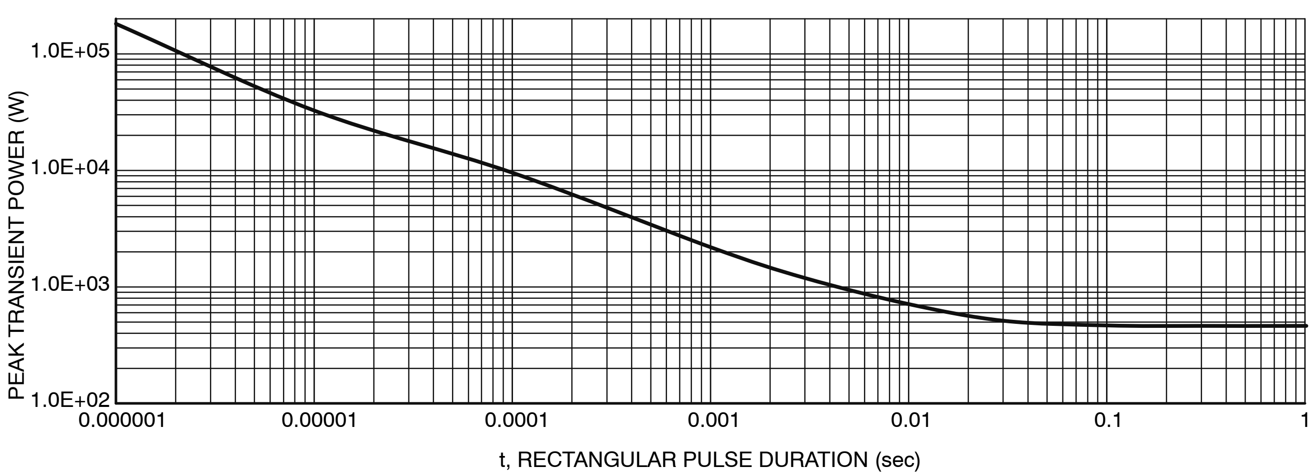


Figure 21. Peak Transient Power Capability

TYPICAL CHARACTERISTICS – DIODES

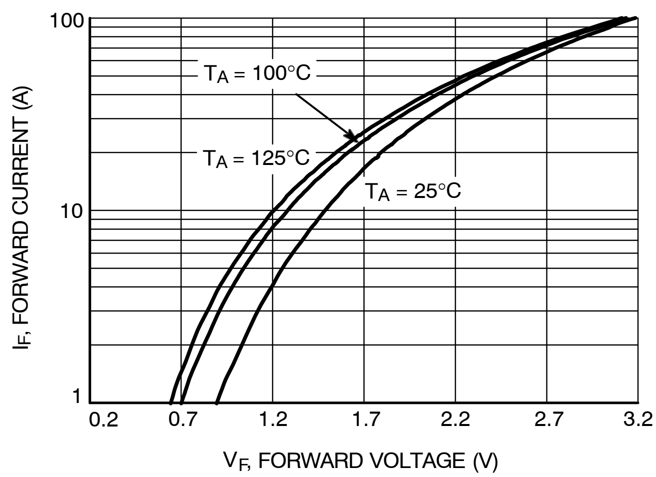


Figure 22. Typical Forward Voltage Drop vs. Forward Current

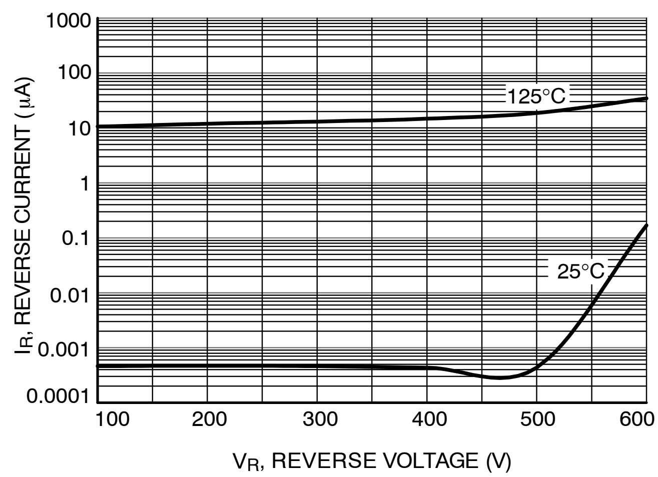


Figure 23. Typical Reverse Current vs. Reverse Voltage

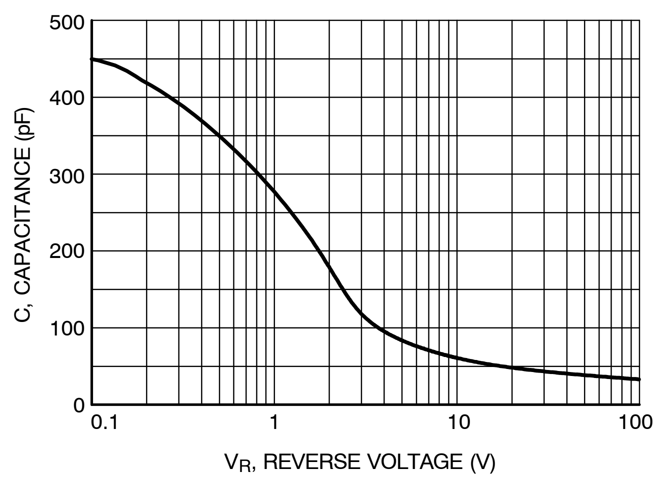


Figure 24. Capacitance

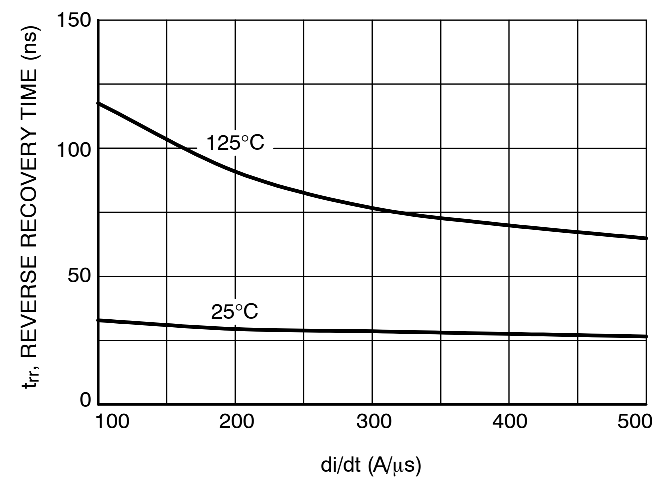


Figure 25. Reverse Recovery Time vs. di/dt

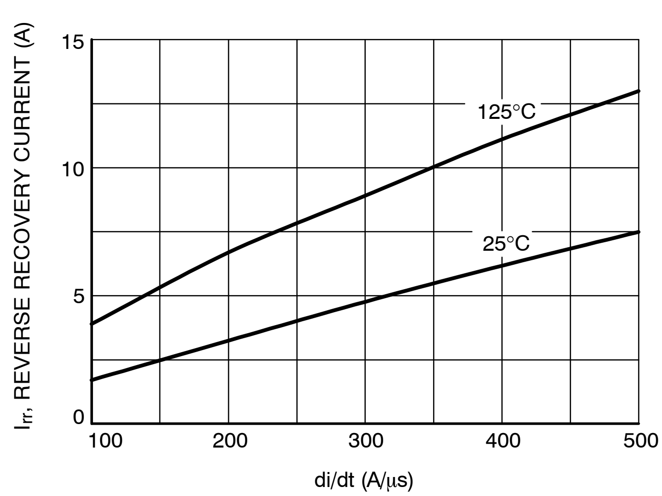


Figure 26. Reverse Recovery Current vs. di/dt

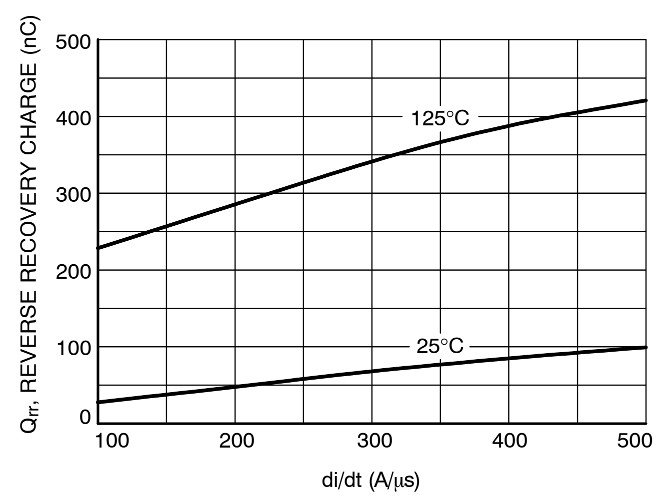


Figure 27. Reverse Recovery Charge vs. di/dt

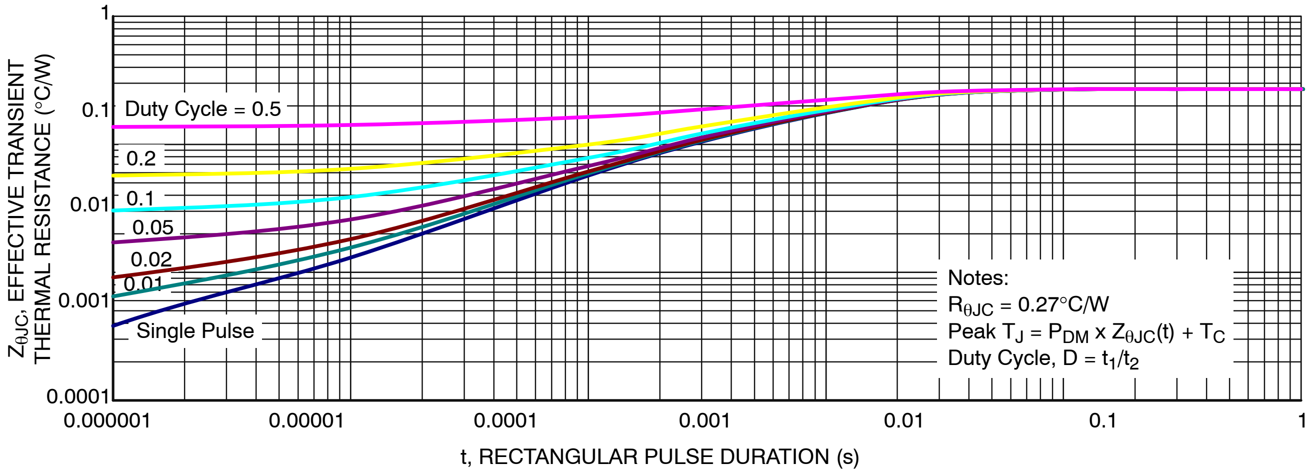
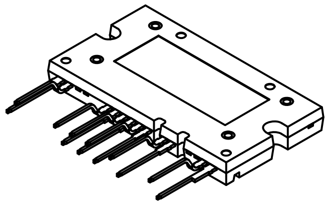
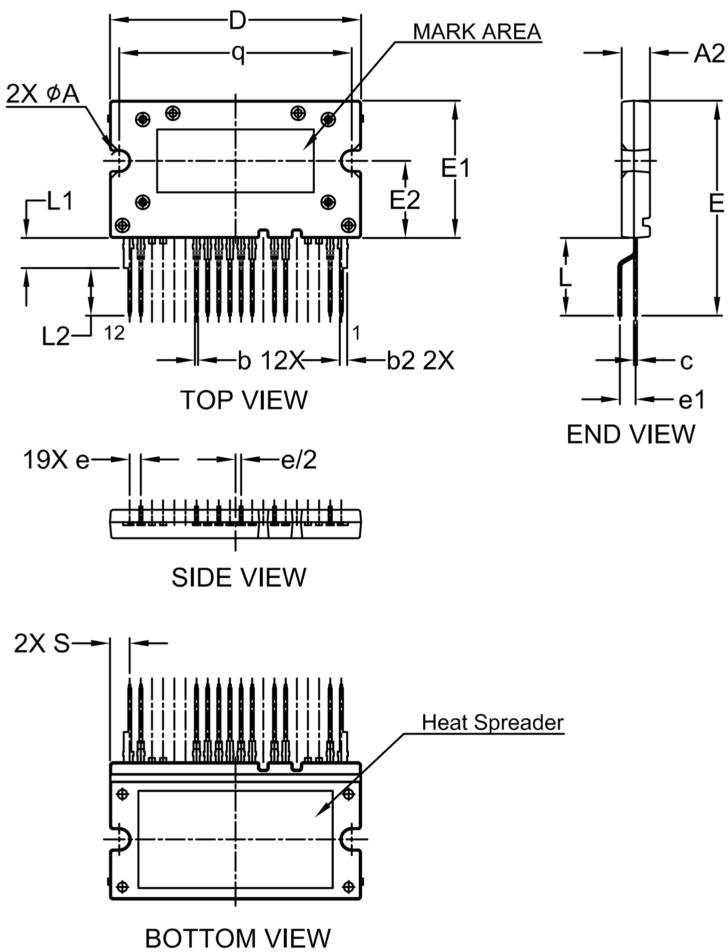


Figure 28. Transient Thermal Impedance



APMCD−A16 / 12LD, AUTOMOTIVE MODULE
CASE MODGG
ISSUE C

DATE 03 NOV 2021



NOTES:

1. DIMENSIONING AND TOLERANCING PER. ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR EXTRUSIONS.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A2	4.30	4.50	4.70
b	0.45	0.50	0.60
b2	1.15	1.20	1.30
c	0.45	0.50	0.60
D	39.90	40.10	40.30
E	33.80	34.30	34.80
E1	21.70	21.90	22.10
E2	12.10	12.30	12.50
e	1.478	1.778	2.078
e1	2.20	2.50	2.80
L	12.10	12.40	12.70
L1	4.80 REF		
L2	7.30	7.60	7.90
q	36.85	37.10	37.35
S	3.159 REF		
ϕA	3.00	3.20	3.40

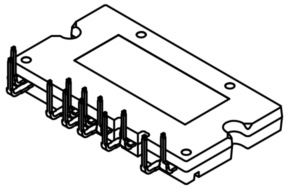
GENERIC MARKING DIAGRAM*

XXXXXXXXXXXXXXXX
ZZZ ATYWW
NNNNNNN

XXXX = Specific Device Code
ZZZ = Lot ID
AT = Assembly & Test Location
Y = Year
WW = Work Week
NNN = Serial Number

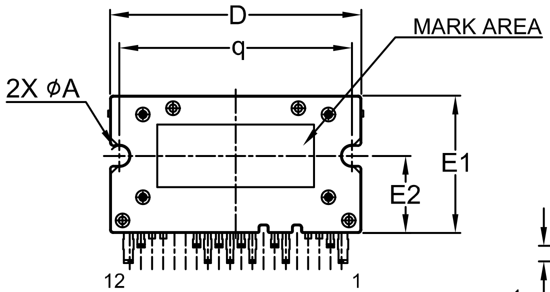
*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

DOCUMENT NUMBER:	98AON94738G	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	APMCD−A16 / 12LD, AUTOMOTIVE MODULE	PAGE 1 OF 1

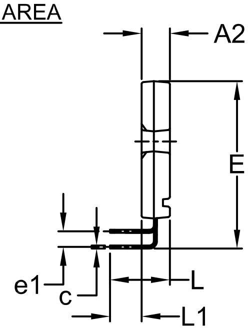


APMCD−B16 / 12LD, AUTOMOTIVE MODULE
CASE MODGK
ISSUE D

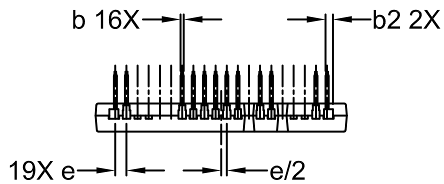
DATE 04 NOV 2021



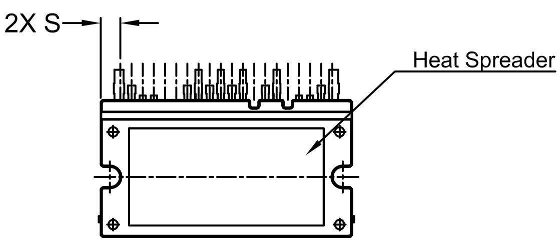
TOP VIEW



END VIEW



SIDE VIEW



BOTTOM VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER. ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR EXTRUSIONS.

	MILLIMETERS		
DIM	MIN.	NOM.	MAX.
A2	4.30	4.50	4.70
b	0.45	0.50	0.60
b2	1.15	1.20	1.30
c	0.45	0.50	0.60
D	39.90	40.10	40.30
E	26.20	26.70	27.20
E1	21.70	21.90	22.10
E2	12.10	12.30	12.50
e	1.478	1.778	2.078
e1	2.20	2.50	2.80
L	9.20	9.55	9.90
L1	4.70	5.05	5.40
q	36.85	37.10	37.35
S	3.159 REF		
ϕA	3.00	3.20	3.40

GENERIC MARKING DIAGRAM*

XXXXXXXXXXXXXXXX
ZZZ ATYWW
NNNNNNN

XXXX = Specific Device Code
ZZZ = Lot ID
AT = Assembly & Test Location
Y = Year
W = Work Week
NNN = Serial Number

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

DOCUMENT NUMBER:	**98AON97134G**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	**APMCD−B16 / 12LD, AUTOMOTIVE MODULE**	**PAGE 1 OF 1**

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
Technical Library: www.onsemi.com/design/resources/technical−documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support
For additional information, please contact your local Sales Representative at
www.onsemi.com/support/sales

◊