Fixed-Output Synchronous TinyBoost® Regulator

FAN48685

WLCSP9
CASE 567QW

Description

The FAN48685 is a low−power boost regulator designed to provide a minimum voltage−regulated rail from a standard single−cell Li−Ion battery and advanced battery chemistries. Even below the minimum system battery voltage, the device maintains the output voltage regulation for an output load current of 800 mA. The combination of built−in power transistors, synchronous rectification, and low supply current suit the FAN48685 for battery−powered applications.

The FAN48685 is available in a 9−bump, 0.4 mm pitch, Wafer−Level Chip−Scale Package (WLCSP).

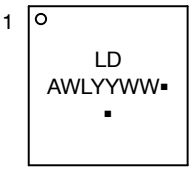
Features

- Input Voltage Range: 2.5 V to 5.5 V
- 800 mA Max. Load Capability
- Forced Pass−Through Mode
- Three Output Voltage Programmability (3.6 V / 5.0 V / 5.45 V) via MODE Pins
- 9−Bump, 0.4 mm Pitch WLCSP
- Four External Components: 0603 Inductor, 0402 Case Size Input, 0402 2 x Output Capacitors
- This is a Pb−Free Device

Applications

- NFC Module Power

MARKING DIAGRAM



LD	= Specific Device Code
A	= Assembly Location
WL	= Wafer Lot
YY	= Year
WW	= Work Week
▪	= Pb−Free Package

(Note: Microdot may be in either location)

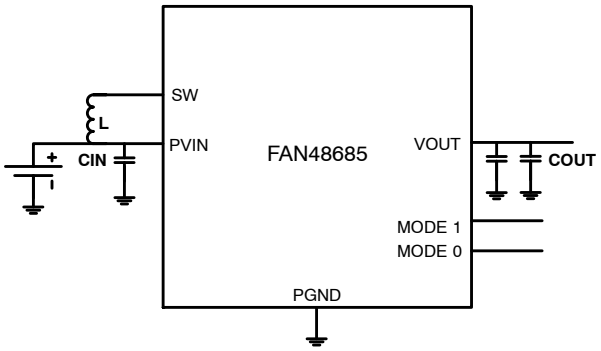


Figure 1. Typical Application

ORDERING INFORMATION

Part Number	Operating Temperature Range	Package	Packing Method	Device Marking
FAN48685UC08X	−40°C to 85°C	9−Bump, 0.4 mm Pitch, WLCSP Package	Tape & Reel	LD

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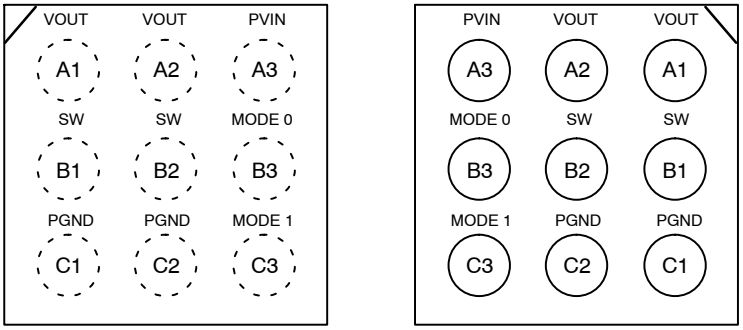
Recommended External Components

Table 1. RECOMMENDED COMPONENTS

Component	Description	Vendor	Parameter	Typical Value	Unit
L	470 nH 0603 (1.6 mm x 0.8 mm x 0.8 mm max)	DFE18SANR47ME Murata	L	0.47	μH
			DCR	64	mΩ
			ISAT	3.1	A
COUT	2 x 22 μF, 6.3 V, X5R, 0402 (1.0 mm x 0.5 mm)	GRM155R60J226ME11 Murata	C	44	μF
CIN	10 μF, 6.3 V, X5R, 0402 (1.0 mm x 0.5 mm)	C1005X5R0J106M050BC TDK	C	10	μF

Pin Configuration



Top View
(Bumps Down)

Bottom View
(Bumps Up)

Figure 2. Pin Assignment

Pin Descriptions

Table 2. PIN DESCRIPTIONS

Pin #	Name	Description
A1	VOUT	**Output Voltage**: This pin is the output voltage terminal. Connect directly to COUT.
A2		
A3	PVIN	**Input Voltage**: Connect to Li−Ion battery input power source and CIN.
B1	SW	**Switching Node**: Connect to inductor.
B2		
B3	MODE 0	**MODE 0**: In combination with MODE 1 selects the operation of the part.
C1	PGND	**Power Ground**: This is the power return for the IC. COUT and CIN capacitors should be returned with the shortest path possible to these pins.
C2		
C3	MODE 1	**MODE 1**: In combination with MODE 0 selects the operation of the part.

Table 3. ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Min	Max	Unit
PVIN	Voltage on PVIN Pin		−0.3	6.5	V
VOUT	Voltage on VOUT Pin		−0.3	6.5(1)	V
VSW	SW Node		−0.3	6.5(1)	V
VCTRL	MODE 0, MODE 1		−0.3	6.5(1)	V
ESD	Electrostatic Discharge Protection Level	Human Body Model, ANSI/ESDA/ JEDEC JS−001−2012	2.0		kV
		Charged Device Model, JESD22−C101	1.0		
T_J	Junction Temperature(2)		−40	150	°C
T_{STG}	Storage Temperature		−65	150	°C
T_L	Lead Soldering Temperature, 10 Seconds			260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Lesser of 6.5 V or PVIN + 0.3 V.
2. Please refer to Thermal Shutdown Protection in the Application information.

Table 4. RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Unit
PVIN	Supply Voltage Range	2.5		5.5	V
L	Inductor		0.470	0.611	μH
CIN	Input Capacitance		10		μF
COUT	Output Capacitance	5 (3)	2 x 22		μF
IOUT	Maximum Output Current	800			mA
T_A	Ambient Temperature	−40		85	°C
T_J	Junction Temperature	−40		125	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

3. The minimum effective capacitance at the output for stability is 5 uF which includes the voltage derated affect with 5.45 V DC applied.

Table 5. THERMAL PROPERTIES

Symbol	Parameter	Typical	Unit
θ_{JA}	Junction−to−Ambient Thermal Resistance	50	°C/W

NOTE: Junction−to−ambient thermal resistance is a function of application and board layout. This data is measured with four−layer 2s2p boards with vias in accordance to JEDEC standard JESD51. Special attention must be paid not to exceed junction temperature, $T_{J(max)}$, at a given ambient temperature, T_A.

Table 6. ELECTRICAL CHARACTERISTICS (Notes 4, 5)
Minimum and maximum values are at PVIN = 2.5 V to VOUT − 200 mV at T_A = −40°C to +85°C, while typical values are at T_A = 25°C and PVIN = 3.8 V, VOUT = 5 V otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Power Supplies						
I_{Q_PT}	IQ When part is in Forced Pass−Through	No Load		3	10	μA
V_{UVLO_RISE}	Under−Voltage Lockout	PVIN Rising	2.10	2.15	2.24	V
V_{UVLO_FALL}		PVIN Falling	2.00	2.05	2.13	V
Output Accuracy						
V_{O_ACC}	Regulated Output Voltage	PVIN = 2.5 V, MODE[1:0] = 10, No Load, PWM Mode, T_A = −10°C to +50°C	3.537	3.600	3.663	V
		PVIN = 2.5 V, MODE[1:0] = 10, No Load, PWM Mode	3.510	3.600	3.690	
		PVIN = 3.8 V, MODE[1:0] = 01, No Load, PWM Mode, T_A = −10°C to +50°C	4.913	5.000	5.088	
		PVIN = 3.8 V, MODE[1:0] = 01, No Load, PWM Mode	4.875	5.000	5.125	
		PVIN = 3.8 V, MODE[1:0] = 11, No Load, PWM Mode, T_A = −10°C to +50°C	5.355	5.450	5.545	
		PVIN = 3.8 V, MODE[1:0] = 11, No Load, PWM Mode	5.314	5.450	5.586	
Regulator						
F_{SW}	Switching Frequency	No Load, PVIN = 3.8 V	2.25	2.50	2.75	MHz
I_{SWLIM}	IL peak Current Limit	PVIN = 2.5 V, Open Loop (Note 6)	2.88	3.63	4.46	A
LIN	Soft−Start Input Linear Current Limit			90	200	mA
I/O Levels						
V_{IL}	Low−Level Input Voltage				0.4	V
V_{IH}	High−Level Input Voltage		1.2		PVIN	V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Min and Max limits are specified by design, test and/or statistical analysis.
5. Refer to Typical Characteristics waveforms/graphs for closed loop data and variation with input supply and temperature. Electrical specifications reflect open loop steady state data.
6. Current Limit specifications is tested open loop, for typical close loop current limit data, refer to typical performance characteristics

Table 7. SYSTEM SPECIFICATIONS (Note 7)

The following system specifications are guaranteed by designed and are not performed in production testing. Recommended operating conditions, unless otherwise noted, PVIN = 2.5 V to VOUT − 200 mV, TA = 40°C to 85°C, VOUT = 5.45 V otherwise noted. Typical values are given PVIN = 3.8 V and TA = 25°C. System Specifications area based on circuit per Figure 1. L = 0.47 μH (0603 DFE1608CK−R47M 70 mΩ/ 3.0 A) CIN = 10 uF (0402 C1005X5R0J106M050BC TDK) COUT = 2 x 22 uF (0402 GRM155R60J226ME11 MURATA.)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Efficiency						
η	Efficiency	VOUT = 5.45 V, IOUT = 100 mA		86		%
		VOUT = 5.45 V, IOUT = 300 mA		92		
		VOUT = 5.45 V, IOUT = 500 mA		93		
IOUT MAX						
I_{OUT}	IOUT Max.		800			mA
VOUT Regulation						
$LOAD_{REG}$	Load Regulation	200 mA < IOUT < 600 mA, VOUT = 5.45 V		−5		mV/A
$LINE_{REG}$	Line Regulation	3.0 V < PVIN < 4.2 V , IOUT = 550 mA, VOUT = 5.45 V		2		mV/V
Output Ripple						
V_{RIPPLE}	Output Ripple	IOUT = 550 mA, VOUT = 5.45 V, PVIN = 3.8 V		15	30	mV
		IOUT = 450 mA, VOUT = 3.6 V, PVIN = 3.0 V		15	30	
VOUT Transitions						
T_{SETTLE}	VOUT Change	MODE[1:0] 00 > 01 to 95% of VOUT, VOUT = Forced Pass−Through Mode > 5 V, IOUT = 1 mA		150	200	μs
		MODE[1:0] 00 > 10 to 95% of VOUT, VOUT = Forced Pass−Through Mode > 3.6 V, IOUT = 1 mA, PVIN = 2.5 V to VOUT − 200 mV		100	200	
I_{SS}	Soft−Start	MODE[1:0] = 00, VOUT = PVIN (Start up into Forced Pass−Through Mode)		1.5		ms
Noise						
en_bw	Output Noise Voltage (Integrated)	VOUT = 5 V, IOUT = 550 mA, Freq = 0 Hz to 200 kHz		26	750	μV
		VOUT = 5 V, IOUT = 550 mA, Freq = 50 kHz to 2 MHz		140	500	
		VOUT = 5 V and 3.6 V, IOUT = 550 mA, Freq = 13.5 MHz ± 200 kHz		70	300	
Transients						
V_{TRRP}	Load Transient	IOUT = 10 mA ↔ 400 mA, $T_R = T_F$ = 1 μs, VOUT = 5.45 V		±75		mV
V_{TRRP}	Load Transient	PVIN = 3.0 V ↔ 3.5 V, $T_R = T_F$ = 10 μs, IOUT = 550 mA, VOUT = 5.45 V		±75		mV

7. System Specifications are tested closed loop while using the recommended external components as listed on Table 1.

Typical Performance Characteristics

Unless otherwise specified; PVIN = 3.8 V, VOUT = 5.45 V, T_A = 25°C, and circuit and components according to Figure 1. Components: CIN = 10 μF (0402 C1005X5R0J106M050BC TDK) COUT = 2 x 22 μF (0402 GRM155R60J226ME11 MURATA), L = 0.47 μH (0603, 70 mΩ, DFE1608CK−R47M).

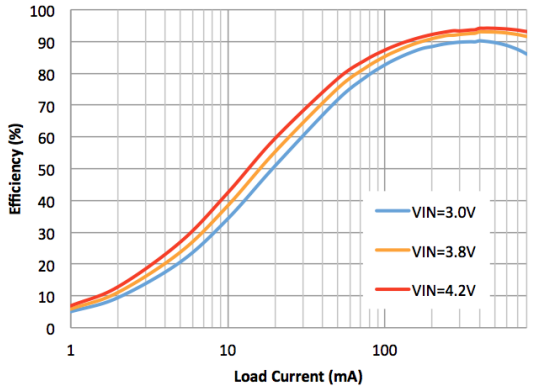


Figure 3. Efficiency vs. Load Current and Input Voltage

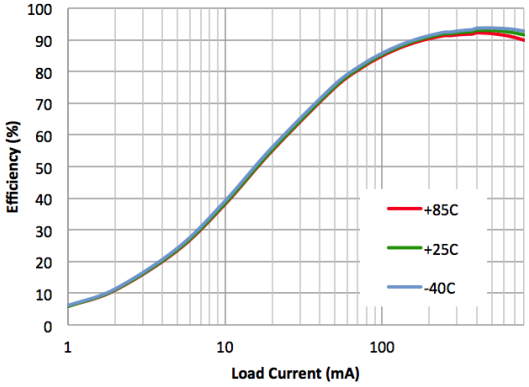


Figure 4. Efficiency vs. Load Current and Temperature

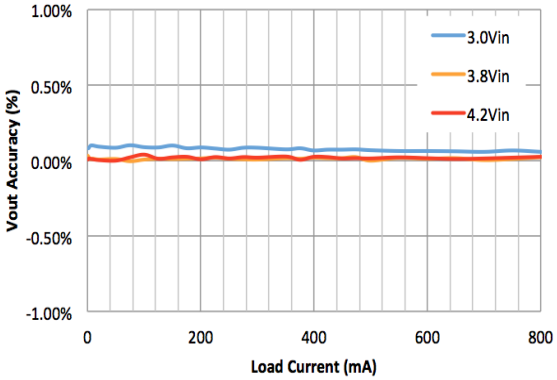


Figure 5. Output Regulation vs. Load Current and Input Voltage

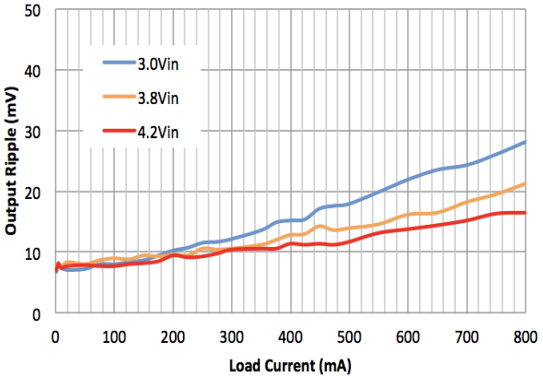


Figure 6. Output Ripple vs. Load Current and Input Voltage

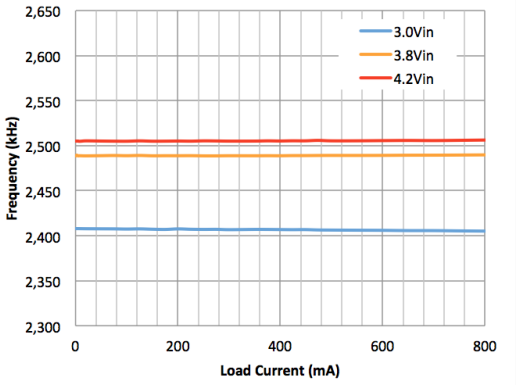


Figure 7. Frequency vs. Load Current and Input Voltage

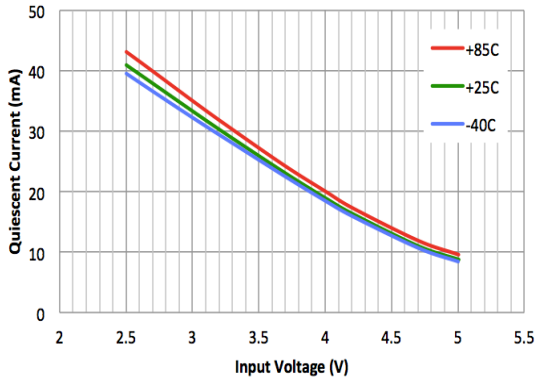


Figure 8. Quiescent Current vs. Input Voltage and Temperature

Typical Performance Characteristics

Unless otherwise specified; PVIN = 3.8 V, VOUT = 5.45 V, T_A = 25°C, and circuit and components according to Figure 1. Components: CIN = 10 μF (0402 C1005X5R0J106M050BC TDK) COUT = 2 x 22 μF (0402 GRM155R60J226ME11 MURATA), L = 0.47 μH (0603, 70 mΩ, DFE1608CK−R47M).

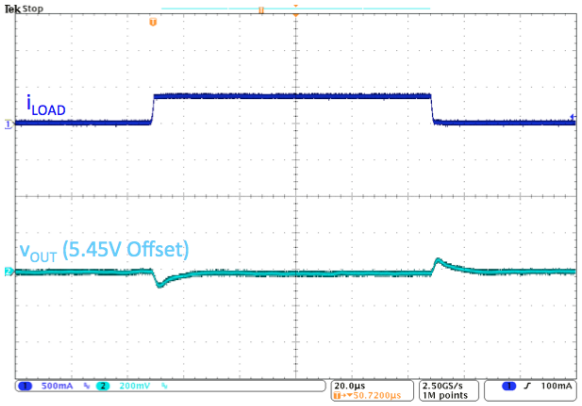


Figure 9. Load Transient, 10 ↔ 400 mA, 1 μs Edge

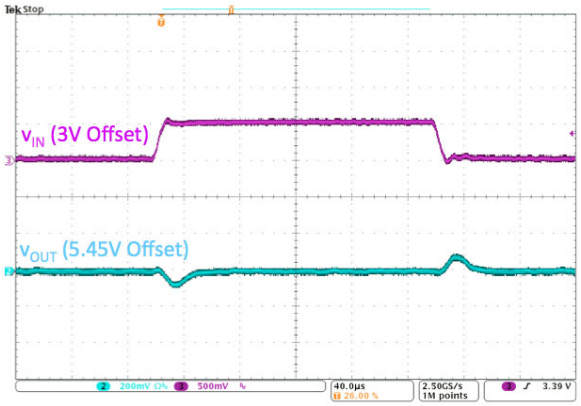


Figure 10. Line Transient, 3.0 V ↔ 3.5 V, 10 μs Edge, 550 mA Load

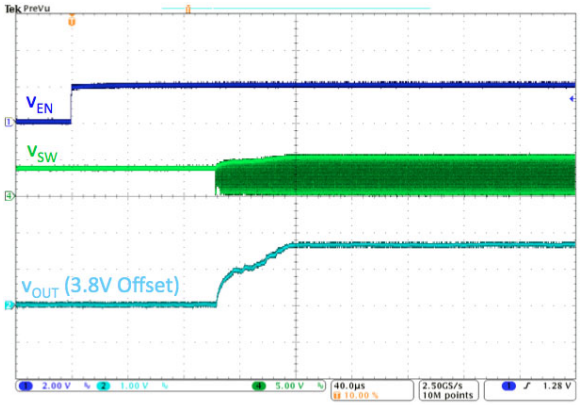


Figure 11. VOUT Change: Forced PT to BOOST

APPLICATION INFORMATION

Operation Description

The FAN48685 is low−power boost regulator designed to provide a minimum voltage regulated rail from a standard single−cell Li−Ion battery. The device offers superior features for NFC applications. PWM switching frequency is maintain away from the sub carrier of NFC application avoiding interference. The FAN48685 automatically goes to 100% duty cycle when the input voltage nears the output voltage. The part can also be placed in forced pass through mode by pulling both mode pins low.

Startup Behavior

Startup Description

The device is designed to startup with no load allowing the implementation of input current controls that support lower capacity batteries without inducing brown out. Care should be taken in the system design to ensure load is applied after regulation has been reached and output capacitance is a suitable value to avoid fault time−outs occurring. The device can startup in either boost mode or forced pass−through mode. When starting in boost mode, the part has a linear mode which limits the battery current to 90 mA (typ.) to avoid large inrush currents from the battery. In linear mode, if VOUT fails to reach PVIN target within 1.5 ms, a fault condition is declared and the device waits 20 ms to attempt an automatic restart. Once VOUT charges up to PVIN, the linear mode current limit is disabled and the output voltage is ramped to the final value via the DAC that programs the output.

When starting up in forced pass−through mode, the output voltage is charged using the same linear mode mechanism until VOUT reaches PVIN.

Modes of Operation

PWM Description

During PWM mode, the output voltage is regulated by switching at a constant frequency and then modulating the energy per cycle to control the power to the load.

Forced Pass−Through Mode

When both mode pins are pulled low, the part will be forced in pass−through mode. The output voltage is around: VOUT = (PVIN − (IOUT* (DCR of L +HIGH SIDE FET RDSON)) during this mode.

Automatic Pass−Through Mode

In normal operation, the device automatically transitions from boost mode to pass−through mode if PVIN is within about 150 mV of VOUT boost voltage. In pass−through mode, the device has a low impedance path between PVIN and VOUT. Entry into pass−through mode occurs when PVIN is sufficiently close to VOUT that minimum on−time persists for 16 cycles. In Automatic pass−through mode, there is short−circuit protection which protects both the IC and external components.

Mode Transition

Pass−Through to Boost Mode

When going from pass−through mode to boost mode, initially there is a delay for the internal digital circuitry to power up the analog circuitry. After, analog circuitry is powered, the internal DAC will begin to start stepping from 2.45 V. As soon as the internal DAC step is greater than PVIN, the VOUT of the device begins to increase until it reaches its final VOUT target value. The device is designed to transitions under no load, care should be taken in system design to ensure the load is not applied during VOUT transitions.

When going from boost mode to pass−through mode, the output voltage decay will be determined by the amount of load at the VOUT.

Boost to Boost Mode

When going from boost mode to a higher VOUT boost mode, the internal DAC starts its step from the current VOUT until the final VOUT target. Since there is no latency for the analog to be powered up, immediately after the DAC stepping, the VOUT of the device begins to increase until it reaches its final VOUT target value.

When going from boost mode to a lower VOUT boost mode, the output voltage decay will be determined by the amount of load at the VOUT.

Protection Features

VOUT Fault

During startup, if the VOUT fails to reach PVIN target within 1.5 ms, the part declares a fault. Once the fault is triggered, the regulator stops switching and presents a high−impedance path between PVIN and VOUT.

Current Limit Protection (OCP)

FAN48685 has a current limit feature, which protects itself and load during overloading conditions. When the inductor peak current is reached and held for 2 ms, the device goes into a fault. The part restarts every 20 ms once fault occurs.

Thermal Shutdown Protection (TSP)

When the die temperature increases, due to a high load condition and/or a high ambient temperature; the output switching is disabled until the die temperature falls sufficiently. The junction temperature at which the thermal shutdown activates is nominally 150°C with a 15°C hysteresis.

Automatic Pass−Through Mode Protection

During automatic pass−through mode, the device is short−circuit protected, if the voltage difference between PVIN and VOUT exceed more than 300 mV for 10 us, then a fault is declared. The part will restart every 20 ms.

Under−Voltage Lockout (UVLO)

Once PVIN reaches UVLO rising the part will begin to switch and begin the startup process. When PVIN falls to UVLO falling, the part stops switching and output voltage starts decays to 0 V.

Control Pin Functionality

Table 8. MODE PINS FUNCTIONALITY (Note 8)

Mode 1	Mode 0	Status of Device
0	0	Forced Pass−Through Mode; VOUT = PVIN
0	1	Active; VOUT = 5.00 V
1	0	Active; VOUT = 3.60 V
1	1	Active; VOUT = 5.45 V

8. Recommended to have logic levels transitions and fall times typically at 100 ns. MODE Pins have smart pulls down of 300 kΩ (typ.) and are only activated when at logic LOW.

ADDITIONAL APPLICATIONS INFORMATION

Application Guidelines

Input Capacitor Considerations

The 10 μF ceramic 0402 (1005 metric) input capacitor should be placed as close as possible between the PVIN pin and GND to minimize the parasitic inductance. If a long wire is used to bring power to the IC, additional “bulk” capacitance (electrolytic or tantalum) should be placed (on Evaluation board) between CIN and the power source lead to reduce the ringing that can occur between the inductance of the power source leads and CIN. The effective capacitance value decreases as PVIN increases due to DC bias effects.

Output Capacitor Considerations

The two 22 μF ceramic 0402 (1005 metric) output capacitor should be placed as close as possible between the VOUT pin and GND to minimize the parasitic inductance. The effective capacitance value decreases as VOUT increases due to DC bias effects. Therefore, a minimum 5 uF capacitance is required to maintain stable regulation at the output.

If the output capacitance is increased beyond the recommended two 22 μF ceramic the system design should be evaluated to ensure that the part does not enter fault state or hiccup during start−up as the device charges the output capacitance.

Inductor Considerations

The FAN48685 employs a peak current limiting, so peak inductor current can reach 3.63 A for a short duration during overload conditions. Saturation effects causes the inductor current ripple to become higher under high loading, as only the peak of the inductor current ripple is controlled.

Layout Considerations

The layout recommendations below highlight various top−copper pours using different colors. To minimize spikes at VOUT, COUT must be placed as close as possible to PGND and VOUT, as shown in Figure 12.

For thermal reasons, it is suggested to maximize the pour area for all planes other than SW. Especially the ground pour should be set to fill all available PCB surface area and tied to internal layers with a cluster of thermal vias.

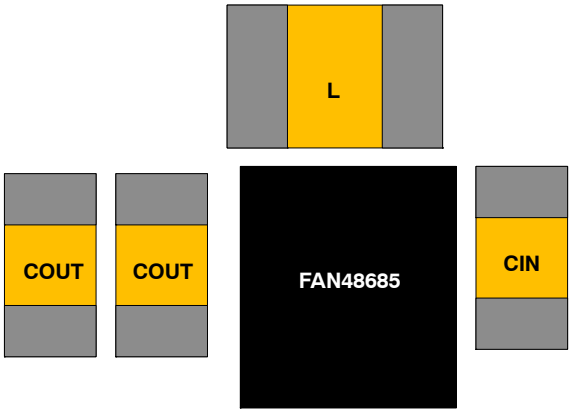
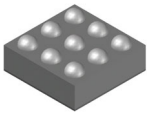
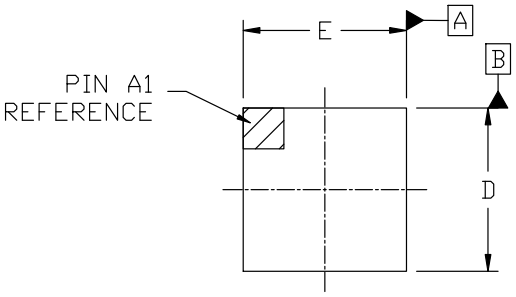


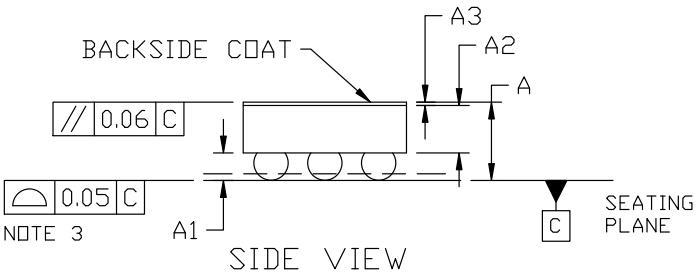
Figure 12. Recommended Layout

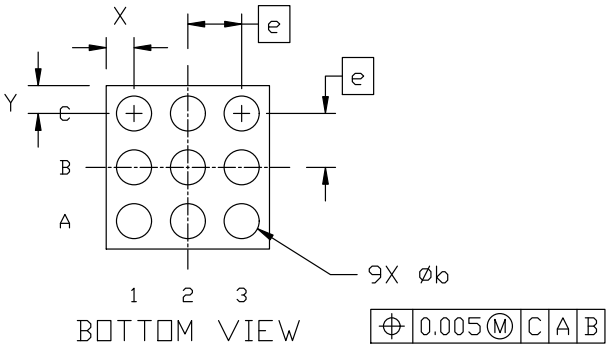


WLCSP9 1.215x1.215x0.581
CASE 567QW
ISSUE B

DATE 24 FEB 2023



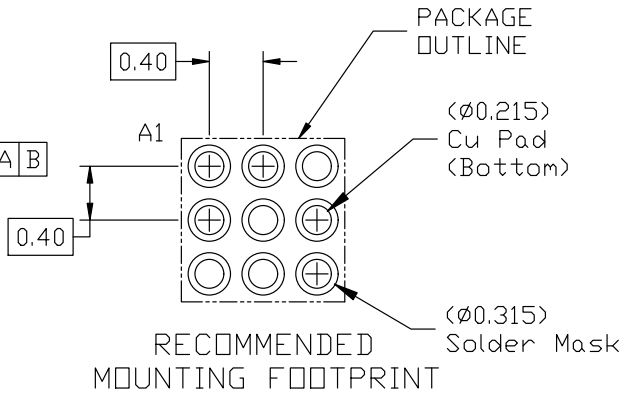




NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. COPLANARITY APPLIES TO THE SPHERICAL CROWNS OF THE SOLDER BALLS.
4. DATUM C, THE SEATING PLANE, IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER PARALLEL TO DATUM C.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.542	0.581	0.620
A1	0.183	0.203	0.223
A2	0.335	0.353	0.371
A3	0.022	0.025	0.027
b	0.24	0.26	0.28
D	1.185	1.215	1.245
E	1.185	1.215	1.245
e	0.400 BSC		
X	0.208 REF		
Y	0.208 REF		



* For additional information on our Pb-Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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