

# Multi-Mode Buck Converter with LDO Assist for GSM / EDGE, 3G/3.5G and 4G PAs

## FAN5910

### Description

The FAN5910 is a high-efficiency, low-noise, synchronous, step-down, DC-DC converter optimized for powering Radio Frequency (RF) Power Amplifiers (PAs) in handsets and other mobile applications. Load currents up to 2.5 A are allowed, which enables GSM / EDGE, 3G/3.5G, and 4G platforms under very poor VSWR conditions.

The output voltage may be dynamically adjusted from 0.40 V to 3.60 V, proportional to an analog input voltage  $V_{CON}$  ranging from 0.16 V to 1.44 V, optimizing power-added efficiency. Fast transition times are achieved, allowing excellent inter-slot settling.

An integrated LDO is automatically enabled under heavy load conditions or when the battery voltage and voltage drop across the DC-DC PMOS device are within a set range of the desired output voltage. This LDO-assist feature supports heavy load currents under the most stringent battery and  $V_{SWR}$  conditions while maintaining high efficiency, low dropout, and superior spectral performance.

The FAN5910 DC-DC operates in PWM Mode with a 2.9 MHz switching frequency and supports a single, small form-factor inductor ranging from 1.0  $\mu$ H to 2.2  $\mu$ H. In addition, PFM operation is allowed at low load currents for output voltages below 1.5 V to maximize efficiency. PFM operation can be disabled by setting MODE pin to LOW.

When output regulation is not required, the FAN5910 may be placed in Sleep Mode by setting  $V_{CON}$  below 100 mV nominally. This ensures a very low  $I_Q$  (<50  $\mu$ A) while enabling a fast return to output regulation.

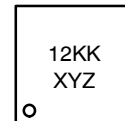
FAN5910 is available in a low profile, small form factor, 16 bump, Wafer-Level Chip-Scale Package (WLCSP) that is 1.615 mm x 1.615 mm. Only three external components are required: two 0402 capacitors and one 2016 inductor.

### Features

- Solution Size < 9.52 mm<sup>2</sup>
- 2.7 V to 5.5 V Input Voltage Range
- $V_{OUT}$  Range from 0.40 V to 3.60 V (or  $V_{IN}$ )
- Single, Small Form-Factor Inductor
- 29 m $\Omega$  Integrated LDO
- 100% Duty Cycle for Low-Dropout Operation
- Input Under-Voltage Lockout / Thermal Shutdown
- 1.615 mm x 1.615 mm, 16-Bump, 0.4 mm Pitch WLCSP
- 2.9 MHz PWM Mode
- Sleep Mode for ~50  $\mu$ A Standby Current Consumption



WLCSP  
16 BUMP  
CASE 567SD



- 12 = Alphanumeric Device Code  
(See Ordering Information for specific marking)
- KK = Lot Run Number
- X = Alphabetical Year Code
- Y = 2-weeks Date Code
- Z = Assembly Plant Code

### ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

- Forced PWM Mode
  - ◆ Up to 95% Efficient Synchronous Operation in High Power Conditions
  - ◆ 2.9 MHz PWM-Only Mode
- Auto PFM/PWM Mode
  - ◆ 2.9 MHz PWM Operation at High Power and PFM Operation at Low Power and Low Output Voltage for Maximum Low Current Efficiency

### Applications

- Dynamic Supply Bias for Polar or Linear GSM / EDGE PAs and 3G/3.5G and 4G PAs
- Dynamic Supply Bias for GSM / EDGE Quad Band Amplifiers for Mobile Handsets and Data Cards

# FAN5910

## ORDERING INFORMATION

| Part Number | Output Voltage | Temperature Range | Package   | Packing†      | Device Marking |
|-------------|----------------|-------------------|---|---------------|----------------|
| FAN5910UCX  | 0.4 V to PVIN  | -40°C to +85°C    | 1.615 mm x 1.615 mm, 16-Bump 0.4 mm Pitch, Wafer-Level Chip-Scale Package (WLCSP) | Tape and Reel | LJ             |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

## BLOCK DIAGRAMS

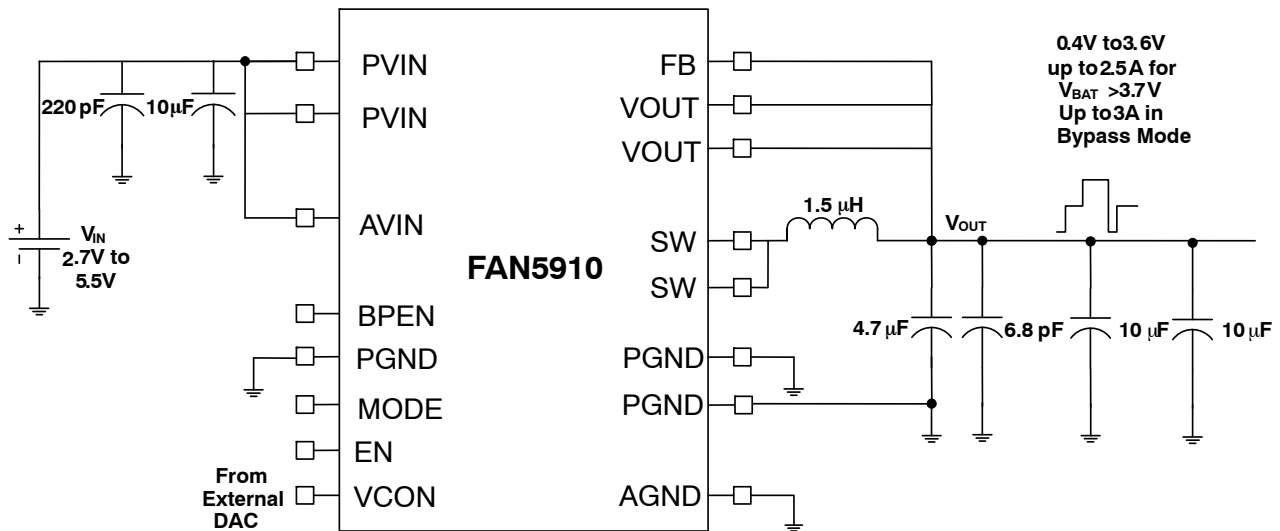


Figure 1. Typical Application

1. The three 4.7  $\mu\text{F}$  capacitors include the FAN5910 output capacitor and PA bypass capacitors.
2. Regulator requires only one 4.7  $\mu\text{F}$ ; the  $V_{\text{OUT}}$  bus should not exceed 14  $\mu\text{F}$  capacitance over DC bias and temperature.

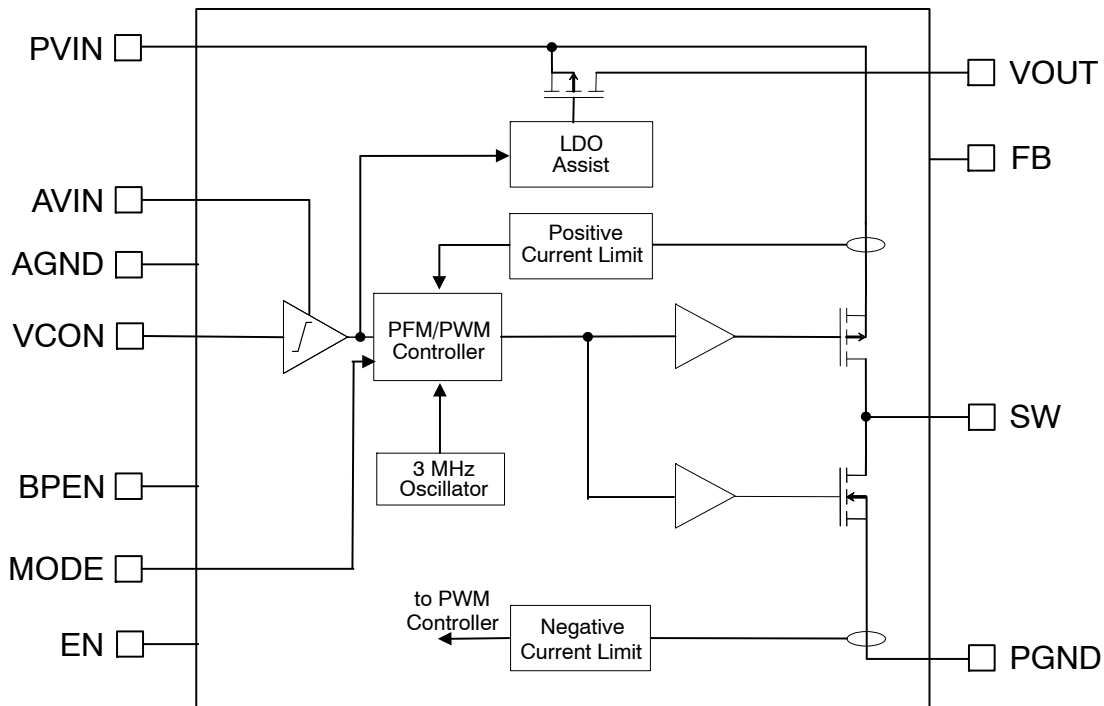


Figure 2. Simplified Block Diagram

# FAN5910

## PIN CONFIGURATION

|            |            |            |            |
|------------|------------|------------|------------|
| PGND<br>A1 | SW<br>A2   | PVIN<br>A3 | VOUT<br>A4 |
| B1         | B2         | B3         | B4         |
| AGND<br>C1 | EN<br>C2   | BPEN<br>C3 | PGND<br>C4 |
| AVIN<br>D1 | VCON<br>D2 | MODE<br>D3 | FB<br>D4   |

Figure 3. Bumps Face Down – Top-Through View

|            |            |            |            |
|------------|------------|------------|------------|
| VOUT<br>A4 | PVIN<br>A3 | SW<br>A2   | PGND<br>A1 |
| B4         | B3         | B2         | B1         |
| PGND<br>C4 | BPEN<br>C3 | EN<br>C2   | AGND<br>C1 |
| FB<br>D4   | MODE<br>D3 | VCON<br>D2 | AVIN<br>D1 |

Figure 4. Bumps Face Up

## PIN DEFINITIONS

| Pin #      | Name | Description   |
|------------|------|---|
| C1         | AGND | Analog ground, reference ground for the IC. Follow PCB routing notes for connecting this pin.   |
| A4, B4     | VOUT | Output voltage sense pin. Connect to $V_{OUT}$ to establish feedback path for regulation point. Connect together on PCB.  |
| D4         | FB   | Feedback pin. Connect to positive (+) pad of $C_{OUT}$ on $V_{OUT}$ .   |
| C2         | EN   | Enables switching when HIGH; Shutdown Mode when LOW. This pin should not be left floating.  |
| D2         | VCON | Analog control pin. Shield signal routing against noise.  |
| D1         | AVIN | Analog supply voltage input. Connect to PVIN.   |
| C3         | BPEN | Force Bypass Mode when HIGH; Auto Bypass Mode when LOW. This pin should not be left floating.   |
| D3         | MODE | When MODE is HIGH, the DC-DC permits PFM operation under low load currents and PWM operation under heavy load currents. When MODE pin is set LOW, the DC-DC operates in forced PWM operation. This pin should not be left floating. |
| A3, B3     | PVIN | Supply voltage input to the internal MOSFET switches. Connect to input power source.  |
| A2, B2     | SW   | Switching node of the internal MOSFET switches. Connect to output inductor.   |
| A1, B1, C4 | PGND | Power ground of the internal MOSFET switches. Follow routing notes for connections between PGND and AGND.   |

**Table 1. ABSOLUTE MAXIMUM RATINGS**

| Symbol           | Parameter                                |                                   | Min      | Max                    | Unit |
|------------------|--|-----------------------------------|----------|------------------------|------|
| V <sub>IN</sub>  | Voltage on AVIN, PVIN                    |                                   | −0.3     | 6.0                    | V    |
|                  | Voltage on Any Other Pin                 |                                   | −0.3     | AV <sub>IN</sub> + 0.3 |      |
| T <sub>J</sub>   | Junction Temperature                     |                                   | −40      | +125                   | °C   |
| T <sub>STG</sub> | Storage Temperature                      |                                   | −65      | +150                   | °C   |
| T <sub>L</sub>   | Lead Soldering Temperature (10 Seconds)  |                                   |          | +260                   | °C   |
| ESD              | Electrostatic Discharge Protection Level | Human Body Model, JESD22−A114     | 2.0      |                        | kV   |
|                  |  | Charged Device Model, JESD22−C101 | 1.0      |                        |      |
| LU               | Latch Up                                 |                                   | JESD 78D |                        |      |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

**Table 2. RECOMMENDED OPERATING CONDITIONS**

| Symbol            | Parameter                            | Min  | Typ | Max       | Unit |
|-------------------|--------------------------------------|------|-----|-----------|------|
| $V_{IN}$          | Supply Voltage Range                 | 2.7  |     | 5.5       | V    |
| $V_{OUT}$         | Output Voltage Range                 | 0.35 |     | $<V_{IN}$ | V    |
| $I_{OUT\_BYPASS}$ | Output Current in Bypass Mode        |      |     | 4.5       | A    |
| $I_{OUT}$         | Output Current                       |      |     | 2.5       | A    |
| L                 | Inductor                             |      | 1.5 |           | μH   |
| $C_{IN}$          | Input Capacitor (Note 3)             |      | 10  |           | μF   |
| $C_{OUT}$         | Output Capacitor (Note 4)            |      | 4.7 |           | μF   |
| $T_A$             | Operating Ambient Temperature Range  | -40  |     | +85       | °C   |
| $T_J$             | Operating Junction Temperature Range | -40  |     | +125      | °C   |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

3. The input capacitor must be large enough to limit the input voltage drop during GSM bursts, bypass transitions, and large output voltage transitions.

4. Regulator requires only one 4.7 μF.

**Table 3. DISSIPATION RATINGS**

| Symbol        | Parameter                                       | Min | Typ | Max | Unit |
|---------------|---|-----|-----|-----|------|
| $\theta_{JA}$ | Junction-to-Ambient Thermal Resistance (Note 5) |     | 40  |     | °C/W |

5. Junction-to-ambient thermal resistance is a function of application and board layout. This data is measured with four-layer 2s2p boards with vias in accordance to JESD51- JEDEC standard. Special attention must be paid not to exceed junction temperature  $T_{J(MAX)}$  at a given ambient temperature  $T_A$ .

# FAN5910

**Table 4. ELECTRICAL CHARACTERISTICS, ALL MODES** Recommended operating conditions, unless otherwise noted, circuit per Figure 1, minimum and maximum values are at  $V_{IN} = 2.7\text{ V}$  to  $5.5\text{ V}$ ,  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ ,  $V_{OUT} = V_{CON} \times 2.5 = 0.4\text{ V}$  to  $3.6\text{ V}$ ,  $V_{IN} \geq V_{OUT} + 0.3\text{ V}$ . Typical values are given  $V_{IN} = 3.8\text{ V}$  and  $V_{OUT} = 2.5\text{ A}$  at  $T_A = 25^\circ\text{C}$ .  $L = 1.5\text{ }\mu\text{H}$ , Murata DFE201610C,  $C_{IN} = 10\text{ }\mu\text{F}$  0402 Samsung CL05A106MP5NUNC,  $C_{OUT} = 1 \times 4.7\text{ }\mu\text{F}$  0402 Murata GRM155R60J475ME47D,  $2 \times 10\text{ }\mu\text{F}$  0402 Murata GRM188B30J106ME47D.

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|--------|-----------|-----------|-----|-----|-----|------|
|--------|-----------|-----------|-----|-----|-----|------|

## POWER SUPPLIES

|            |                                 |                                |      |      |      |               |
|------------|---------------------------------|--------------------------------|------|------|------|---------------|
| $V_{IN}$   | Input Voltage Range             | $I_{OUT} \leq 2.5\text{ A}$    | 2.7  |      | 5.5  | V             |
| $I_{SD}$   | Shutdown Supply Current         | $EN = 0\text{ V}$ , $MODE = 0$ |      | 0.5  | 3.0  | $\mu\text{A}$ |
| $V_{UVLO}$ | Under Voltage Lockout Threshold | $V_{IN}$ Rising                | 2.20 | 2.45 | 2.60 | V             |
|            |                                 | Hysteresis                     |      | 250  |      | mV            |

## LOGIC CONTROL

|            |   |                      |     |      |      |               |
|------------|---|----------------------|-----|------|------|---------------|
| $V_{IH}$   | Logic Threshold Voltage;<br>EN, BPEN, MODE          | Input HIGH Threshold | 1.2 |      |      | V             |
| $V_{IL}$   |   | Input LOW Threshold  |     |      | 0.4  | V             |
| $I_{CTRL}$ | Logic Control Input Bias Current;<br>EN, BPEN, MODE | $V_{IN}$ or GND      |     | 0.01 | 1.00 | $\mu\text{A}$ |

## ANALOG CONTROL

|                     |   |   |     |              |     |               |
|---------------------|---|---|-----|--------------|-----|---------------|
| $V_{CON\_BYP\_EN1}$ | $V_{CON}$ Forced Bypass Entry Threshold | $V_{CON}$ Voltage that Forces Bypass;<br>$V_{IN} \geq 4\text{ V}$ | 1.6 |              |     | V             |
| $V_{CON\_BYP\_EN2}$ | $V_{CON}$ Forced Bypass Entry Threshold | $V_{CON}$ Voltage that Forces Bypass;<br>$V_{IN} < 4\text{ V}$    |     | $V_{IN}/2.5$ |     | V             |
| $V_{CON\_BYP\_EX}$  | $V_{CON}$ Forced Bypass Exit Threshold  | $V_{CON}$ Voltage that Exits Forced Bypass                        |     |              | 1.4 | V             |
| $V_{CON\_SL\_EN}$   | $V_{CON}$ Sleep Enter                   | $V_{CON}$ Voltage Forcing Low $I_Q$ Sleep Mode                    | 70  |              |     | mV            |
| $V_{CON\_SL\_EX}$   | $V_{CON}$ Sleep Exit                    | $V_{CON}$ Voltage that Exits SLEEP Mode                           |     |              | 125 | mV            |
| $I_Q$               | DC-DC Quiescent Current in Sleep Mode   | $V_{CON} < 70\text{ mV}$  |     | 50           | 80  | $\mu\text{A}$ |
| Gain                | $V_{CON}$ to $V_{OUT}$ Gain             | $V_{CON} = 0.16\text{ V}$ to $1.44\text{ V}$                      |     | 2.5          |     | V/V           |
| $V_{OUT\_ACC}$      | $V_{OUT}$ Accuracy                      | Ideal = $2.5 \times V_{CON}$                                      | -50 |              | +50 | mV            |

## LDO

|                       |                      |                          |  |     |  |            |
|-----------------------|----------------------|--------------------------|--|-----|--|------------|
| $R_{FET}$             | LDO FET Resistance   |                          |  | 29  |  | m $\Omega$ |
| $\Delta V_{OUT\_LDO}$ | LDO Dropout (Note 6) | $I_{OUT} = 2.0\text{ A}$ |  | 100 |  | mV         |

## OVER TEMPERATURE PROTECTION

|           |                             |                    |  |      |  |                  |
|-----------|-----------------------------|--------------------|--|------|--|------------------|
| $T_{OTP}$ | Over-Temperature Protection | Rising Temperature |  | +150 |  | $^\circ\text{C}$ |
|           |                             | Hysteresis         |  | +20  |  | $^\circ\text{C}$ |

## OSCILLATOR

|          |                              |  |     |     |     |     |
|----------|------------------------------|--|-----|-----|-----|-----|
| $f_{SW}$ | Average Oscillator Frequency |  | 2.6 | 2.9 | 3.2 | MHz |
|----------|------------------------------|--|-----|-----|-----|-----|

## DC-DC

|                 |                                     |                           |      |      |      |            |
|-----------------|-------------------------------------|---------------------------|------|------|------|------------|
| $R_{DS(on)}$    | PMOS On Resistance                  |                           |      | 80   |      | m $\Omega$ |
|                 | NMOS On Resistance                  |                           |      | 60   |      |            |
| $I_{LIMp}$      | P-Channel Current Limit (Note 7)    |                           | 1.50 | 1.90 | 2.30 | A          |
| $I_{LIMn}$      | N-Channel Current Limit (Note 7)    |                           | 1.50 | 1.90 | 2.30 | A          |
| $I_{Discharge}$ | Maximum Transient Discharge Current |                           |      | 3.7  | 4.5  | A          |
| $V_{OUT\_MIN}$  | Minimum Output Voltage              | $V_{CON} = 0.16\text{ V}$ | 0.35 | 0.40 | 0.45 | V          |

6. Dropout depends on LDO and DC-DC PFET  $R_{DS(on)}$  and inductor DCR.

7. The current limit is the peak (maximum) current.

8. Guaranteed by design. Maximum values are based on simulation results with 50%  $C_{OUT}$  derating; not tested in production. Voltage transient only. Assumes  $C_{OUT} = 24.7\text{ }\mu\text{F}$  ( $1 \times 4.7\text{ }\mu\text{F}$  for regulator and  $2 \times 10\text{ }\mu\text{F}$  for PA decoupling capacitors).

9. Protects part under short-circuit conditions

# FAN5910

**Table 4. ELECTRICAL CHARACTERISTICS, ALL MODES** Recommended operating conditions, unless otherwise noted, circuit per Figure 1, minimum and maximum values are at  $V_{IN} = 2.7\text{ V}$  to  $5.5\text{ V}$ ,  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ ,  $V_{OUT} = V_{CON} \times 2.5 = 0.4\text{ V}$  to  $3.6\text{ V}$ ,  $V_{IN} \geq V_{OUT} + 0.3\text{ V}$ . Typical values are given  $V_{IN} = 3.8\text{ V}$  and  $V_{OUT} = 2.5\text{ A}$  at  $T_A = 25^\circ\text{C}$ .  $L = 1.5\text{ }\mu\text{H}$ , Murata DFE201610C,  $C_{IN} = 10\text{ }\mu\text{F}$  0402 Samsung CL05A106MP5NUNC,  $C_{OUT} = 1 \times 4.7\text{ }\mu\text{F}$  0402 Murata GRM155R60J475ME47D,  $2 \times 10\text{ }\mu\text{F}$  0402 Murata GRM188B30J106ME47D.

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|--------|-----------|-----------|-----|-----|-----|------|
|--------|-----------|-----------|-----|-----|-----|------|

## DC-DC

|                |                        |   |      |      |      |   |
|----------------|------------------------|---|------|------|------|---|
| $V_{OUT\_MAX}$ | Maximum Output Voltage | $V_{CON} = 1.44\text{ V}$ , $V_{IN} = 3.9\text{ V}$ | 3.55 | 3.60 | 3.65 | V |
|----------------|------------------------|---|------|------|------|---|

## DC-DC EFFICIENCY

|                |                                       |   |  |    |  |   |
|----------------|---------------------------------------|---|--|----|--|---|
| $\eta_{Power}$ | Power Efficiency, Low-Power Auto Mode | $V_{OUT} = 3.1\text{ V}$ , $I_{LOAD} = 250\text{ mA}$ |  | 95 |  | % |
|                |                                       | $V_{OUT} = 1.8\text{ V}$ , $I_{LOAD} = 250\text{ mA}$ |  | 90 |  |   |
|                |                                       | $V_{OUT} = 0.5\text{ V}$ , $I_{LOAD} = 10\text{ mA}$  |  | 65 |  |   |

## OUTPUT REGULATION

|                   |                           |  |  |          |  |    |
|-------------------|---------------------------|--|--|----------|--|----|
| $V_{OUT\_RLine}$  | $V_{OUT}$ Line Regulation | $3.1 \leq V_{IN} \leq 3.8$ , $100\text{ mA}$   |  | $\pm 5$  |  | mV |
| $V_{OUT\_RLoad}$  | $V_{OUT}$ Load Regulation | $20\text{ mA} \leq I_{OUT} \leq 800\text{ mA}$ |  | $\pm 25$ |  | mV |
| $V_{OUT\_Ripple}$ | $V_{OUT}$ Ripple          | PFM Mode, $I_{OUT} < 100\text{ mA}$            |  | 11       |  | mV |
|                   |                           | PWM Mode                                       |  | 4        |  |    |

## TIMING

|                 |   |  |  |      |  |               |
|-----------------|---|--|--|------|--|---------------|
| $t_{SS}$        | Startup Time  | $V_{IN} = 3.8\text{ V}$ , $V_{OUT}$ from $0\text{ V}$ to $2.5\text{ V}$ , $C_{OUT} = 1 \times 4.7\text{ }\mu\text{F}$ , $10\text{ V}$ , X5R; $2 \times 10\text{ }\mu\text{F}$ , $6.3\text{ V}$ , X5R |  | 12   |  | $\mu\text{s}$ |
| $t_{DC-DC\_TR}$ | $V_{CON}$ Step Response Rise Time                           | From $V_{CON}$ to $95\% V_{OUT}$ , $\Delta V_{OUT} \leq 2.7\text{ V}$ ( $0.7\text{ V} - 3.4\text{ V}$ ), $R_{LOAD} = 5\text{ }\Omega$ , $C_{OUT} = 24.7\text{ }\mu\text{F}$                          |  | 18   |  | $\mu\text{s}$ |
| $t_{DC-DC\_TF}$ | $V_{CON}$ Step Response Fall Time                           | From $V_{CON}$ to $5\% V_{OUT}$ , $\Delta V_{OUT} \leq 2.7\text{ V}$ ( $3.4\text{ V} - 0.7\text{ V}$ ), $R_{LOAD} = 200\text{ }\Omega$ , $C_{OUT} = 24.7\text{ }\mu\text{F}$                         |  | 12   |  | $\mu\text{s}$ |
| $t_{DC-DC\_CL}$ | Maximum Allowed Time for Consecutive Current Limit (Note 9) | $V_{OUT} < 1\text{ V}$   |  | 1500 |  | $\mu\text{s}$ |
| $t_{DCDC\_CLR}$ | Consecutive Current Limit Recovery Time (Note 9)            |  |  | 4800 |  | $\mu\text{s}$ |

6. Dropout depends on LDO and DC-DC PFET  $R_{DS(on)}$  and inductor DCR.

7. The current limit is the peak (maximum) current.

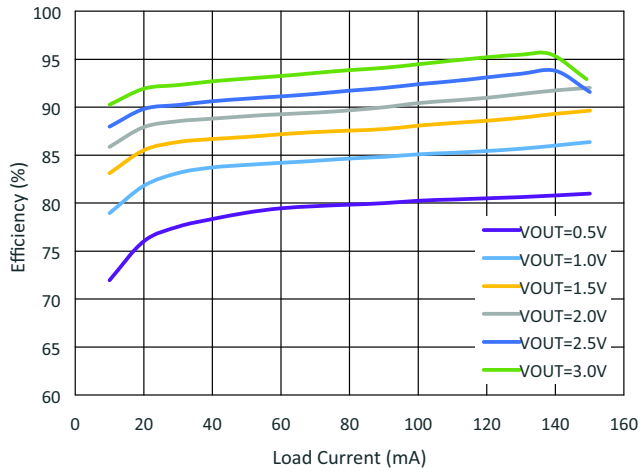
8. Guaranteed by design. Maximum values are based on simulation results with 50%  $C_{OUT}$  derating; not tested in production. Voltage transient only. Assumes  $C_{OUT} = 24.7\text{ }\mu\text{F}$  ( $1 \times 4.7\text{ }\mu\text{F}$  for regulator and  $2 \times 10\text{ }\mu\text{F}$  for PA decoupling capacitors).

9. Protects part under short-circuit conditions

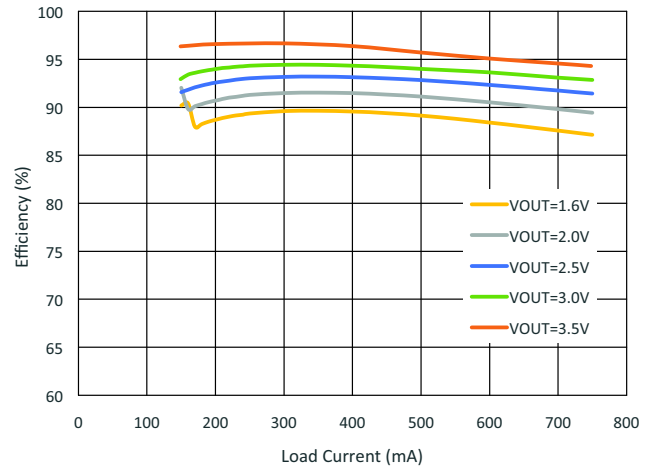
Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

## TYPICAL CHARACTERISTICS

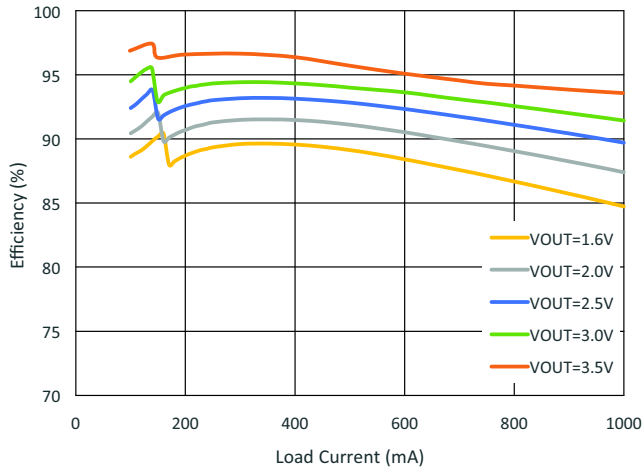
Unless otherwise noted,  $V_{IN} = EN = 3.8\text{ V}$ ,  $L = 1.0\text{ }\mu\text{H}$ ,  $C_{IN} = 10\text{ }\mu\text{F}$ ,  $C_{OUT} = 1 \times 4.7\text{ }\mu\text{F}$ ,  $2 \times 10\text{ }\mu\text{F}$ , and  $T_A = +25^\circ\text{C}$ .



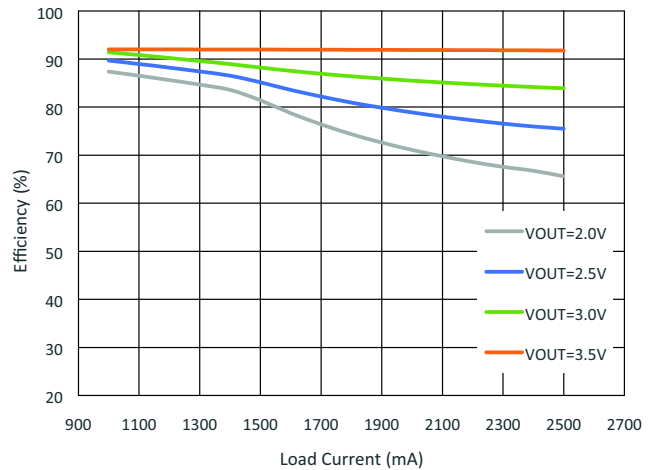
**Figure 5. Efficiency vs. Load Current and Output Voltage,  $V_{IN} = 3.8\text{ V}$ ,  $I_{OUT} = 10\text{ mA}$  to  $150\text{ mA}$**



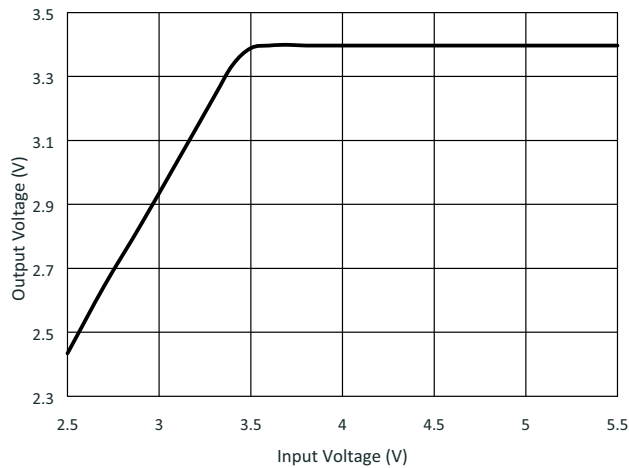
**Figure 6. Efficiency vs. Load Current and Output Voltage,  $V_{IN} = 3.8\text{ V}$**



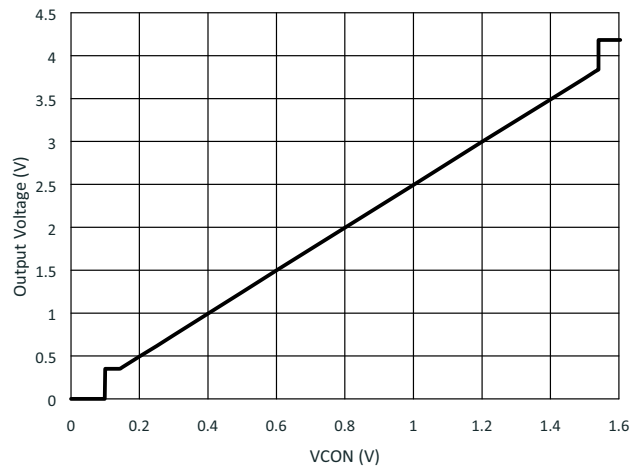
**Figure 7. Efficiency vs. Load Current and Output Voltage,  $V_{IN} = 3.8\text{ V}$ ,  $I_{OUT} = 100\text{ mA}$  to  $1\text{ A}$**



**Figure 8. Efficiency vs. Load Current and Output Voltage,  $V_{IN} = 3.8\text{ V}$ ,  $I_{OUT} = 1\text{ A}$  to  $2.5\text{ A}$**



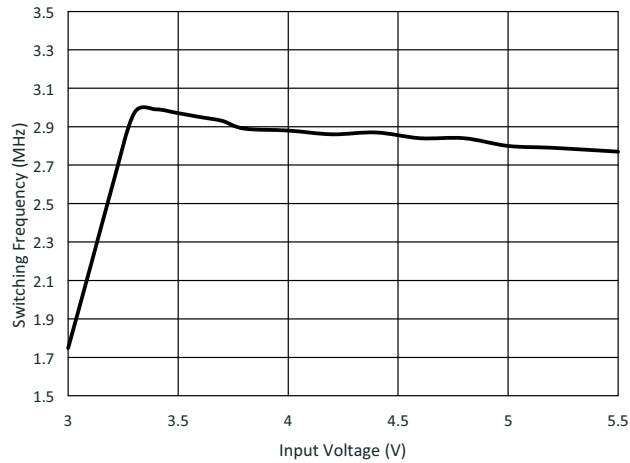
**Figure 9. Output Voltage vs. Supply Voltage,  $V_{OUT} = 3.4\text{ V}$ ,  $I_{OUT} = 1.5\text{ A}$ ,  $V_{IN} = 4.3\text{ V}$  to Dropout**



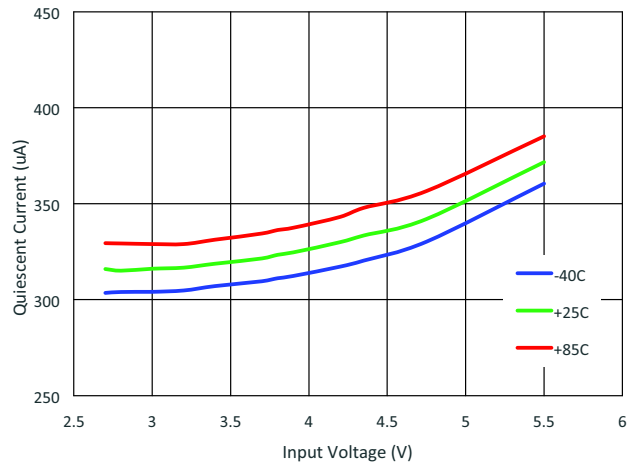
**Figure 10. Output Voltage vs.  $V_{CON}$  Voltage,  $V_{IN} = 4.2\text{ V}$ ,  $R_{LOAD} = 6.8\text{ }\Omega$ ,  $0.1\text{ V} < V_{CON} < 1.6\text{ V}$**

# TYPICAL CHARACTERISTICS

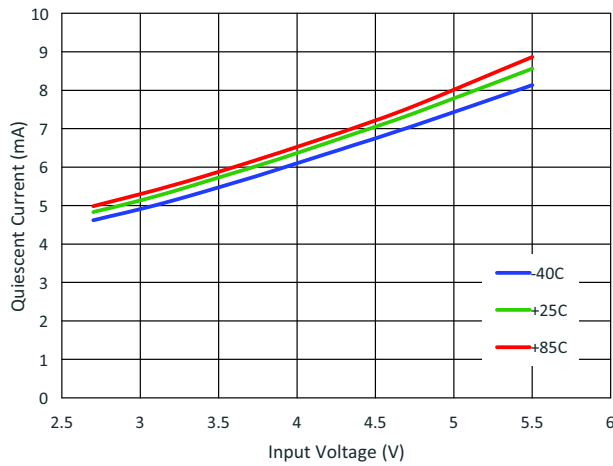
Unless otherwise noted,  $V_{IN} = EN = 3.8\text{ V}$ ,  $L = 1.5\text{ }\mu\text{H}$ ,  $C_{IN} = 10\text{ }\mu\text{F}$ ,  $C_{OUT} = 1 \times 4.7\text{ }\mu\text{F}$ ,  $2 \times 10\text{ }\mu\text{F}$ , and  $T_A = +25^\circ\text{C}$ .



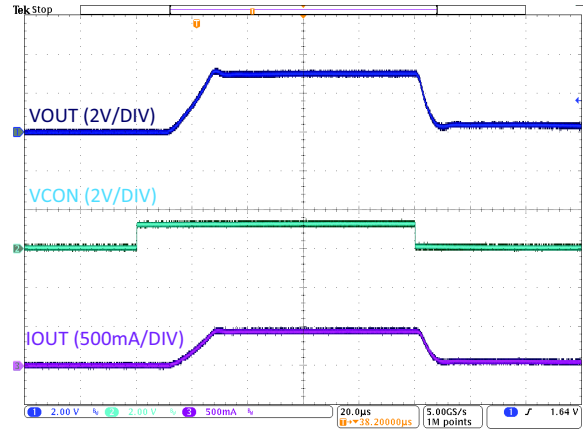
**Figure 11. Center-Switching Frequency vs. Supply Voltage,  $V_{OUT} = 2.5\text{ V}$ ,  $I_{OUT} = 700\text{ mA}$**



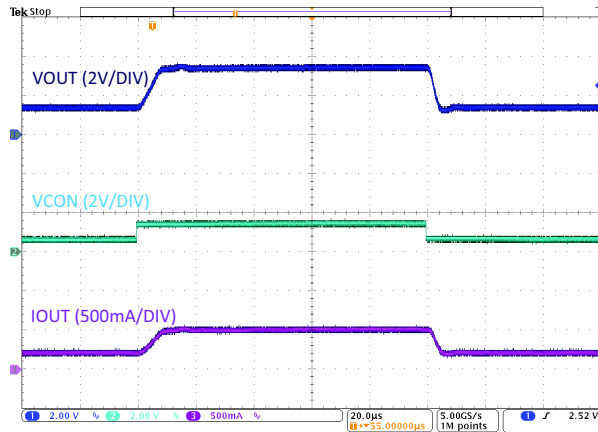
**Figure 12. Quiescent Current (PFM) vs. Supply Voltage,  $V_{OUT} = 1\text{ V}$ ,  $2.7\text{ V} < V_{IN} < 5.5\text{ V}$  (No Load)**



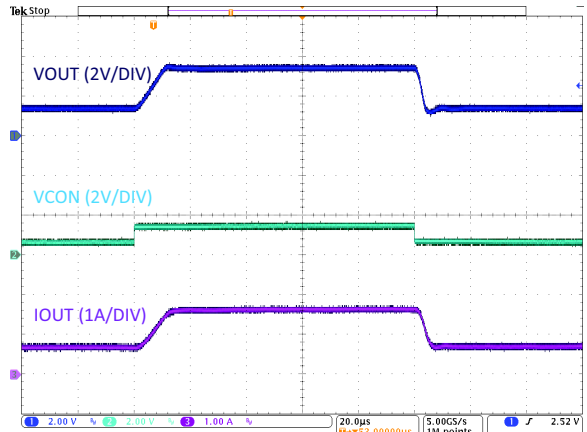
**Figure 13. Quiescent Current (PWM) vs. Supply Voltage,  $V_{OUT} = 2.5\text{ V}$ ,  $2.7\text{ V} < V_{IN} < 5.5\text{ V}$  (No Load)**



**Figure 14.  $V_{CON}$  Transient (3 G/4 G),  $V_{OUT} = 0\text{ V}$  to  $3\text{ V}$ ,  $R_{LOAD} = 6.8\text{ }\Omega$ ,  $V_{IN} = 3.8\text{ V}$ ,  $100\text{ ns}$  Edge**



**Figure 15.  $V_{CON}$  Transient (PFM to PWM),  $V_{OUT} = 1.4\text{ V}$  to  $3.4\text{ V}$ ,  $R_{LOAD} = 6.8\text{ }\Omega$ ,  $V_{IN} = 3.8\text{ V}$ ,  $100\text{ ns}$  Edge**



**Figure 16.  $V_{CON}$  Transient (PWM),  $V_{OUT} = 1.4\text{ V}$  to  $3.4\text{ V}$ ,  $R_{LOAD} = 1.9\text{ }\Omega$ ,  $V_{IN} = 4.2\text{ V}$ ,  $100\text{ ns}$  Edge**



## TYPICAL CHARACTERISTICS

Unless otherwise noted,  $V_{IN} = EN = 3.8\text{ V}$ ,  $L = 1.5\text{ }\mu\text{H}$ ,  $C_{IN} = 10\text{ }\mu\text{F}$ ,  $C_{OUT} = 1 \times 4.7\text{ }\mu\text{F}$ ,  $2 \times 10\text{ }\mu\text{F}$ , and  $T_A = +25^\circ\text{C}$ .

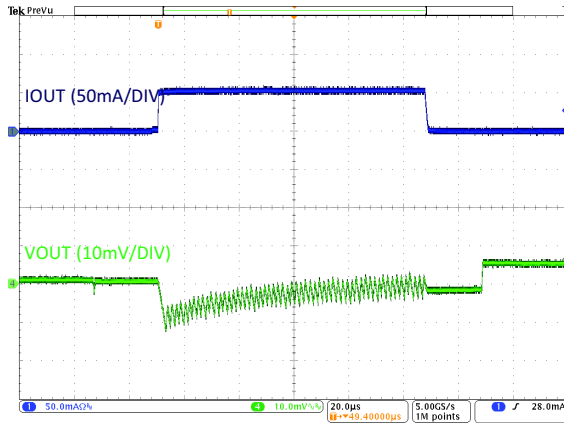


Figure 17. Load Transient in PFM Mode,  $V_{IN} = 3.6\text{ V}$ ,  $V_{OUT} = 1\text{ V}$ ,  $I_{OUT} = 0\text{ mA}$  to  $60\text{ mA}$ ,  $1\text{ }\mu\text{s}$  Edge

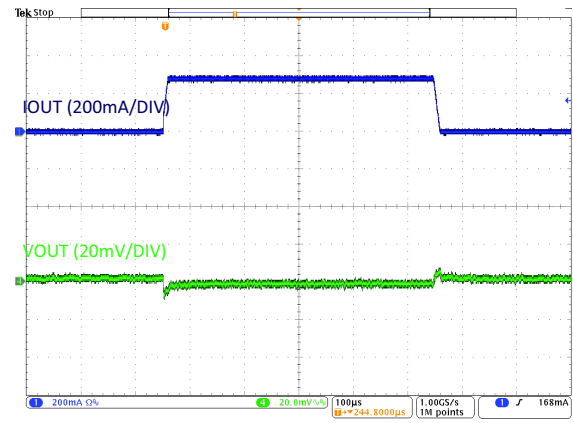


Figure 18. Load Transient in PWM Mode,  $V_{IN} = 3.8\text{ V}$ ,  $V_{OUT} = 2.5\text{ V}$ ,  $I_{OUT} = 0\text{ mA}$  to  $300\text{ mA}$ ,  $10\text{ }\mu\text{s}$  Edge

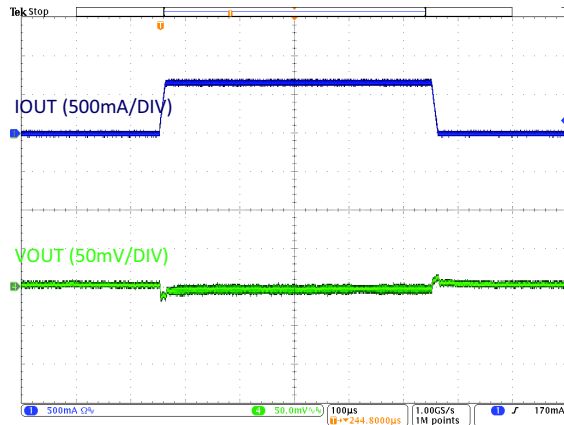


Figure 19. Load Transient in PWM Mode,  $V_{IN} = 3.8\text{ V}$ ,  $V_{OUT} = 3.0\text{ V}$ ,  $I_{OUT} = 0\text{ mA}$  to  $700\text{ mA}$ ,  $10\text{ }\mu\text{s}$  Edge

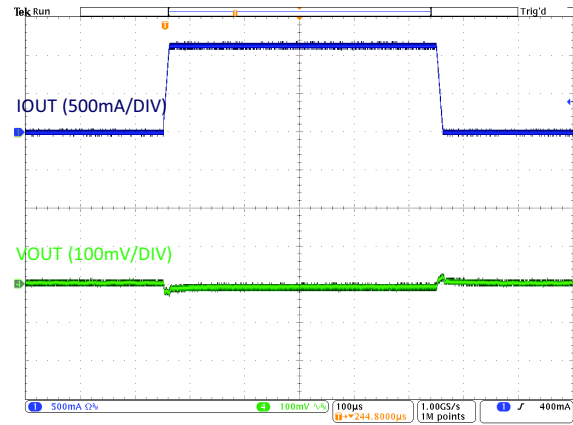


Figure 20. Load Transient in PWM Mode,  $V_{IN} = 4.2\text{ V}$ ,  $V_{OUT} = 3.0\text{ V}$ ,  $I_{OUT} = 0\text{ mA}$  to  $1.2\text{ A}$ ,  $10\text{ }\mu\text{s}$  Edge

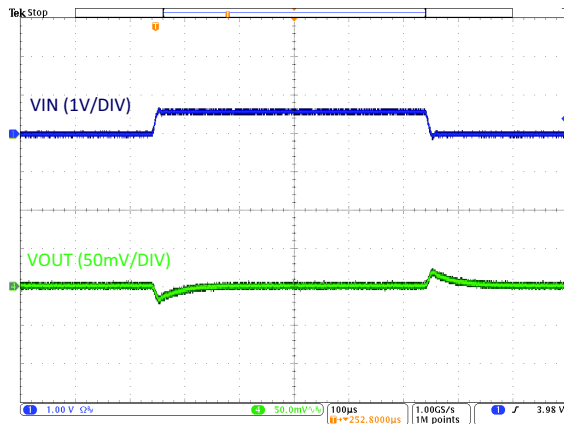


Figure 21. Line Transient,  $V_{IN} = 3.6\text{ V}$  to  $4.2\text{ V}$ ,  $V_{OUT} = 1.0\text{ V}$ ,  $6.8\text{ }\Omega$  Load,  $10\text{ }\mu\text{s}$  Edge

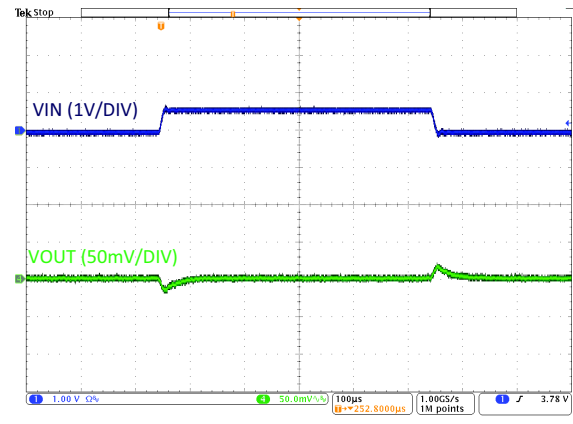
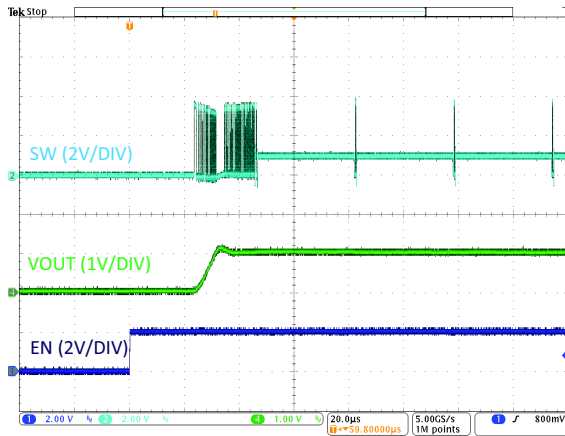


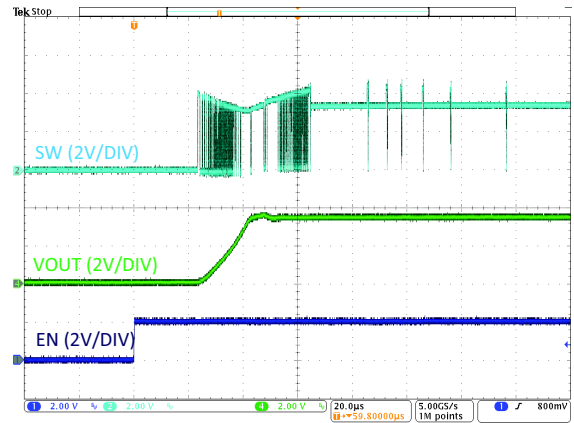
Figure 22. Line Transient,  $V_{IN} = 3.6\text{ V}$  to  $4.2\text{ V}$ ,  $V_{OUT} = 2.5\text{ V}$ ,  $6.8\text{ }\Omega$  Load,  $10\text{ }\mu\text{s}$  Edge

## TYPICAL CHARACTERISTICS

Unless otherwise noted,  $V_{IN} = EN = 3.8\text{ V}$ ,  $L = 1.5\text{ }\mu\text{H}$ ,  $C_{IN} = 10\text{ }\mu\text{F}$ ,  $C_{OUT} = 1 \times 4.7\text{ }\mu\text{F}$ ,  $2 \times 10\text{ }\mu\text{F}$ , and  $T_A = +25^\circ\text{C}$ .



**Figure 23. Startup in PFM Mode,  $V_{IN} = 3.8\text{ V}$ ,  $V_{OUT} = 1.0\text{ V}$ , No Load, EN = Low to High**



**Figure 24. Startup in PWM Mode,  $V_{IN} = 4.2\text{ V}$ ,  $V_{OUT} = 3.4\text{ V}$ , No Load, EN = Low to High**

## OPERATING DESCRIPTION

The FAN5910 is a high-efficiency, synchronous, step-down converter (DC-DC) with LDO-assist function.

The DC-DC converter operates with current-mode control and supports a wide range of load currents. High-current applications up to a 2.5 A DC output, such as mandated by GSM/EDGE applications, are allowed. Performance degradation due to spurs is removed by spreading the ripple energy through clock dither. A regulated Bypass Mode continues to regulate the output to the desired voltage as  $V_{IN}$  approaches  $V_{OUT}$ . The LDO offers a dropout voltage of approximately 100 mV under a 2 A load current.

The output voltage  $V_{OUT}$  is regulated to 2.5 times the input control voltage,  $V_{CON}$ , set by an external DAC. The FAN5910 operates in either PWM or PFM Mode, depending on the output voltage and load current.

**In Pulse Width Modulation (PWM) Mode,** regulation begins with on-state. A P-channel transistor is turned on and the inductor current is ramped up until the off-state begins. In the off-state, the P-channel is switched off and an N-channel transistor is turned on. The inductor current decreases to maintain an average value equal to the DC load current. The inductor current is continuously monitored. A current sense flags when the P-channel transistor current exceeds the current limit and the switcher is turned back to off-state to decrease the inductor current and prevent magnetic saturation. The current sense flags when the N-channel transistor current exceeds the current limit and redirects discharging current through the inductor back to the battery.

**In Pulse Frequency Modulation (PFM) Mode,** the FAN5910 operates in a constant on-time mode at low load currents. During on-state, the P-channel is turned on for a specified time before switching to off-state. In off-state, the N-channel switch is enabled until inductor current decreases to 0 A. The switcher enters three-state until a new regulation cycle starts.

PFM operation is allowed only in Low-Power Mode (MODE=1) for output voltages nominally less than 1.5 V. At low load currents, PFM achieves higher efficiency than PWM. The trade-off for efficiency improvement, however, is larger output ripple. Some applications, such as audio, may not tolerate the higher ripple, especially at high output voltages.

## DYNAMIC OUTPUT VOLTAGE TRANSITIONS

FAN5910 has a complex voltage transition controller that realizes fast transition times with a large output capacitor and output voltage ranges.

The transition controller manages five transitions:

- $\Delta V_{OUT}$  positive step
- $\Delta V_{OUT}$  negative step
- $\Delta V_{OUT}$  transition to or from 100% duty cycle
- $\Delta V_{OUT}$  transition at startup

In all cases, it is recommended that sharp  $V_{CON}$  transitions be applied, letting the transition controller optimize the output voltage slew rate.

### $\Delta V_{OUT}$ Positive Step

After a  $V_{CON}$  positive step, the FAN5910 enters Current-Limit Mode, where  $V_{OUT}$  ramps with a constant slew rate dictated by the output capacitor and the current limit.

### $\Delta V_{OUT}$ Negative Step

After a  $V_{CON}$  negative step, the FAN5910 enters Current Limit Mode where  $V_{OUT}$  is reduced with a constant slew rate dictated by the output capacitor and the current limit.

### $V_{OUT}$ Transition to or from Forced Bypass

The DC-DC is forced into 100% duty cycle for  $V_{CON}$  nominally greater than 1.6 V. This allows the output to be connected to the supply through both the low-resistance DC-DC and the LDO PFETs.

### $V_{OUT}$ Transition at Startup

At startup, after the EN rising edge is detected, the system requires 25  $\mu$ s for all internal voltage references and amplifiers to start before enabling the DC-DC converter function.

## MODE PIN

The MODE pin enable Forced PWM Mode or Auto PFM / PWM Mode. When the MODE pin is toggled HIGH (logic 1), the FAN5910 operates in PFM for  $V_{OUT} \leq 1.5$  V under light-load conditions and PWM for heavy-load conditions. If the MODE pin is set LOW (logic = 0), it operates in Forced PWM Mode.

### Auto PFM / PWM Mode (MODE = 1)

Auto PFM/PWM Mode is appropriate for 3G/3.5G and 4G applications.

### Forced PWM Mode (MODE = 0)

Forced PWM Mode is appropriate for applications that demand minimal ripple over the entire output voltage range.

### Bypass Mode

Bypass mode is entered based on the voltage difference between the battery voltage and the internal Vref voltage. The threshold when DCDC enters bypass mode is  $V_{IN} = V_{OUT} + 200$  mV. In bypass mode, the low  $R_{DS}$  on LDO PFET is active and the DCDC is running with 100% duty cycle, which allows very low voltage dropout and load current of up to 2.5 A.

Bypass mode can also be automatically entered when  $V_{con}$  exceeds 1.6 V and exits when  $V_{con}$  is below 1.4 V. When the BPEN pin is low, the FAN5910 runs in automatic bypass mode where bypass operation depends on  $V_{CON}$ . The BPEN pin set high can be used to ignore bypass flags and enable forced bypass mode. Bypass mode is active regardless of  $V_{CON}$  including overriding sleep mode when BPEN is high.

### DC-DC – LDO-ASSIST

The LDO-assist function maintains output regulation when  $V_{IN}$  approaches  $V_{OUT}$ , enables fast transition times under heavy loads, and minimizes PCB space by enabling a smaller inductor to be employed by using the LDO to provide a portion of the necessary load current.

The LDO-assist function limits the maximum current that the DC-DC may supply by shunting current away from the DC-DC under heavy loads and high duty cycles. In addition, the LDO-assist enables a seamless transition into 100% duty cycle, ensuring both low output ripple and constant output regulation. Since the LDO-assist function limits the maximum current supplied by the DC-DC, PCB area is minimized by enabling a lower current capable, and thus smaller form factor, inductor to be used.

### DC-DC – Sleep Mode

The Sleep Mode minimizes current while enabling rapid return to regulation. Sleep Mode is entered when  $V_{CON}$  is held below 70 mV for at least 40  $\mu$ s. In this mode, current consumption is reduced to under 50  $\mu$ A. Sleep Mode is exited after ~12  $\mu$ s when  $V_{CON}$  is set above 125 mV.

### APPLICATION INFORMATION

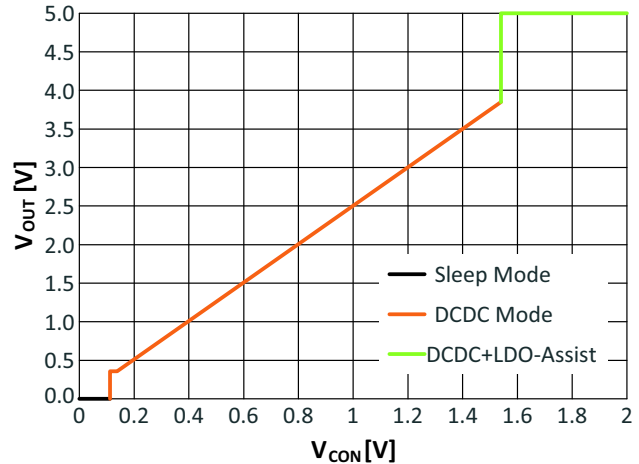
Figure 26 illustrates the FAN5910 in a GSM / EDGE / WCDMA transmitter configuration, driving multiple GSM / EDGE and 3G/3.5G and 4G PAs. Figure 27 presents a timing diagram designed to meet GSM specifications.

### DC Output Voltage

The output voltage is determined by  $V_{CON}$  provided by an external DAC or voltage reference:

$$V_{OUT} = 2.5 \times V_{CON} \quad (\text{eq. 1})$$

The FAN5910 provides regulated  $V_{OUT}$  only if  $V_{CON}$  falls within the typical range from 0.16 V to 1.44 V. This allows  $V_{OUT}$  to be adjusted between 0.4 V and 3.6 V. If  $V_{CON}$  is less than 0.16 V,  $V_{OUT}$  is clamped to 0.40 V. In Auto PFM/PWM Mode, the FAN5910 automatically switches between PFM and PWM. In Forced PWM Mode (MODE = 0), the FAN5910 automatically switches into PWM Mode.



**Figure 25. Output Voltage vs. Control Voltage**

The FAN5910 is designed to support fast voltage transients when configured for GSM/EDGE applications (MODE=0). Figure 28 shows a timing diagram for WCDMA applications.

# FAN5910

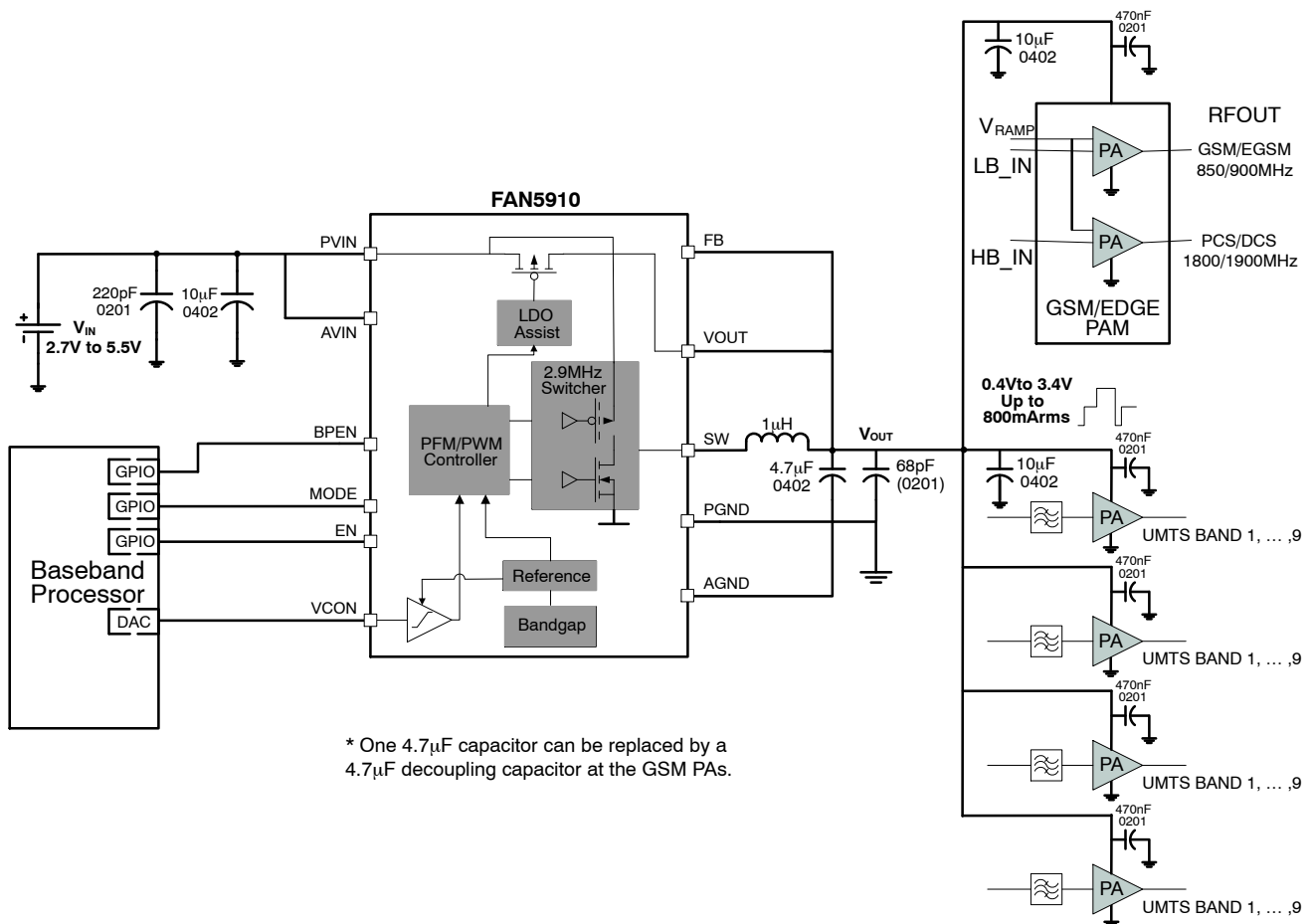


Figure 26. Typical Application Diagram with GSM/EDGE/WCDMA Transmitters

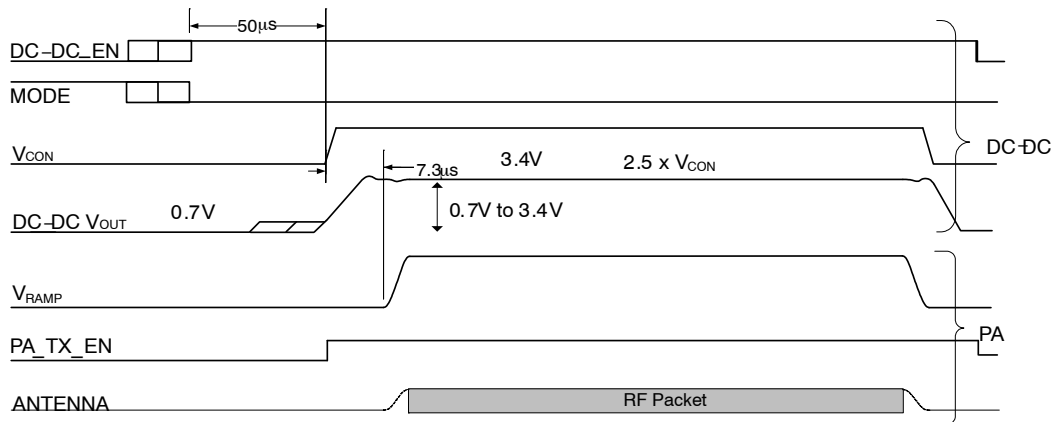
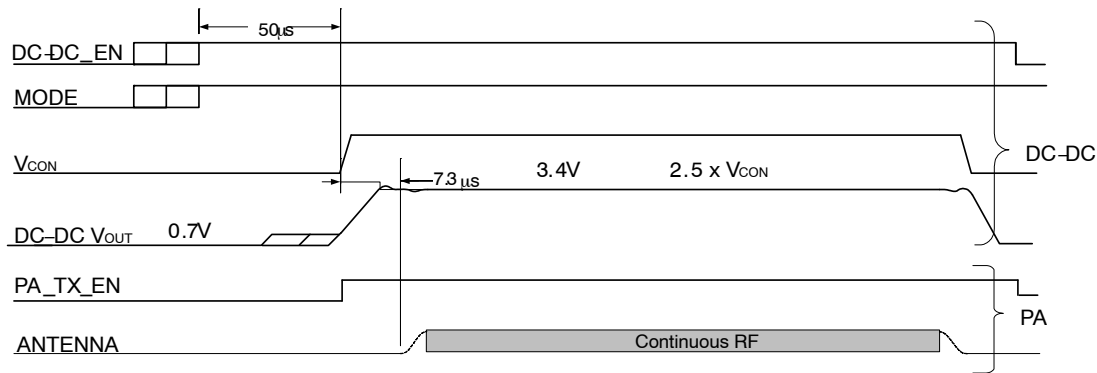


Figure 27. Timing Diagram for GSM/EDGE Transmitters

# FAN5910



**Figure 28. Timing Diagram for WCDMA Transmitters**

## Inductor Selection

The FAN5910 operates at 2.9 MHz switching frequency, allowing 1.0 µH or 1.5 µH inductors to be used in designs. For applications requiring the smallest possible PCB area, use a 1.0 µH 2012 inductor or a 1.0 µH 2016 inductor for optimum efficiency performance.

**Table 5. RECOMMENDED INDUCTORS**

| Inductor | Description  |
|----------|--|
| L        | 1.5 µH ±20%, 2.2 A, 2016 Case Size<br>Murata DFE201610C-1R5M   |
|          | 1.0 µH ±20%, 2.2 A, 2016 Case Size<br>Tokio: DFE201610R-H-1R0M |

## Capacitor Selection

The minimum required output capacitor C<sub>OUT</sub> should be one (1) 4.7 µF, 6.3 V, X5R with an ESR of 10 mΩ or lower and an ESL of 0.3 nH or lower in parallel after inductor L1. Larger case sizes result in increased loop parasitic inductance and higher noise. One 10 µF capacitor should be used as a decoupling capacitor at the GSM/EDGE PA V<sub>CC</sub> pin and another 10 µF capacitor should be placed at V<sub>CC</sub> pin of the 3G/4G PA.

A 6.8 pF capacitor may be added in parallel with C<sub>OUT</sub> to reduce the capacitor's parasitic inductance.

**Table 6. RECOMMENDED CAPACITOR VALUES**

| Capacitor        | Description  |
|------------------|--|
| C <sub>IN</sub>  | 10 µF, 20%, X5R, 10 V, 0402 (1005 metric)<br>Samsung CL05A106MP5NUNC     |
| C <sub>OUT</sub> | 4.7 µF, ±20%, X5R, 10 V, 0402 (1005 metric)<br>Murata GRM155R60J475ME47D |

## PCB Layout and Component Placement

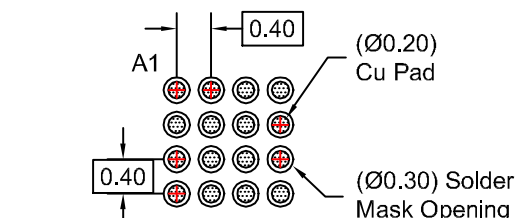
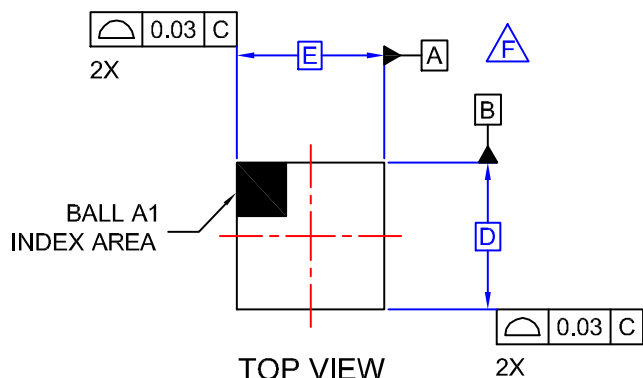
- The key point in the placement is the power ground (PGND) connection shared between the FAN5910, C<sub>IN</sub>, and C<sub>OUT</sub>. This minimizes the parasitic inductance of the switching loop paths.
- Place the inductor away from the feedback pins to prevent unpredictable loop behavior.
- Ensure the traces are wide enough to handle the maximum current value, especially in Bypass Mode.
- Ensure the vias are able to handle the current density. Use filled vias if available.

## PRODUCT SPECIFIC DIMENSIONS

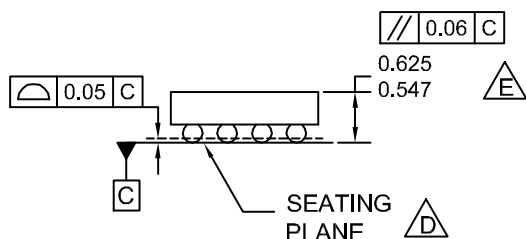
| D             | E             | X      | Y      | Unit |
|---------------|---------------|--------|--------|------|
| 1.615 ± 0.030 | 1.615 ± 0.030 | 0.2075 | 0.2075 | mm   |

CASE 567SD  
ISSUE 0

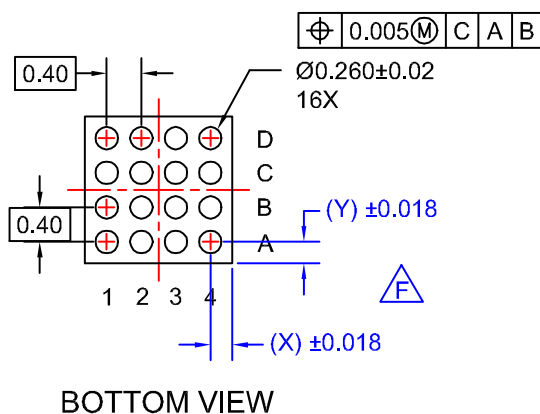
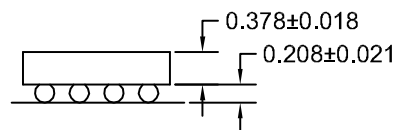
DATE 30 NOV 2016



### RECOMMENDED LAND PATTERN (NSMD PAD TYPE)



## SIDE VIEWS



NOTES:

- A. NO JEDEC REGISTRATION APPLIES.  
B. DIMENSIONS ARE IN MILLIMETERS.  
C. DIMENSIONS AND TOLERANCE  
PER ASME Y14.5M, 1994.

**D.** DATUM C IS DEFINED BY THE SPHERICAL CROWNS OF THE BALLS.

**E.** PACKAGE NOMINAL HEIGHT IS 586 MICRONS  
±39 MICRONS (547-625 MICRONS).

**F.** FOR DIMENSIONS D, E, X, AND Y SEE PRODUCT DATASHEET.

|                         |                                  |   |
|-------------------------|----------------------------------|---|
| <b>DOCUMENT NUMBER:</b> | <b>98AON16597G</b>               | Electronic versions are uncontrolled except when accessed directly from the Document Repository.<br>Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red. |
| <b>DESCRIPTION:</b>     | <b>WLCSP16 1.615x1.615x0.586</b> | <b>PAGE 1 OF 1</b>  |

**onsemi** and **onsemi** are trademarks of Semiconductor Components Industries, LLC dba **onsemi** or its subsidiaries in the United States and/or other countries. **onsemi** reserves the right to make changes without further notice to any products herein. **onsemi** makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. **onsemi** does not convey any license under its patent rights nor the rights of others.

**onsemi**, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at [www.onsemi.com/site/pdf/Patent-Marking.pdf](http://www.onsemi.com/site/pdf/Patent-Marking.pdf). **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

## ADDITIONAL INFORMATION

### TECHNICAL PUBLICATIONS:

Technical Library: [www.onsemi.com/design/resources/technical-documentation](http://www.onsemi.com/design/resources/technical-documentation)  
onsemi Website: [www.onsemi.com](http://www.onsemi.com)

### ONLINE SUPPORT: [www.onsemi.com/support](http://www.onsemi.com/support)

For additional information, please contact your local Sales Representative at  
[www.onsemi.com/support/sales](http://www.onsemi.com/support/sales)