FAN6241M6X

Secondary Side Synchronous Rectifier Controller for Flyback Converters

ON Semiconductor®

www.onsemi.com

SOT−23, 6 Lead
CASE 527AJ

Description

The FAN6241M6X is a secondary−side synchronous rectifier (SR) controller for an isolated flyback converter operating in Discontinuous Conduction Mode (DCM). The adaptive dead−time control algorithm minimizes the body diode conduction of SR MOSFET while guaranteeing stable and robust SR operation against noise and disturbance caused by the circuit parasitic components. The 26 V rated input voltage LDO and Low VDD Under−Voltage Lockout (UVLO) voltage allow FAN6241M6X to be used for wide ranges of switched mode power supply output voltage without additional circuit.

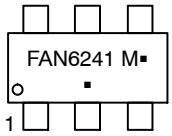
Features

- Support Discontinuous Conduction Modes (DCM) and Boundary Conduction Mode (BCM)
- Adaptive Turn−off Dead Time Tuning for General SR MOSFET Application
- 120 V of Voltage Rating on the Drain Pin
- Charge Pump (CP) Function which Enhance SR MOSFET Voltage Driving Level through Connected a Ceramic Capacitor between Gate and CP Pin
- Short Turn−on Delay (20 ns)
- Supporting PD General Output Voltage (VIN) Range: 3.25 V~25 V with LDO Input
- Fewest External Component Allowed
- At Green mode SR Driving Signal is Still Working under Extremely Low Power Consumption
- Small Footprint: SOT−23 6 pin
- These Device is Pb−Free and is RoHS Compliant

Typical Applications

- Travel Adapter for Smart Phones, Feature Phones, and Tablet PCs
- AC−DC Adapters for Portable Devices that Require CV/CC Control
- IoT Power Applications5tt

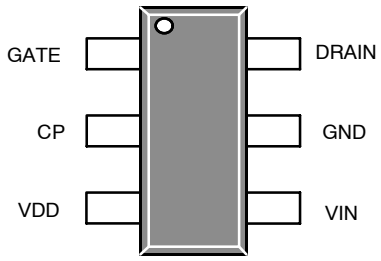
MARKING DIAGRAM



FAN6241	= Specific Device Code
M	= Date Code
▪	= Pb−Free Package

(Note: Microdot may be in either location)

PIN CONNECTIONS



ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

ORDERING INFORMATION

Part Number	Operating Temperature	Package	Packing Method
FAN6241M6X	−40°C ~125°C	6−Lead, SOT23 (Pb−Free)	3000 / Tap & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

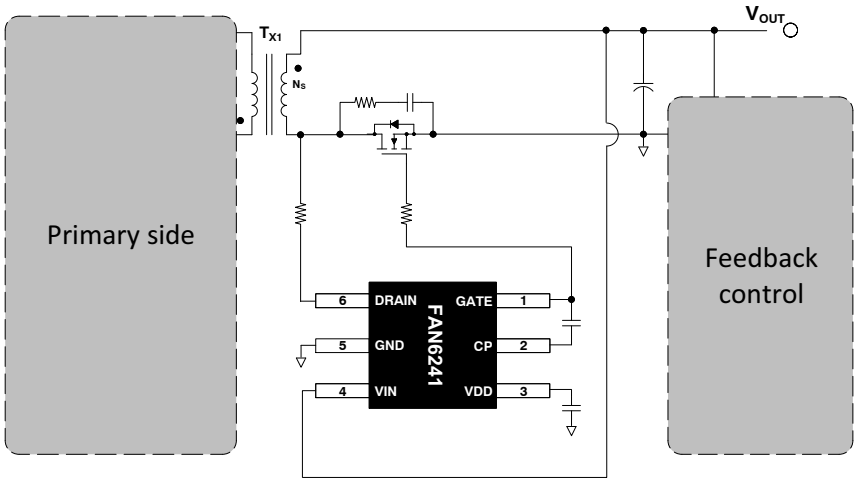


Figure 1. FAN6241M6X Typical Application Schematic

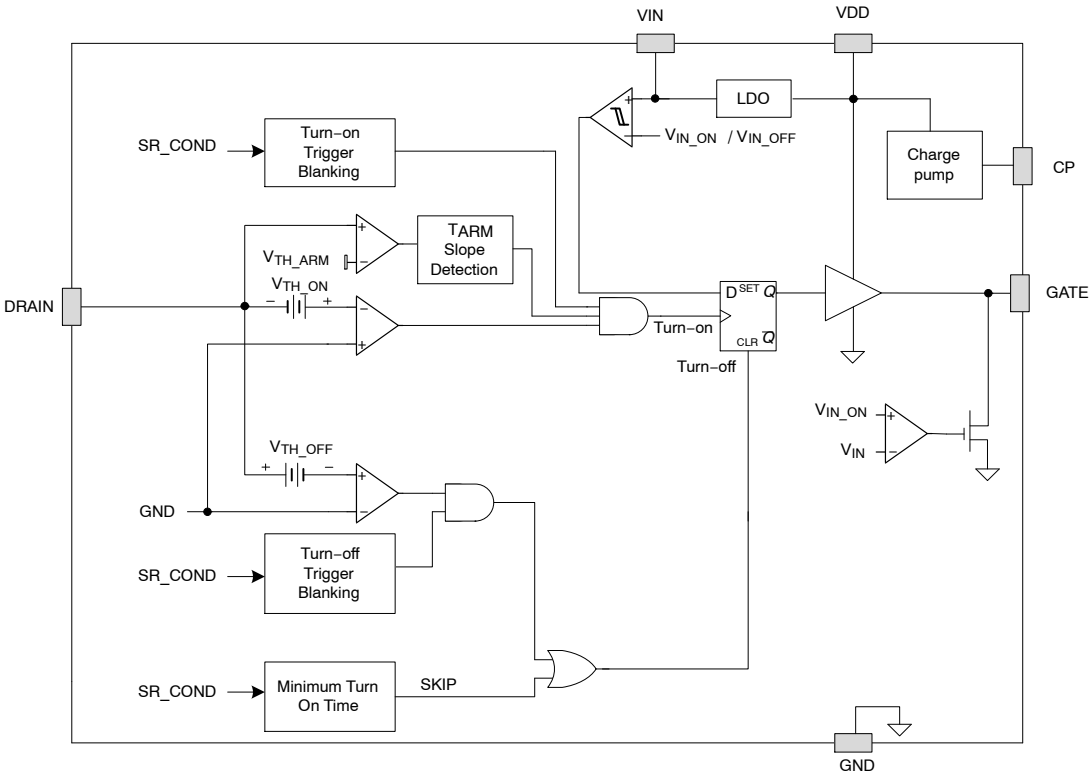


Figure 2. FAN6241M6X Function Block Diagram

PIN FUNCTION DESCRIPTION

Pin #	Name	Description
1	GATE	Gate drive output pin
2	CP	SR gate charge pump. connect one 3.3 nF capacitor to GATE pin
3	VDD	Internal regulator 5 V output and gate drive power supply rail. Bypass with 1 μF capacitor to GND
4	VIN	LDO input, supports up to 26 V operation. An integrated 5 V LDO generates the internal VDD power supply rail for the low−voltage control circuitry
5	GND	Ground pin
6	DRAIN	Synchronous rectifier drain sense input

ABSOLUTE MAXIMUM RATINGS (Notes 1, 2, 3)

Parameter	Symbol	Min.	Max.	Unit
V_{IN}	Power Supply Input Pin Voltage	−0.3	26	V
V_{DD}	Internal Regulator Output Pin Voltage	−0.3	6.5 V	V
V_{DRAIN}	Drain Sense Input Pin Voltage	−1	120	V
V_{GATE}	Gate Drive Output Pin Voltage	−0.3	6.5 V	V
CP	Charge pump Pin Voltage	−0.3	6.5 V	V
P_D	Power Dissipation (T_A = 25°C)		540	mW
θ_{JA}	Thermal Resistance (Junction−to−Ambient Thermal)		230	°C/W
T_J	Operating Junction Temperature	−40	125	°C
T_{STG}	Storage Temperature Range	−60	150	°C
T_L	Lead Temperature (Soldering) 10 Seconds		260	°C
Electrostatic Discharge Capability	Human Body Model, ANSI / ESDA / JEDEC JS−001−2012		2.0	kV
	Charged Device Model, JESD22−C101		0.5	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. All voltage values, except differential voltages, are given with respect to the GND pin.
2. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device.
3. Meets JEDEC standards JS−001−2012 and JESD 22−C101.

THERMAL CHARACTERISTICS (Note 4)

Parameter	Symbol	Min	Unit
Junction−to−Ambient Thermal Impedance	θ_{JA}	230	°C/W
Junction−to−Top Thermal Impedance	θ_{JT}	36	°C/W

4. T_A = 25°C unless otherwise specified.

RECOMMENDED OPERATING RANGES (Note 5)

Parameter	Symbol	Min.	Max.	Unit
Power Supply Input Pin Voltage	V_{VIN}	2.8	20	V
Internal Regulator Output Pin Voltage	V_{VDD}	2.8	6	V
Drain Sense Input Pin Voltage	V_{DRAIN}	−0.3	100	V
Gate Drive Output Pin Voltage	V_{GATE}	−0.3	6	V
Charge pump Pin voltage	V_{CP}	0	5.5	V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

5. The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance. On Semiconductor does not recommend exceeding them or designing to Absolute Maximum Ratings.

ELECTRICAL CHARACTERISTICS V_{IN} = 5.5 V and T_A = −40~125°C unless noted

Parameter	Conditions	Symbol	Min.	Typ.	Max.	Unit
VDD SECTION						
Turn−On Threshold	V_{IN} rising	V_{IN-ON}	3.06	3.38	3.70	V
Turn−Off Threshold	V_{IN} falling	V_{IN-OFF}	2.78	2.915	3.050	V
Operating Current	f_{SW} = 100 kHz, C_{iss} = 3.3 nF, V_{IN} = 5 V	I_{IN-OP}	–	2.0	3.5	mA
Operating Current at green mode	f_{SW} = 100 Hz, C_{iss} = 3.3 nF, V_{IN} = 5 V	$I_{IN-GREEN}$	–	250	350	μA
POWER SUPPLY SECTION						
Internal LDO Output Voltage	V_{IN} = 20 V	V_{DD}	5.10	5.35	5.60	V
Dropout Voltage of LDO	I_{OUT} = 10 mA, V_{IN} = 3.3 V	V_{DO}	–	–	0.3	V
DRAIN VOLTAGE SENSING SECTION						
Comparator Input Offset Voltage	Internal design suggestion	V_{OSI} (Note 6)	−1	0	1	mV
Turn−On Threshold Voltage	R_{DRAIN} = 0 Ω (includes comparator input offset voltage)	V_{TH-ON}	−250	−200	−150	mV
Turn−Off Threshold Tuning Range	15 Steps	V_{TH-OFF}	−5	–	5	mV
Turn−On Delay	With 50 mV overdrive From V_{TH-ON} to V_{GATE} = 1 V	$t_{ON.DLY}$ (Note 6)	–	20	–	ns
Turn−Off Delay	With 0 mV overdrive From V_{TH-OFF} to V_{GATE} voltage = 1 V	$t_{OFF-DLY}$ (Note 6)	–	20	–	ns
Slope detection disable criteria		$t_{SLO-DIS}$	–	100	–	μs
Gate Re−arming threshold	V_{IN} = 5 V (Typically 0.65V_{DD})	V_{TH-ARM}	3.00	3.25	3.50	V
Gate Re−arming time for slope detection		t_{ARM} (Note 6)	75	90	105	ns
Slope detection high threshold		V_{TH-HGH} (Note 6)	0.4	0.5	0.6	V
MINIMUM ON−TIME AND MINIMUM OFF−TIME SECTION						
Adaptive Minimum On−Time Ratio	Ratio between minimum on time and SR conduction of previous switching cycle	K_{TON} (Note 6)	–	50	–	%
Minimum On−Time low value		$t_{ON-MIN-LL}$	300	450	600	ns
Minimum On−Time High value		$t_{ON-MIN-UL}$	1	2	3	μs
Minimum Off−Time		$t_{OFF-MIN}$	1.0	1.2	1.4	μs
DEAD TIME CONTROL SECTION						
Dead time self−tuning target	From GATE OFF to V_{DRAIN} rising above 0.5 V	t_{DEAD} (Note 6)	150	200	230	ns

ELECTRICAL CHARACTERISTICS V_{IN} = 5.5 V and T_A = −40~125°C unless noted

Parameter	Conditions	Symbol	Min.	Typ.	Max.	Unit
GREEN MODE CONTROL						
Gate Period of enter green mode		$t_{GREEN-ON}$	240	300	360	μs
Gate period of leave green mode −min		$t_{GREEN-OFF-min}$	80	100	120	μs
Gate period of leave green mode −max		$t_{GREEN-OFF-max}$	120	150	180	μs
Gate cycle of leave green mode	$t_S < t_{GREEN-OFF-min}$	$N_{GREEN-OFF}$	–	32	–	Cycles
OUTPUT DRIVER SECTION						
Output Voltage Low	V_{IN} = 6 V	V_{OL}	–	–	0.25	V
Output Voltage High	V_{IN} = 6 V	V_{OH}	5.0	5.5	6.0	V
Rise Time	V_{IN} = 5 V, C_L = 3300 pF, GATE = 1 V~4 V	t_R	–	–	24	ns
Fall Time	V_{IN} = 5 V, C_L = 3300 pF, GATE = 4 V~1 V	t_F	–	–	21	ns
Gate voltage during charge pump	V_{IN} = 3.3 V, C_{LOAD} = 3300 pF, Ciss = 4.7 ns, fs = 100 Hz	$V_{GATE-CP}$	4.0	5.0	6.0	V
Gate clamping level before IC turn on	$V_{IN} < V_{IN-ON}$, C_{LOAD} = 3300 pF	$V_{0V-CLAMP}$	–	–	0.5	V
CP function enable level	High to low enable level	V_{CP-EN}	4.30	4.45	4.60	V
CP function disable level	Low to high disable level	V_{CP-DIS}	4.610	4.755	4.900	V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

6. Guaranteed by Design.

TYPICAL PERFORMANCE CHARACTERISTICS

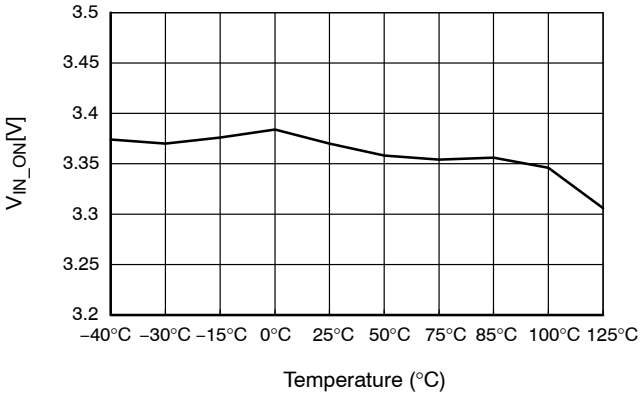


Figure 3. V_{IN_ON} vs. Temperature

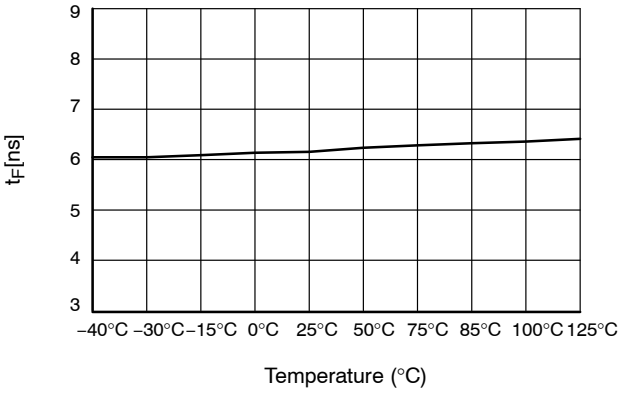


Figure 4. t_F vs. Temperature

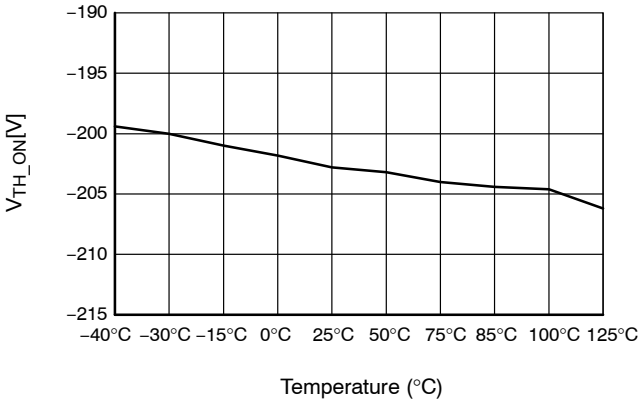


Figure 5. V_{TH_ON} vs. Temperature

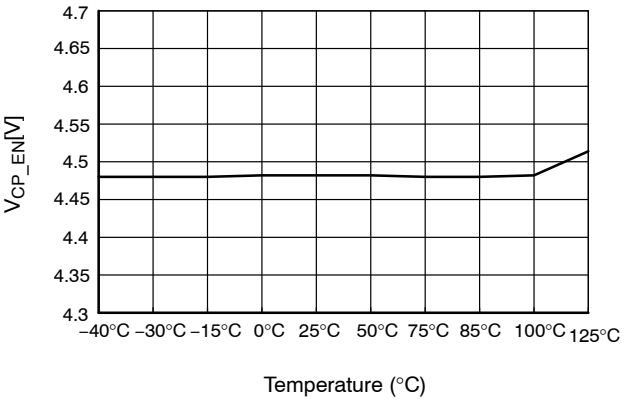


Figure 6. V_{CP_EN} vs. Temperature

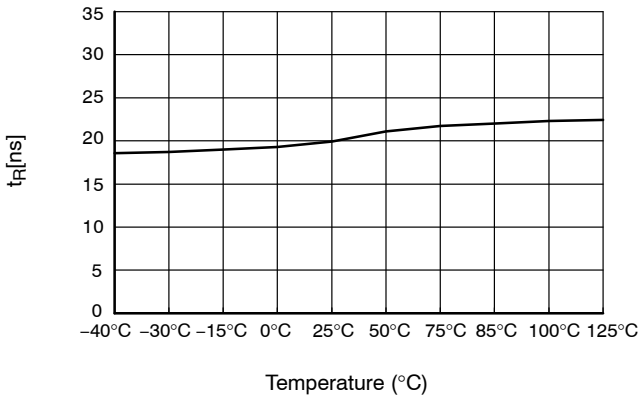


Figure 7. t_R vs. Temperature

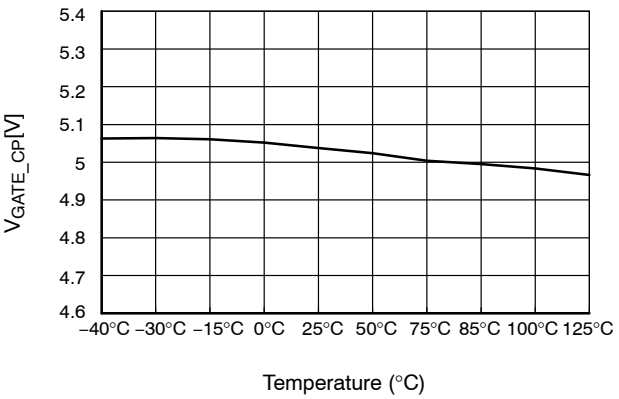


Figure 8. V_{GATE_CP} vs. Temperature

FUNCTIONAL DESCRIPTION

Theory of SR Control Operation

For an ideal circuit operation, the SR control algorithm of FAN6241M6X is very straightforward. FAN6241M6X controls the SR MOSFET based on the instantaneous Drain−to−Source voltage as illustrated in Figure 9. When the body diode starts conducting, the drain−to−source voltage drops below the turn−on threshold (V_{TH-ON}) which triggers the turn−on of the gate. Then the product of R_{DS_ON} and instantaneous SR current determines the Drain−to−Source voltage. When the drain−to−source voltage reaches the turn−off threshold (V_{TH-OFF}) as SR MOSFET current decreases to near zero, FAN6241M6X turns off the gate. If the turn off threshold (V_{TH-OFF}) is 0 V and no stray inductance from MOSFET package and PCB layout, there is no dead time which is an ideal case.

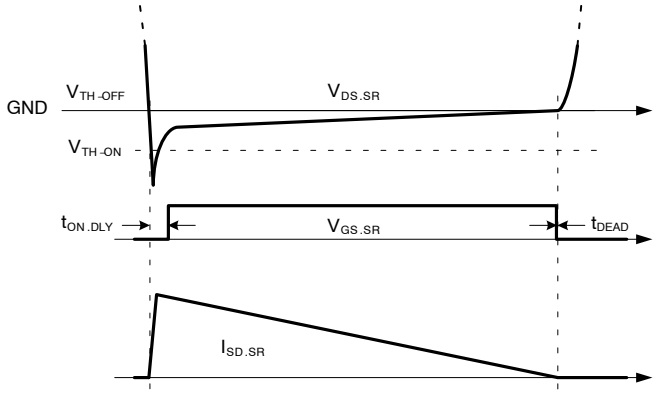


Figure 9. SR MOSFET Operation Waveforms (Ideal Case)

SR Turn−On Algorithm

As the diagram shown in Figure 10, the turn−on of SR GATE is triggered by the three input signals of AND gate. The first input signal is TURN_ON_ALLOW signal, which is given after $t_{OFF-MIN}$ from the falling edge of $V_{GS.SR}$ signal. The second input is the TURN_ON_TRG signal, which is enable after DRAIN pin voltage drops below V_{TH-ON}. The third signal is t_{ARM} which allows turn−on trigger only when SR drain voltage drops fast with a large slope, preventing SR from triggering by the drain resonance voltage in DCM operation.

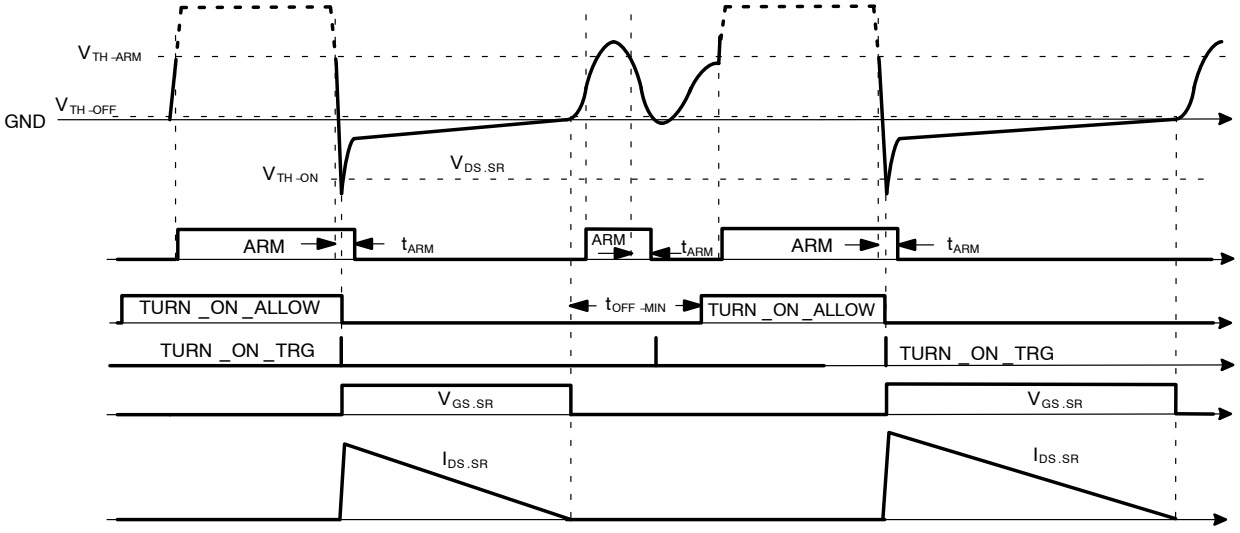


Figure 10. Turn−On Algorithm

SR Turn−Off Algorithm

As diagram shown in Figure 11, the turn−off of SR GATE is triggered by the two input signals of AND gate. The first input signal is turn off signal, which is enabled when $V_{DS.SR}$>V_{TH_OFF}. The second input is TURN_OFF_ALLOW signal given from the adaptive turn−off blanking. The blanking time is adaptively determined as half of SR conduction time (SR_COND) of the previous switching cycle for better noise immunity. V_{TH_OFF} is automatically adjusted based on the dead time to minimize the conduction time of the body diode of SR FET.

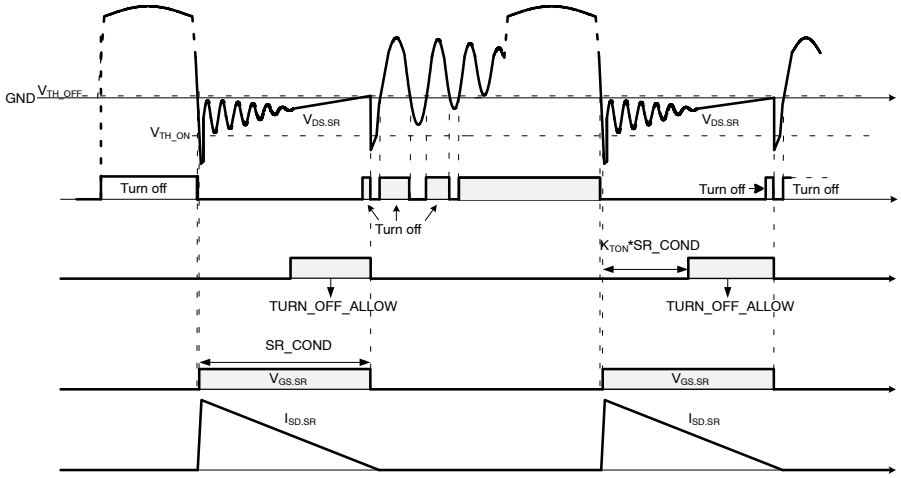


Figure 11. SR Turn−Off Algorithm

Dead Time Tuning

When the drain−to−source voltage reaches the turn−off threshold (V_{TH-OFF}) as SR MOSFET current decreases to near zero, FAN6241M6X turns off the gate. However, usually there also exists voltage offset induced by the stray inductance of MOSFET package and PCB layout. Therefore, it is very difficult to optimize dead time against all the circuit tolerances and operating conditions. FAN6241M6X implements dead time self−tuning control block in Figure 12. FAN6241M6X tries to optimize dead time to 190 ns(typ.) by modulating the V_{TH-OFF} level. The V_{TH-OFF} adjustment range is from − 5 mV to +5 mV with 4 bits resolution. Each step of V_{TH-OFF} adjustment is 0.156 mV per bit. FAN6241M6X optimizes the dead time by increasing V_{TH-OFF} step by step until T_{DEAD} is shorter than targeting dead time 200 ns(typ.).

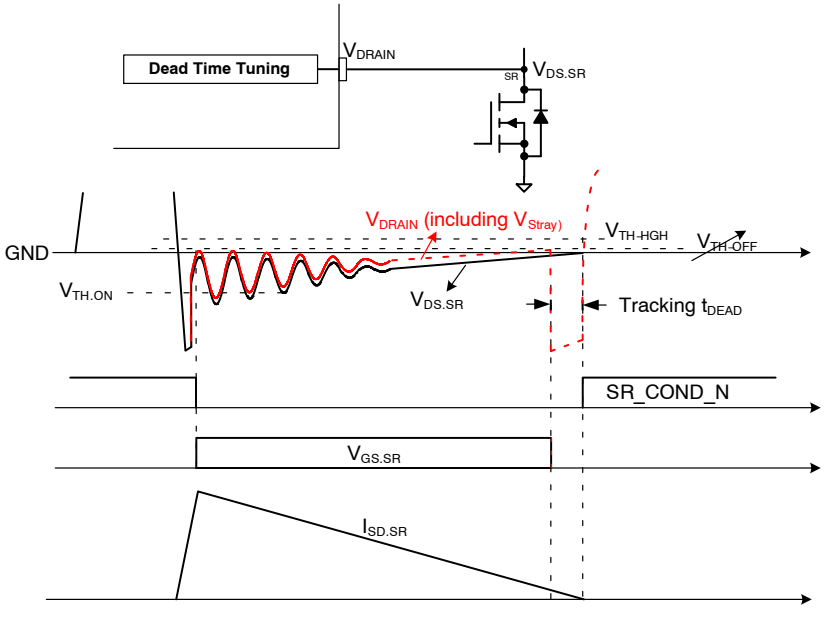


Figure 12. SR Dead Time Tracking

Charge Pump

Generally, SR driving voltage is powered by V_{DD} through VIN to drive SR MOSFET through GATE pin so the GATE driving voltage be higher than VIN. When VIN is low, FET is not fully turned on, high conduction loss is inevitable and suffers total system efficiency. In order to achieve system high efficiency and low MOSFET thermal performance at low system output voltage (low VIN) with high output current application case, GATE voltage boosting function is introduced as Figure 13.

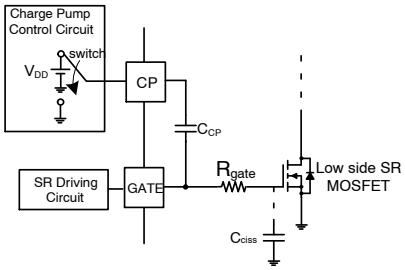


Figure 13. Charge Pump Control Circuit

Non−logic MOSFET, that have conventional gate on threshold, is around 4 V(max) of gate threshold voltage. FAN6241M6X's internal charge pump works as Figure 14 to raise gate voltage, V_{OH}. During blanking time the switch inside Charge Pump Control Circuit will switch to GND in order to have C_{CP} charge via SR Driving Circuit. After blanking time, the switch will connect to V_{DD} to boost V_{OH}. The V_{OH} will be clamped to 5.5 V(typ.) to ensure the voltage no higher than pin maximum rating to ensure driving circuit safe operation. An adequate C_{CP} capacitance is required to achieve reasonable GATE drive voltage for different SR MOSFET selection. While C_{CP} capacitance is larger, the higher is V_{OH} voltage that will have smaller MOSFET R_{ds-on}. However, charging current from SR Driving Circuit takes longer time to charge C_{iss} and C_{CP}. In the end of blanking time larger C_{CP} has higher V_{OH} level but slower V_{OH} rising rate to late turn on MOSFET. R_{gate} used for EMI solution also will reduce SR Driving Circuit charging current to slow down V_{OH} rising rate as well.

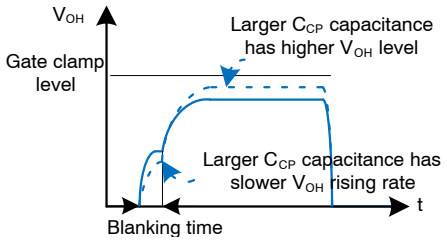


Figure 14. Timing Flow of Charge Pump

Below summarize all kinds of C_{CP} and R_{gate} combination results which needs to trade off for EMI and efficiency

- C_{CP} capacitance increase→ Slower V_{OH} rising rate but greater V_{OH}
- C_{CP} capacitance decrease→ Faster V_{OH} rising rate but less V_{OH}
- R_{gate} increase→ Slower V_{OH} rising rate and lower V_{OH} with better EMI
- R_{gate} decrease→ Faster V_{OH} rising rate and higher V_{OH} but poor EMI

As real test Figure 15 and Figure 16 using C_{CP} = 2.2 nF and 10 nF are half and double size of C_{iss}= 5.32 nF (typ.) of MOSFET NVMFS6B03NL respectively with 10 Ω R_{gate}. At 3.3 V V_{BUS} which is the minimum output voltage for example, the V_{OH} is 4.16 V and 4.97 V with C_{CP} = 2.2 nF and 10 nF respectively that allow user to use non−logic MOSFET for to achieve cost effective.

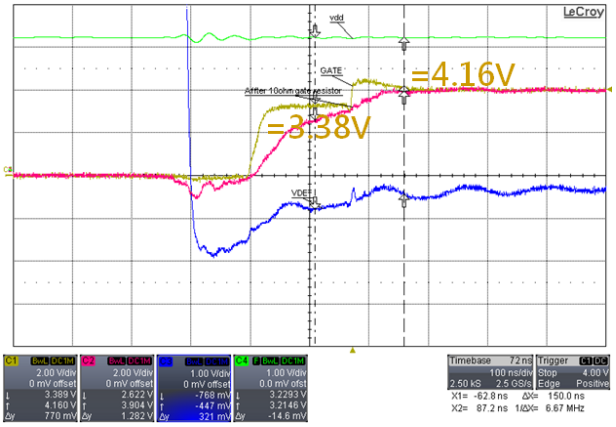


Figure 15. V_{OH} Level with C_{CP} = 2.2 nF (ch1: GATE pin; ch2: MOSFET Vgs; ch3 : V_{RAIN} : ch4 : VDD)

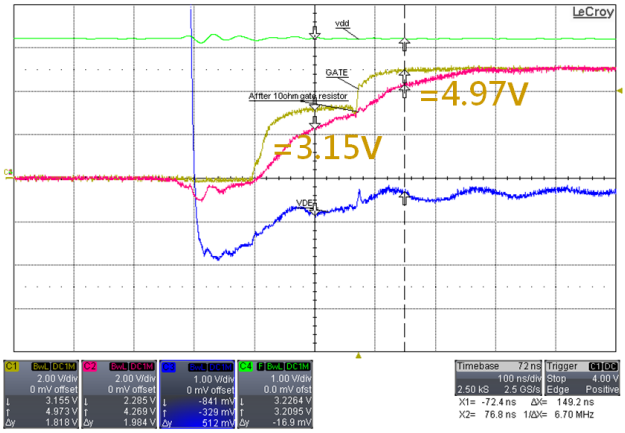


Figure 16. V_{OH} Level with C_{CP} = 10 nF (ch1: GATE pin; ch2: MOSFET Vgs; ch3 : VRAIN : ch4 : VDD)

PCB LAYOUT GUIDANCE

Printed Circuit Board (PCB) Layout

- Better PCB layout improves and minimizes excessive EMI and prevents power supply from being disrupted during ESD/Surge test. Figure 17 shows the layout guidance for low−side system

IC Side:

- Due to VDS direct sensing method, trace1 (light blue) should be as short as possible to have better noise immunity
- GND pin is also to be routed close to the source of SR FET Q2, with short routings

System Side:

- Y−cap is connected to output cap directly as trace2 (orange)

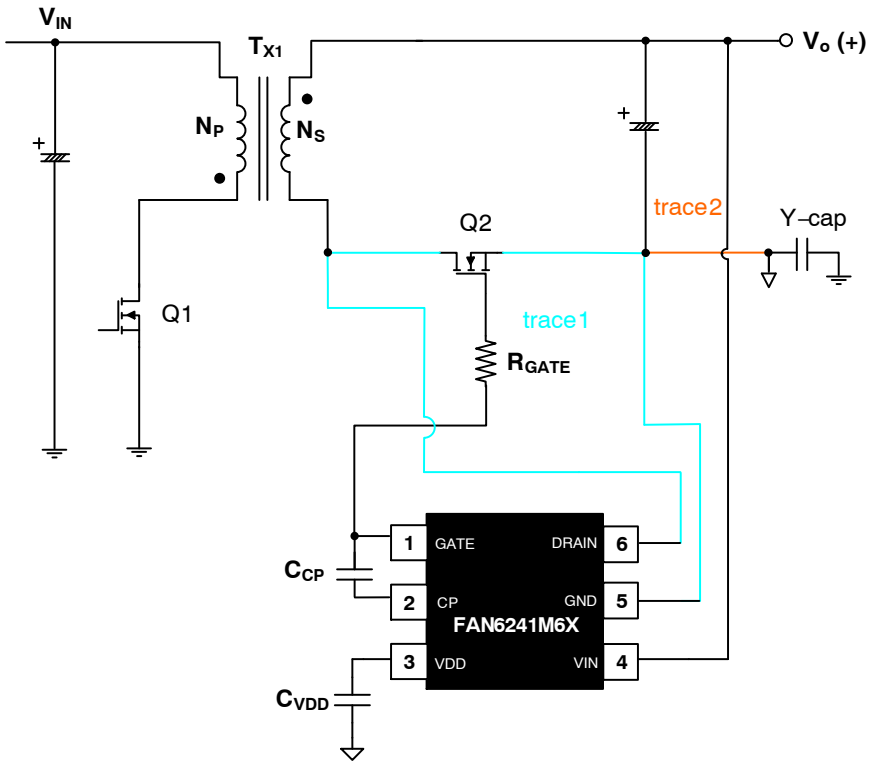
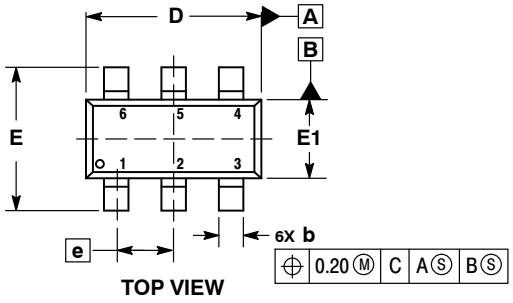


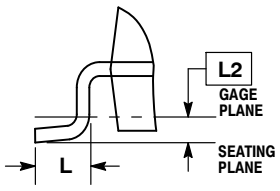
Figure 17. SR Layout Considerations of Low−Side System

SOT−23, 6 Lead
CASE 527AJ
ISSUE B

DATE 29 FEB 2012

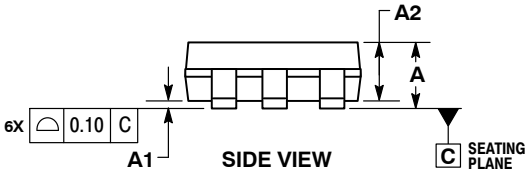
SCALE 2:1

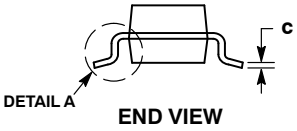




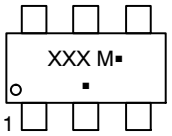
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DATUM C IS THE SEATING PLANE.

	MILLIMETERS	
DIM	MIN	MAX
A	---	1.45
A1	0.00	0.15
A2	0.90	1.30
b	0.20	0.50
c	0.08	0.26
D	2.70	3.00
E	2.50	3.10
E1	1.30	1.80
e	0.95 BSC	
L	0.20	0.60
L2	0.25 BSC	





GENERIC MARKING DIAGRAM*

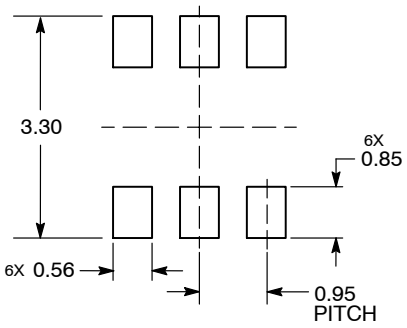


XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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