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FCD4N60

N 沟道 SuperFET® MOSFET

600 V, 3.9 A, 1.2 Ω

特性

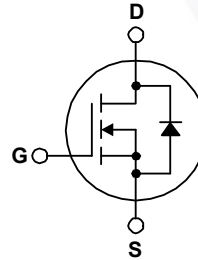
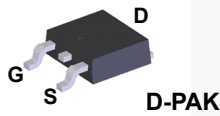
- 650 V @ $T_J = 150^\circ\text{C}$
- $\text{Typ. } R_{DS(on)} = 1.0 \Omega$
- 超低栅极电荷 (典型值 $Q_g = 12.8 \text{ nC}$)
- 低有效输出电容 (典型值 $C_{oss,eff} = 32 \text{ pF}$)
- 100% 经过雪崩测试
- 符合 RoHS 标准

说明

SuperFET® MOSFET 是飞兆半导体第一代利用电荷平衡技术实现出色低导通电阻和更低栅极电荷性能的高压超级结 (SJ) MOSFET 系列产品。这项技术专用于最小化导通损耗并提供卓越的开关性能、dv/dt 额定值和更高雪崩能量。因此, SuperFET MOSFET 非常适合开关电源应用, 如功率因数校正 (PFC)、服务器 / 电信电源、平板电视电源、ATX 电源及工业电源应用。

应用

- 照明
- AC-DC 电源
- 光伏逆变器



MOSFET 最大额定值 $T_C = 25^\circ\text{C}$ 除非另有说明。

符号	参数	FCD4N60TM	单位
V_{DSS}	漏极-源极电压	600	V
I_D	漏极电流	- 连续 ($T_C = 25^\circ\text{C}$)	3.9
		- 连续 ($T_C = 100^\circ\text{C}$)	2.5
I_{DM}	漏极电流	- 脉冲 (说明 1)	11.7
V_{GSS}	栅极-源极电压	± 30	V
E_{AS}	单脉冲雪崩能量	(说明 2)	128
I_{AR}	雪崩电流	(说明 1)	3.9
E_{AR}	重复雪崩能量	(说明 1)	5.0
dv/dt	二极管恢复 dv/dt 峰值	(说明 3)	4.5
P_D	功耗	($T_C = 25^\circ\text{C}$)	50
		- 超过 25°C 时降低	0.4
T_J, T_{STG}	工作和存储温度范围	-55 至 +150	$^\circ\text{C}$
T_L	用于焊接的最高引脚温度, 距离外壳 1/8", 持续 5 秒	300	$^\circ\text{C}$

热性能

符号	参数	FCD4N60TM	单位
$R_{\theta JC}$	结至外壳热阻最大值	2.5	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	结至环境热阻最大值	83	$^\circ\text{C}/\text{W}$

封装标识与订购信息

器件标识	器件	封装	卷尺寸	带宽	数量
FCD4N60	FCD4N60TM	D-PAK	380mm	16m	2500

电气特性 $T_C = 25^\circ\text{C}$ 除非另有说明。

符号	参数	测试条件	最小值	典型值	最大值	单位
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关断特性

BV_{DSS}	漏极-源极击穿电压	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}, T_C = 25^\circ\text{C}$	600	-	-	V
		$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}, T_C = 150^\circ\text{C}$	-	650	-	V
$\Delta BV_{DSS} / \Delta T_J$	击穿电压温度系数	$I_D = 1\text{ mA}$, 以 25°C 为参考	-	0.6	-	$\text{V}/^\circ\text{C}$
BV_{DS}	漏源极雪崩击穿电压	$V_{GS} = 0\text{ V}, I_D = 3.9\text{ A}$	-	700	-	V
I_{DSS}	零栅极电压漏极电流	$V_{DS} = 600\text{ V}, V_{GS} = 0\text{ V}$	-	-	1	μA
		$V_{DS} = 480\text{ V}, T_C = 125^\circ\text{C}$	-	-	10	μA
I_{GSS}	栅极-体漏电流	$V_{GS} = \pm 30\text{ V}, V_{DS} = 0\text{ V}$	-	-	± 100	nA

导通特性

$V_{GS(th)}$	栅极阈值电压	$V_{GS} = V_{DS}, I_D = 250\ \mu\text{A}$	3.0	-	5.0	V
$R_{DS(on)}$	漏极至源极静态导通电阻	$V_{GS} = 10\text{ V}, I_D = 2.0\text{ A}$	-	1.0	1.2	Ω
g_{FS}	正向跨导	$V_{DS} = 40\text{ V}, I_D = 2.0\text{ A}$	-	3.2	-	S

动态特性

C_{iss}	输入电容	$V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V}$ $f = 1.0\text{ MHz}$	-	415	540	pF
C_{oss}	输出电容		-	210	275	pF
C_{rss}	反向传输电容		-	19.5	-	pF
C_{oss}	输出电容	$V_{DS} = 480\text{ V}, V_{GS} = 0\text{ V}, f = 1.0\text{ MHz}$	-	12	16	pF
$C_{oss\text{eff}}$	有效输出电容	$V_{DS} = 0\text{ V}$ 至 $400\text{ V}, V_{GS} = 0\text{ V}$	-	32	-	pF

开关特性

$t_{d(on)}$	导通延迟时间	$V_{DD} = 300\text{ V}, I_D = 3.9\text{ A}$ $R_G = 25\ \Omega$	-	16	45	ns
t_r	开通上升时间		-	45	100	ns
$t_{d(off)}$	关断延迟时间		-	36	85	ns
t_f	关断下降时间		(说明 4)	-	30	70
$Q_{g(tot)}$	10 V 的栅极电荷总量	$V_{DS} = 480\text{ V}, I_D = 3.9\text{ A},$ $V_{GS} = 10\text{ V}$	-	12.8	16.6	nC
Q_{gs}	栅极-源极栅极电荷		-	2.4	-	nC
Q_{gd}	栅极-漏极“米勒”电荷		(说明 4)	-	7.1	-

漏极-源极二极管特性

I_S	漏极-源极二极管最大正向连续电流	-	-	3.9	A	
I_{SM}	漏极-源极二极管最大正向脉冲电流	-	-	11.7	A	
V_{SD}	漏极-源极二极管正向电压	$V_{GS} = 0\text{ V}, I_{SD} = 11\text{ A}$	-	-	1.4	V
t_{rr}	反向恢复时间	$V_{GS} = 0\text{ V}, I_{SD} = 11\text{ A}$ $di_F/dt = 100\text{ A}/\mu\text{s}$	-	277	-	ns
Q_{rr}	反向恢复电荷		-	2.07	-	μC

注意:

- 重复额定值: 脉冲宽度受限于最大结温
- $I_{AS} = 1.9\text{ A}, V_{DD} = 50\text{ V}, R_G = 25\ \Omega$, 开始 $T_J = 25^\circ\text{C}$
- $I_{SD} \leq 3.9\text{ A}, di/dt \leq 200\text{ A}/\mu\text{s}, V_{DD} \leq BV_{DSS}$, 开始 $T_J = 25^\circ\text{C}$
- 本质上独立于工作温度的典型特性

典型性能特征

图 1. 导通区域特性

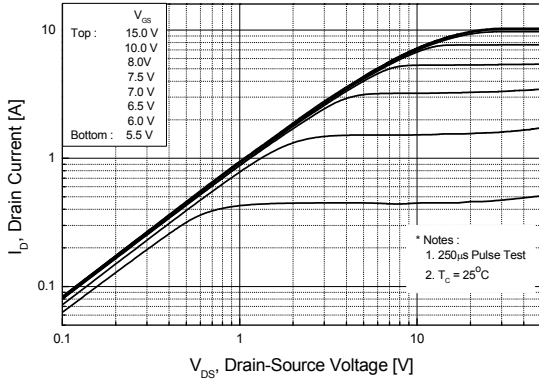


图 2. 传输特性

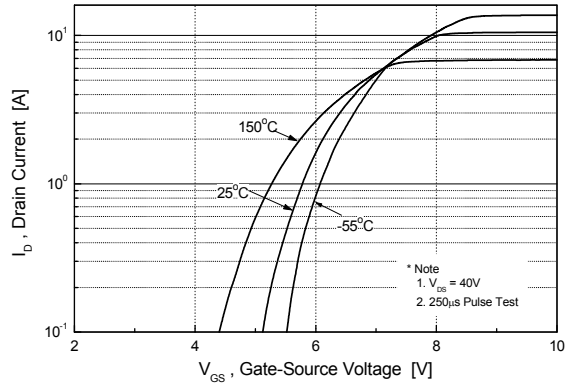


图 3. 导通电阻变化与漏极电流和栅极电压的关系

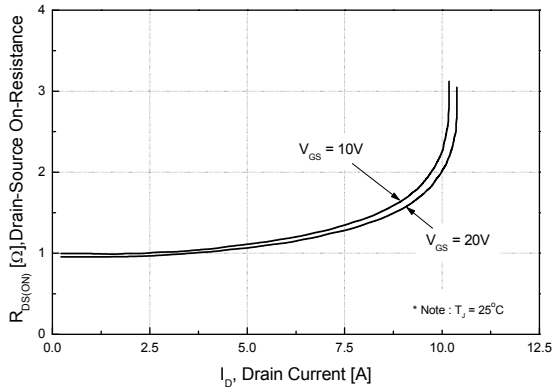


图 4. 体二极管正向电压变化与源电流和温度的关系

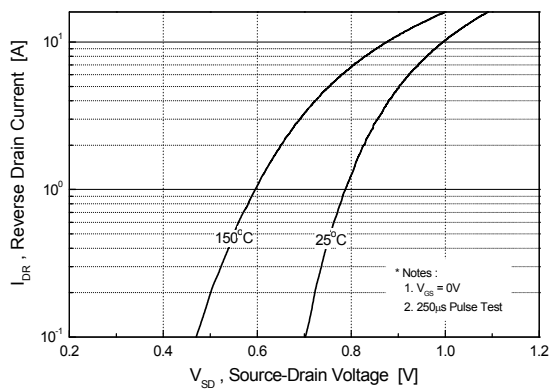


图 5. 电容特性

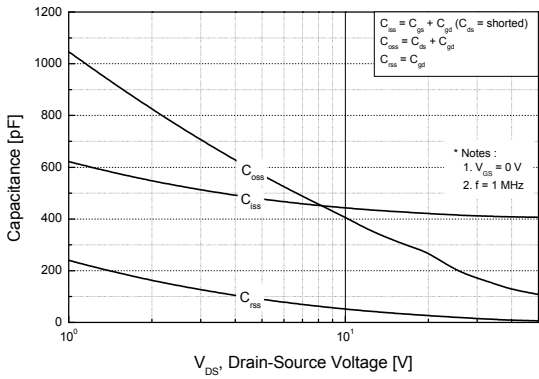
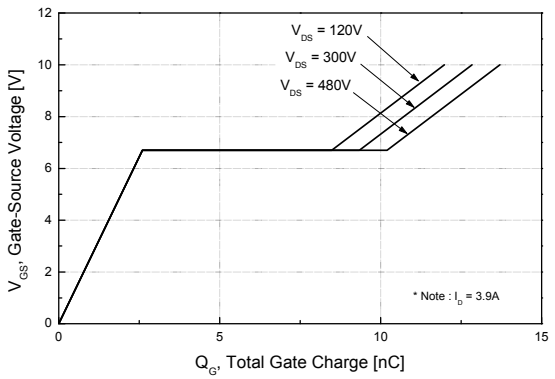


图 6. 栅极电荷特性



典型性能特性 (接上页)

图 7. 击穿电压变化与温度的关系

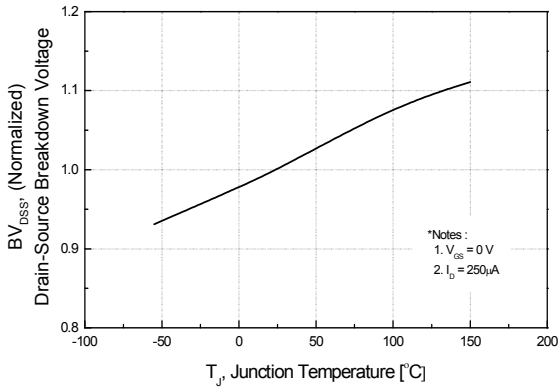


图 8. 导通电阻变化与温度的关系

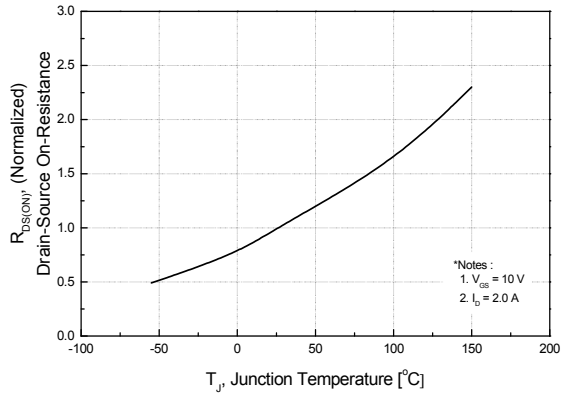


图 9. 最大安全工作区

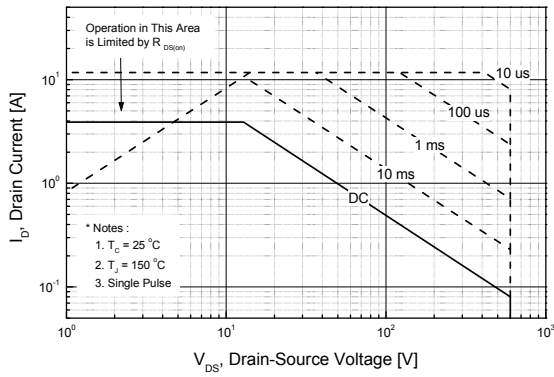


图 10. 最大漏极电流与壳温的关系

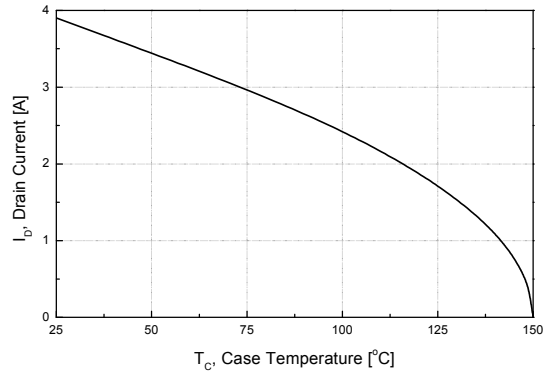


图 11. 瞬态热响应曲线

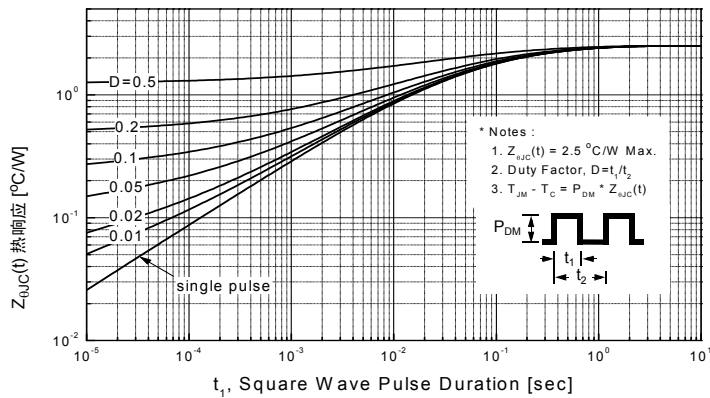


图 12. 栅极电荷测试电路与波形

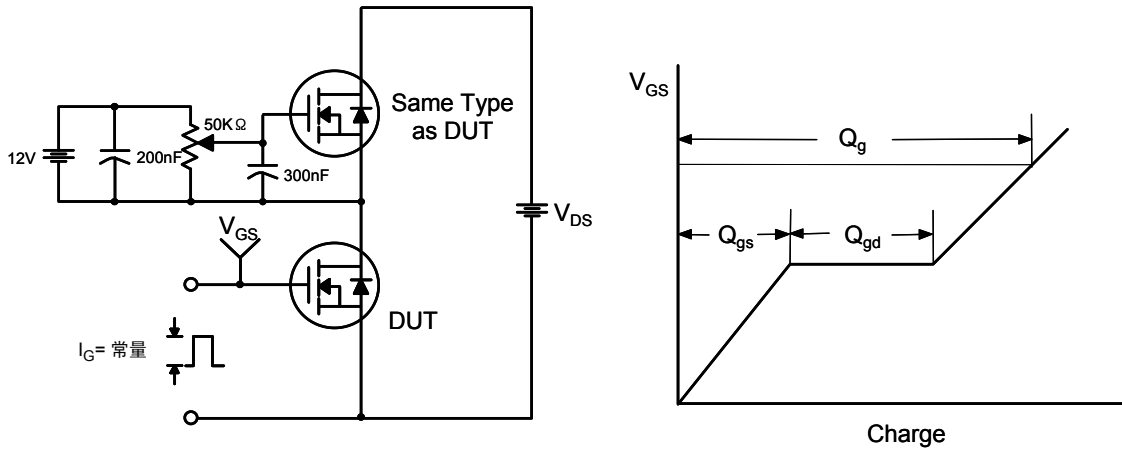


图 13. 阻性开关测试电路与波形



图 14. 非箝位感性开关测试电路与波形

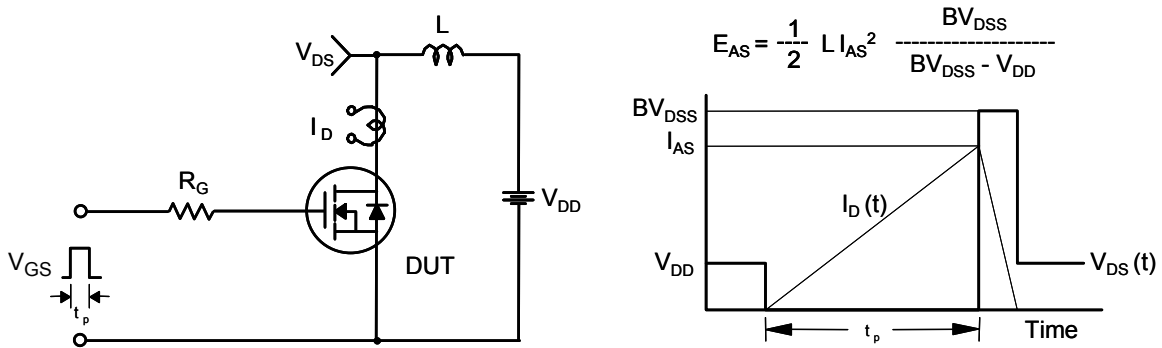
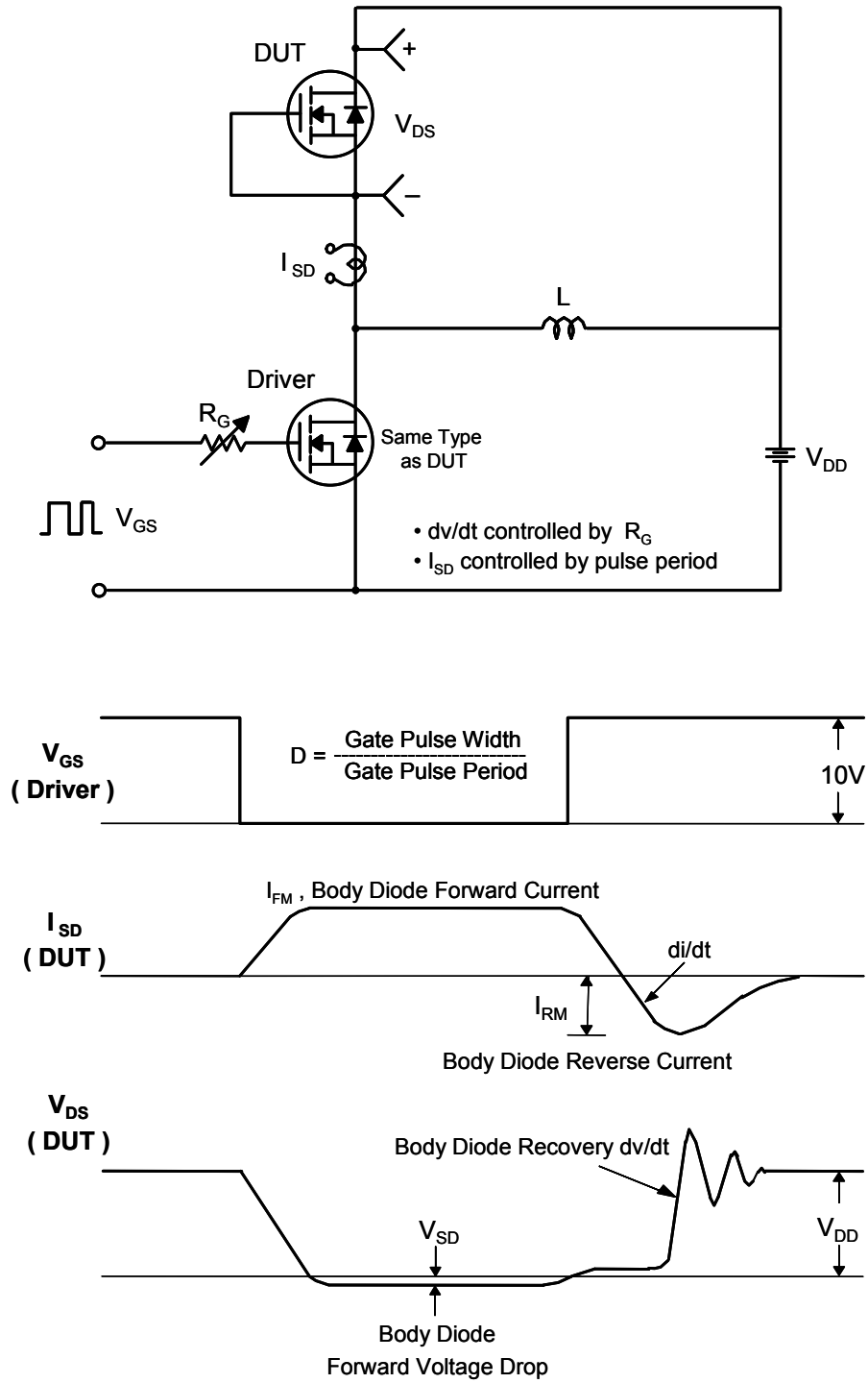
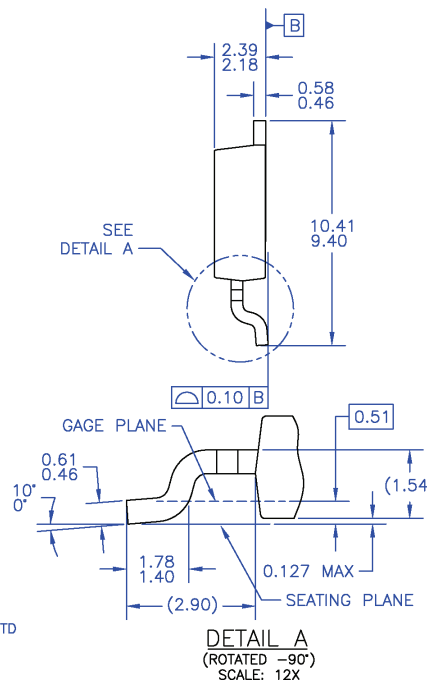
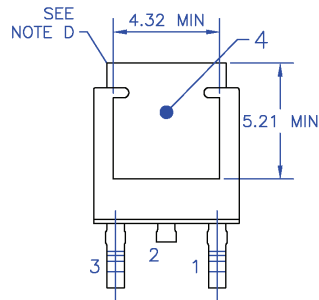
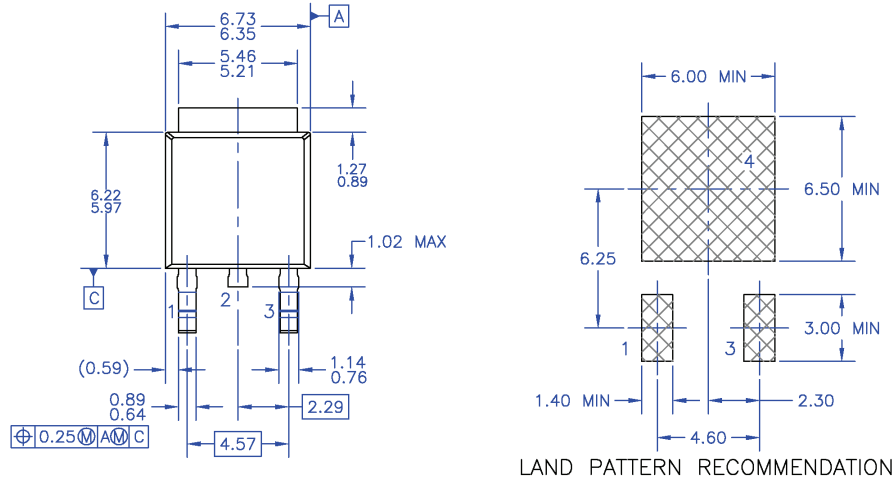


图 15. 峰值二极管恢复 dv/dt 测试电路与波形



机械尺寸

TO-252 3L (DPAK)



- NOTES: UNLESS OTHERWISE SPECIFIED
- A) THIS PACKAGE CONFORMS TO JEDEC, TO-252, ISSUE C, VARIATION AA.
 - B) ALL DIMENSIONS ARE IN MILLIMETERS.
 - C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
 - D) HEAT SINK TOP EDGE COULD BE IN CHAMFERED CORNERS OR EDGE PROTRUSION.
 - E) PRESENCE OF TRIMMED CENTER LEAD IS OPTIONAL.
 - F) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR EXTRUSIONS.
 - G) LAND PATTERN RECOMMENDATION IS BASED ON IPC7351A STD TO220P1003X238-3N.
 - H) DRAWING NUMBER AND REVISION: MKT-T0252A03REV8

图 16. TO252 (D-PAK), 模塑, 3 引脚, 选项 AA&AB

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No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
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