

MOSFET – N-Channel, SUPERFET[®] II

800 V, 58 A, 60 mΩ

FCH060N80

Description

SUPERFET II MOSFET is ON Semiconductor's brand-new high voltage super-junction (SJ) MOSFET family that is utilizing charge balance technology for outstanding low on-resistance and lower gate charge performance. This technology is tailored to minimize conduction loss, provide superior switching performance, dv/dt rate and higher avalanche energy. Consequently, SUPERFET II MOSFET is very suitable for the switching power applications such as PFC, server/telecom power, FPD TV power, ATX power and industrial power applications.

Features

- Typ. $R_{DS(on)}$ = 54 mΩ
- 850 V @ $T_J = 150^{\circ}\text{C}$
- Ultra Low Gate Charge (Typ. $Q_g = 270$ nC)
- Low E_{OSS} (Typ. 23 μJ @ 400 V)
- Low Effective Output Capacitance (Typ. $C_{oss(eff.)} = 981$ pF)
- 100% Avalanche Tested
- This Device is RoHS Compliant

Applications

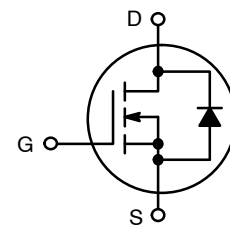
- AC-DC Power Supply
- LED Lighting



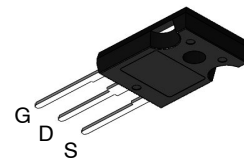
ON Semiconductor[®]

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V_{DSS}	$R_{DS(on)}$ MAX	I_D MAX
800 V	60 mΩ @ 10 V	58 A

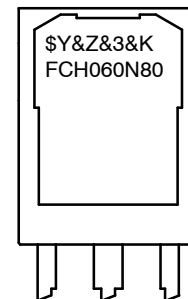


POWER MOSFET



TO-247-3LD
CASE 340CH

MARKING DIAGRAM



\$Y	= ON Semiconductor Logo
&Z	= Assembly Plant Code
&3	= Numeric Date Code
&K	= Lot Code
FCH060N80	= Specific Device Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

FCH060N80

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C, Unless otherwise noted)

Symbol	Parameter	Value	Unit
V _{DSS}	Drain to Source Voltage	800	V
V _{GSS}	Gate to Source Voltage	DC	±20
		AC (f > 1 Hz)	±30
I _D	Drain Current	Continuous (T _C = 25°C)	58
		Continuous (T _C = 100°C)	36.8
I _{DM}	Drain Current	Pulsed (Note 1)	174
E _{AS}	Single Pulsed Avalanche Energy (Note 2)	2317	mJ
I _{AS}	Avalanche Current (Note 1)	11.6	A
E _{AR}	Repetitive Avalanche Energy (Note 1)	50	mJ
dv/dt	MOSFET dv/dt	100	V/ns
	Peak Diode Recovery dv/dt (Note 3)	20	
P _D	Power Dissipation	(T _C = 25°C)	500
		Derate Above 25°C	4
T _J , T _{STG}	Operating and Storage Temperature Range	-55 to +150	°C
T _L	Maximum Lead Temperature for Soldering Purpose 1/8" from Case for 5 seconds	300	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Repetitive rating: pulse width limited by maximum junction temperature.

2. I_{AS} = 11.6 A, V_{DD} = 50 V, R_G = 25 Ω, starting T_J = 25°C.

3. I_{SD} ≤ 58 A, di/dt ≤ 200 A/μs, V_{DD} ≤ BV_{DSS}, starting T_J = 25°C.

THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Unit
R _{θJC}	Thermal Resistance, Junction to Case, Max.	0.25	°C/W
R _{θJA}	Thermal Resistance, Junction to Ambient, Max.	40	

PACKAGE MARKING AND ORDERING INFORMATION

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FCH060N80-F155	FCH060N80	TO-247-3LD	Tube	N/A	N/A	30 Units

FCH060N80

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
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OFF CHARACTERISTICS

BV_{DSS}	Drain to Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 1\text{ mA}, T_J = 25^\circ\text{C}$	800			V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 1\text{ mA}$, Referenced to 25°C		0.8		$\text{V}/^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 800\text{ V}, V_{GS} = 0\text{ V}$			25	μA
		$V_{DS} = 640\text{ V}, T_C = 125^\circ\text{C}$			250	
I_{GSS}	Gate to Body Leakage Current	$V_{GS} = \pm 20\text{ V}, V_{DS} = 0\text{ V}$			± 100	nA

ON CHARACTERISTICS

$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS} = V_{DS}, I_D = 5.8\text{ mA}$	2.5		4.5	V
$R_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\text{ V}, I_D = 29\text{ A}$		54	60	$\text{m}\Omega$
g_{FS}	Forward Transconductance	$V_{DS} = 20\text{ V}, I_D = 29\text{ A}$		68		S

DYNAMIC CHARACTERISTICS

C_{iss}	Input Capacitance	$V_{DS} = 100\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$		11040	14685	pF
C_{oss}	Output Capacitance			298	395	
C_{rSS}	Reverse Transfer Capacitance			10		
C_{oss}	Output Capacitance	$V_{DS} = 480\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$		147		pF
$C_{oss(eff.)}$	Effective Output Capacitance	$V_{DS} = 0\text{ V to } 480\text{ V}, V_{GS} = 0\text{ V}$		981		pF
$Q_{g(tot)}$	Total Gate Charge at 10 V	$V_{DS} = 640\text{ V}, I_D = 58\text{ A}, V_{GS} = 10\text{ V}$ (Note 4)		270	350	nC
Q_{gs}	Gate to Source Gate Charge			54		
Q_{gd}	Gate to Drain "Miller" Charge			100		
ESR	Equivalent Series Resistance	$f = 1\text{ MHz}$		0.78		Ω

SWITCHING CHARACTERISTICS

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 400\text{ V}, I_D = 58\text{ A}, V_{GS} = 10\text{ V}$ $R_g = 4.7\ \Omega$ (Note 4)		55	120	ns
t_r	Turn-On Rise Time			73	156	
$t_{d(off)}$	Turn-Off Delay Time			213	436	
t_f	Turn-Off Fall Time			72	154	

SOURCE-DRAIN DIODE CHARACTERISTICS

I_S	Maximum Continuous Drain to Source Diode Forward Current			58	A
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current			174	A
V_{SD}	Drain to Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_{SD} = 58\text{ A}$		1.2	V
t_{rr}	Reverse Recovery Time	$V_{GS} = 0\text{ V}, I_{SD} = 58\text{ A},$ $dI_F/dt = 100\text{ A}/\mu\text{s}$		850	ns
Q_{rr}	Reverse Recovery Charge			35	μC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Essentially independent of operating temperature typical characteristics.

TYPICAL PERFORMANCE CHARACTERISTICS

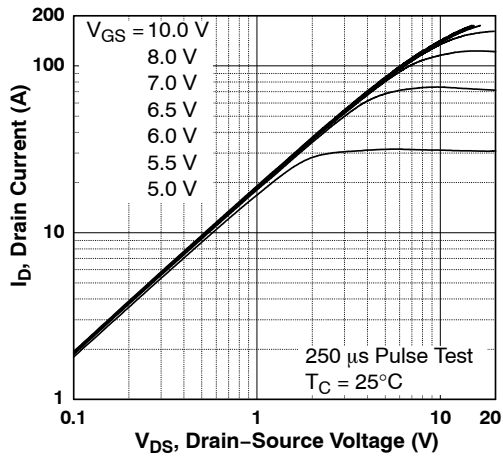


Figure 1. On-Region Characteristics

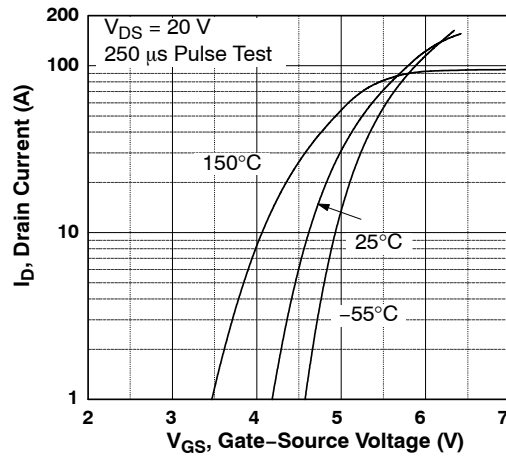


Figure 2. Transfer Characteristics

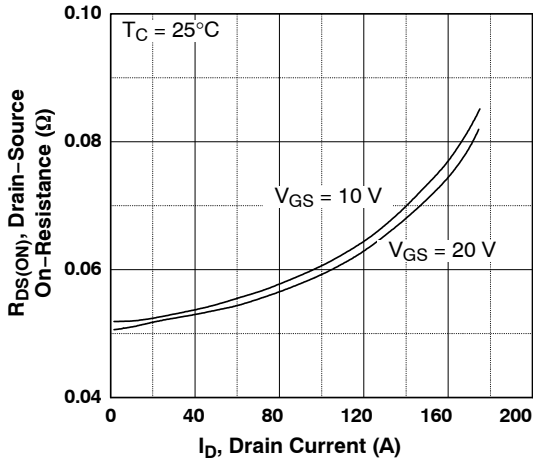


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

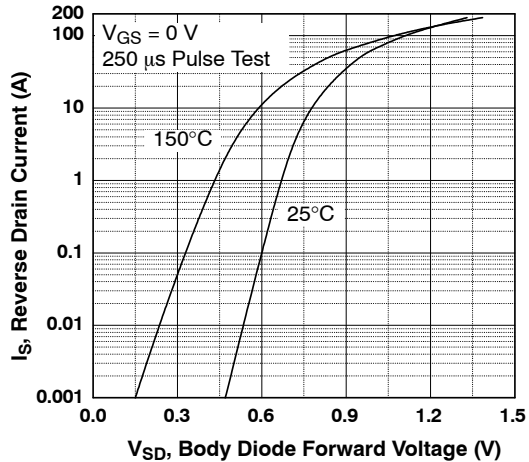


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

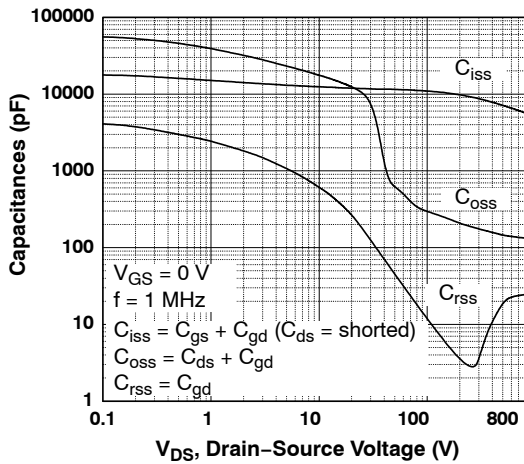


Figure 5. Capacitance Characteristics

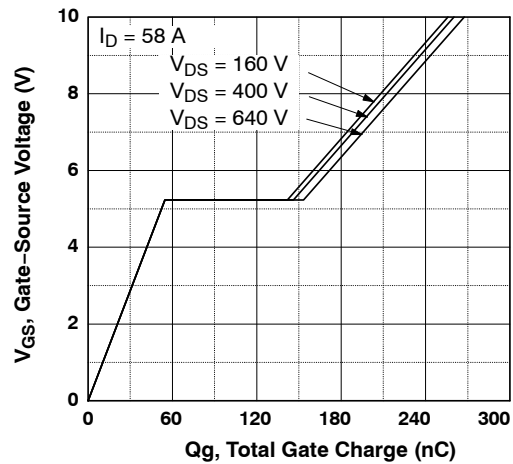


Figure 6. Gate Charge Characteristics

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

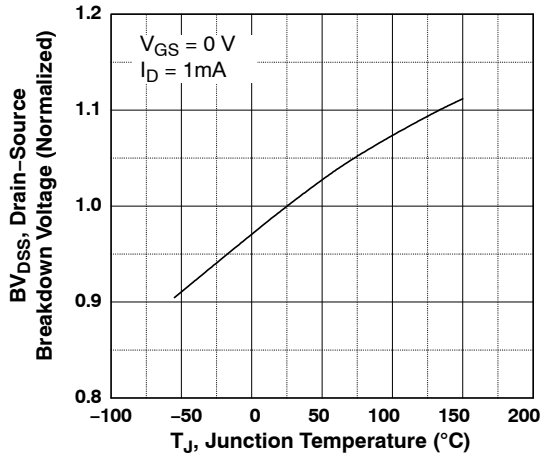


Figure 7. Breakdown Voltage Variation vs. Temperature

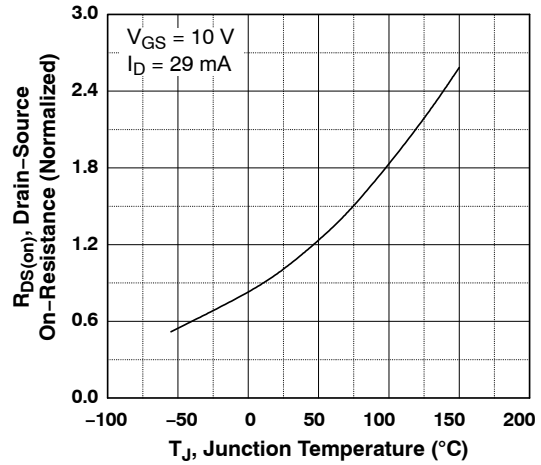


Figure 8. On-Resistance Variation vs. Temperature

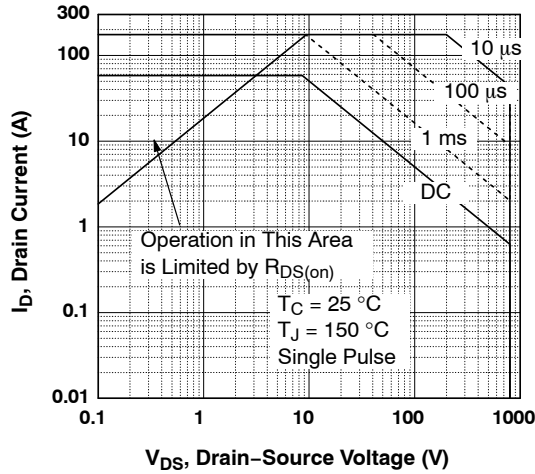


Figure 9. Maximum Safe Operating Area

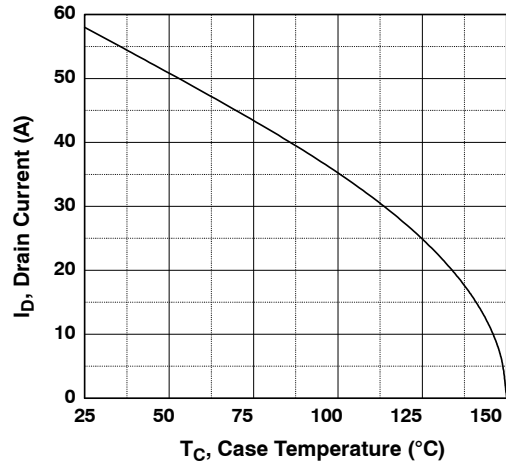


Figure 10. Maximum Drain Current vs. Case Temperature

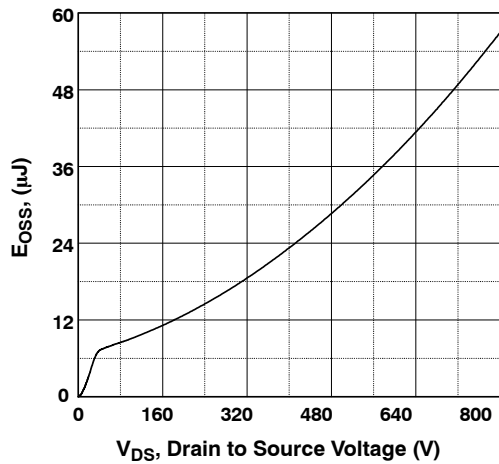


Figure 11. E_{OSS} vs. Drain to Source Voltage

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TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

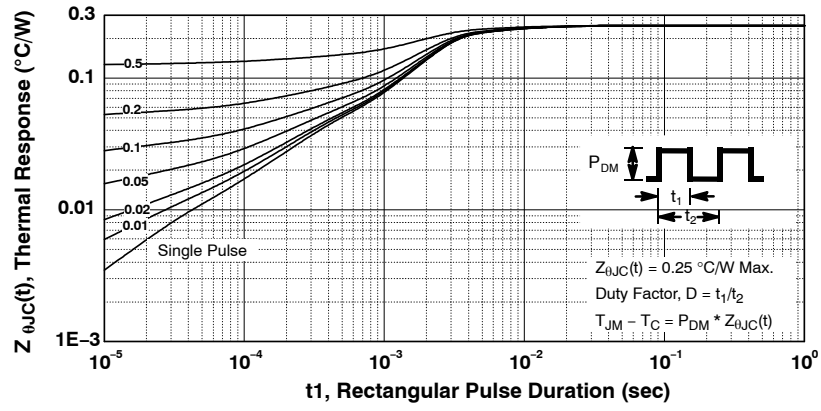


Figure 12. Transient Thermal Response Curve

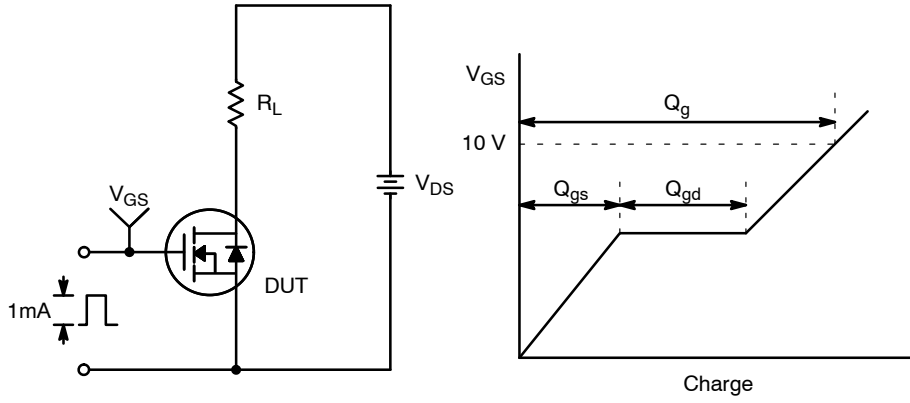


Figure 13. Gate Charge Test Circuit & Waveform

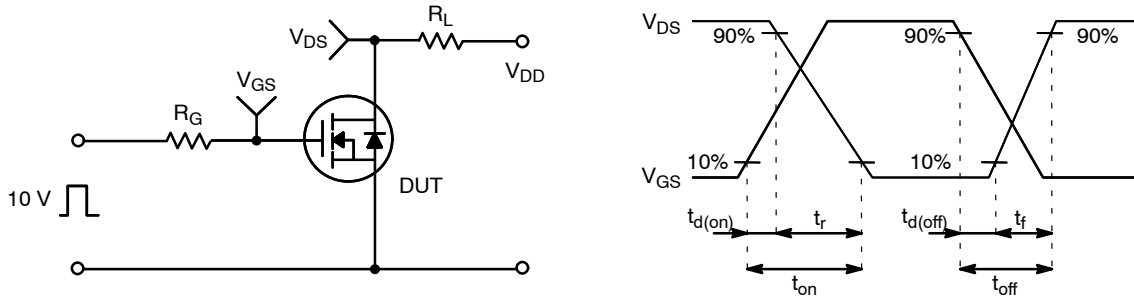


Figure 14. Resistive Switching Test Circuit & Waveforms

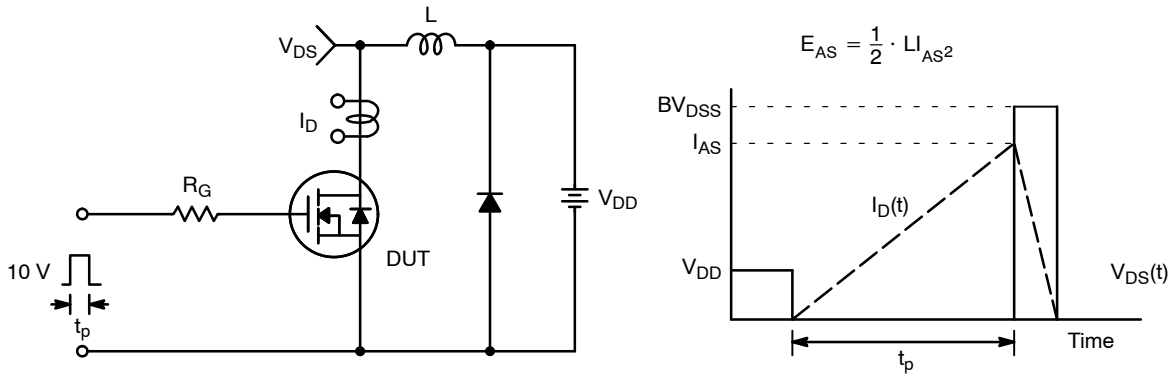


Figure 15. Unclamped Inductive Switching Test Circuit & Waveforms

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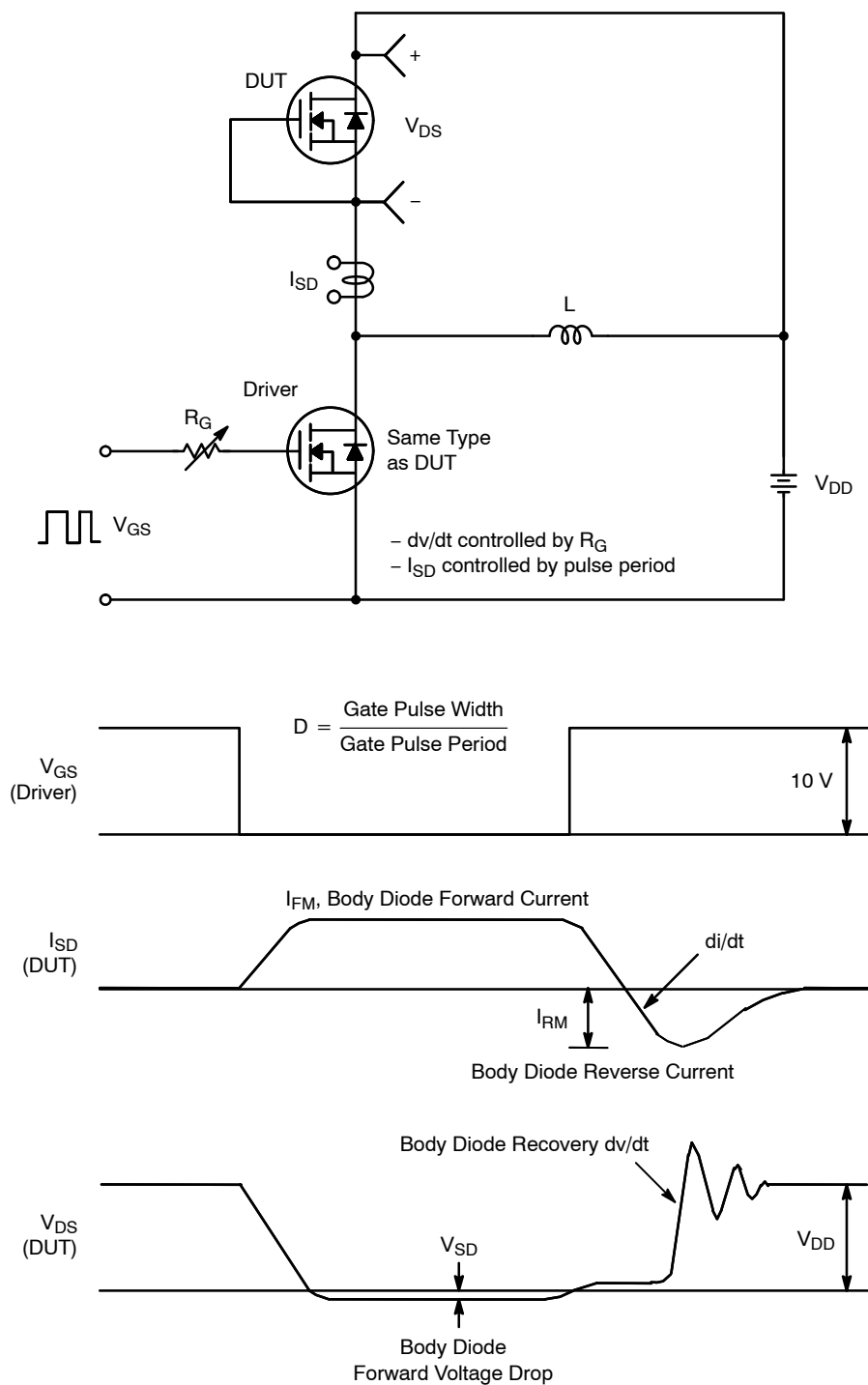


Figure 16. Peak Diode Recovery dv/dt Test Circuit & Waveforms

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MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

ON Semiconductor®



TO-247-3LD
CASE 340CH
ISSUE A

DATE 09 OCT 2019



NOTES: UNLESS OTHERWISE SPECIFIED.

- A. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
- B. ALL DIMENSIONS ARE IN MILLIMETERS.
- C. DRAWING CONFORMS TO ASME Y14.5 - 2009.
- D. DIMENSION A1 TO BE MEASURED IN THE REGION DEFINED BY L1.
- E. LEAD FINISH IS UNCONTROLLED IN THE REGION DEFINED BY L1.

GENERIC MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
G = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

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