

MOSFET – N-Channel, SUPERFET® II

800 V, 46 A, 85 mΩ

FCH085N80

Description

SuperFET II MOSFET is ON Semiconductor's brand-new high voltage super-junction (SJ) MOSFET family that is utilizing charge balance technology for outstanding low on-resistance and lower gate charge performance. This technology is tailored to minimize conduction loss, provide superior switching performance, dv/dt rate and higher avalanche energy. Consequently, SuperFET II MOSFET is very suitable for the switching power applications such as PFC, server/telecom power, FPD TV power, ATX power and industrial power applications.

Features

- Typ. $R_{DS(on)}$ = 67 mΩ
- 850 V @ $T_J = 150^\circ\text{C}$
- Ultra Low Gate Charge (Typ. $Q_g = 196$ nC)
- Low E_{OSS} (Typ. 18 μJ @ 400 V)
- Low Effective Output Capacitance (Typ. $C_{oss(eff.)} = 568$ pF)
- 100% Avalanche Tested
- These Devices are Pb-Free and are RoHS Compliant

Applications

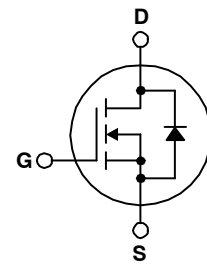
- AC-DC Power Supply
- LED Lighting



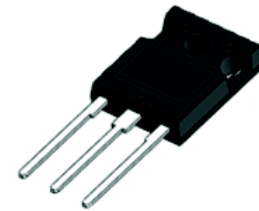
ON Semiconductor®

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V_{DS}	$R_{DS(on)}$ MAX	I_D MAX
800 V	85 mΩ @ 10 V	46 A

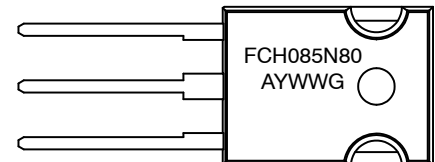


N-CHANNEL MOSFET



TO-247-3LD
CASE 340CH

MARKING DIAGRAM



FCH085N80 = Specific Device Code
 A = Assembly Location
 Y = Year
 WW = Work Week
 G = Pb-Free Package

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

FCH085N80

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Symbol	Parameter	Value	Unit
V _{DSS}	Drain to Source Voltage	800	V
V _{GSS}	Gate to Source Voltage	- DC	±20
		- AC (f > 1 Hz)	±30
I _D	Drain Current:	- Continuous (T _C = 25°C)	46
		- Continuous (T _C = 100°C)	29
I _{DM}	Drain Current:	- Pulsed (Note 1)	138
E _{AS}	Single Pulsed Avalanche Energy (Note 2)	1701	mJ
I _{AS}	Avalanche Current (Note 2)	9.2	A
E _{AR}	Repetitive Avalanche Energy (Note 1)	4.4	mJ
dv/dt	MOSFET dv/dt	100	V/ns
	Peak Diode Recovery dv/dt (Note 3)	20	
P _D	Power Dissipation	(T _C = 25°C)	446
		Derate Above 25°C	3.5
T _J , T _{STG}	Operating and Storage Temperature Range	-55 to + 150	°C
T _L	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 seconds	300	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Repetitive rating: pulse-width limited by maximum junction temperature.
2. I_{AS} = 9.2 A, V_{DD} = 50 V, R_G = 25 Ω, starting T_J = 25 °C.
3. I_{SD} ≤ 46 A, di/dt ≤ 200 A/μs, V_{DD} ≤ BV_{DSS}, starting T_J = 25 °C.

PACKAGE MARKING AND ORDERING INFORMATION

Part Number	Top Marking	Package	Packing Method	Reel Size	Tape Width	Quantity
FCH085N80-F155	FCH085N80	TO-247 G03	Tube	N/A	N/A	30 Units

THERMAL CHARACTERISTICS

Symbol	Parameter	FCH085N80-F155	Unit
R _{θJC}	Thermal Resistance, Junction to Case, Max.	0.28	°C/W
R _{θJA}	Thermal Resistance, Junction to Ambient, Max.	40.0	

FCH085N80

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
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OFF CHARACTERISTICS

BV _{DSS}	Drain to Source Breakdown Voltage	V _{GS} = 0 V, I _D = 1 mA, T _J = 25°C	800	–	–	V
ΔBV _{DSS} /ΔT _J	Breakdown Voltage Temperature Coefficient	I _D = 1 mA, Referenced to 25°C	–	0.8	–	V/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 80 V, V _{GS} = 0 V	–	–	25	μA
		V _{DS} = 640 V, V _{GS} = 0 V, T _C = 125 °C	–	–	250	
I _{GSS}	Gate to Body Leakage Current	V _{GS} = ±20 V, V _{DS} = 0 V	–	–	±100	nA

ON CHARACTERISTICS

V _{GS(th)}	Gate Threshold Voltage	V _{GS} = V _{DS} , I _D = 4.6 mA	2.5	–	4.5	V
R _{DS(on)}	Static Drain to Source On Resistance	V _{GS} = 10 V, I _D = 23 A	–	67	85	mΩ
g _{FS}	Forward Transconductance	V _{DS} = 20 V, I _D = 23 A	–	55	–	S

DYNAMIC CHARACTERISTICS

C _{iss}	Input Capacitance	V _{DS} = 100 V, V _{GS} = 0 V, f = 1 MHz	–	8140	10825	pF
C _{oss}	Output Capacitance		–	255	340	pF
C _{rss}	Reverse Transfer Capacitance		–	10	–	pF
C _{oss}	Output Capacitance	V _{DS} = 480 V, V _{GS} = 0 V, f = 1 MHz	–	1000	–	pF
C _{oss(eff.)}	Effective Output Capacitance	V _{DS} = 0 V to 480 V, V _{GS} = 0 V	–	728	–	pF
Q _{g(tot)}	Total Gate Charge at 10 V	V _{DS} = 640 V, I _D = 46 A, V _{GS} = 10 V (Note 4)	–	196	255	nC
Q _{gs}	Gate to Source Gate Charge		–	40	–	nC
Q _{gd}	Gate to Drain “Miller” Charge		–	72	–	nC
ESR	Equivalent Series Resistance	f = 1 MHz	–	0.8	–	Ω

SWITCHING CHARACTERISTICS

t _{d(on)}	Turn-On Delay Time	V _{DD} = 400 V, I _D = 46 A, V _{GS} = 10 V, R _g = 4.7 Ω (Note 4)	–	45	100	ns
t _r	Turn-On Rise Time		–	55	120	ns
t _{d(off)}	Turn-Off Delay Time		–	160	330	ns
t _f	Turn-Off Fall Time		–	35	80	ns

DRAIN-SOURCE DIODE CHARACTERISTICS

I _S	Maximum Continuous Source to Drain Diode Forward Current	–	–	46	A	
I _{SM}	Maximum Pulsed Drain to Source Diode Forward Current	–	–	138	A	
V _{SD}	Drain to Source Diode Forward Voltage	V _{GS} = 0 V, I _{SD} = 46 A	–	–	1.2	V
t _{rr}	Reverse Recovery Time	V _{GS} = 0 V, I _{SD} = 46 A, di _F /dt = 100 A/μs	–	800	–	ns
Q _{rr}	Reverse Recovery Charge		–	32	–	μC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Essentially independent of operating temperature typical characteristics.

TYPICAL CHARACTERISTICS

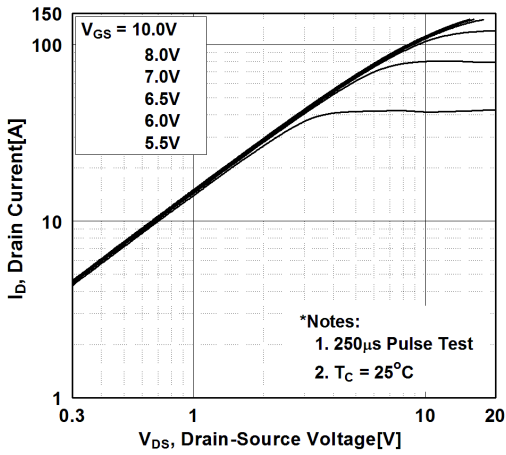


Figure 1. On-Region Characteristics

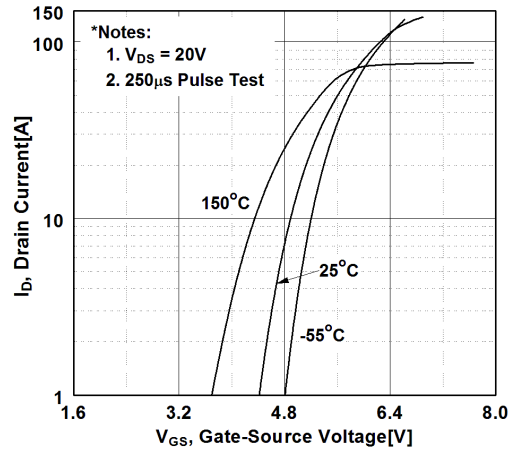


Figure 2. Transfer Characteristics

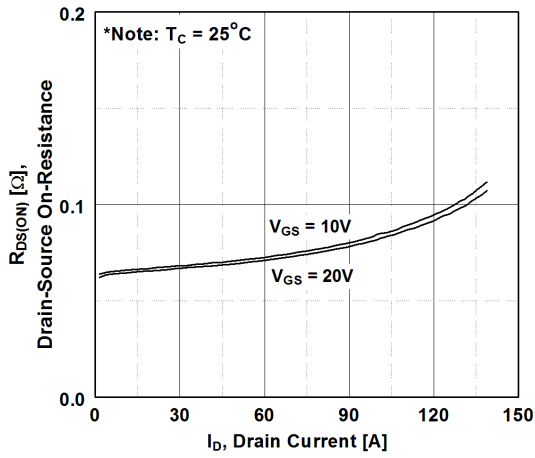


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

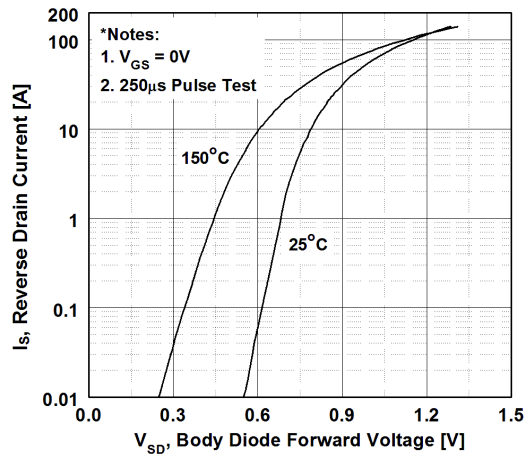


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

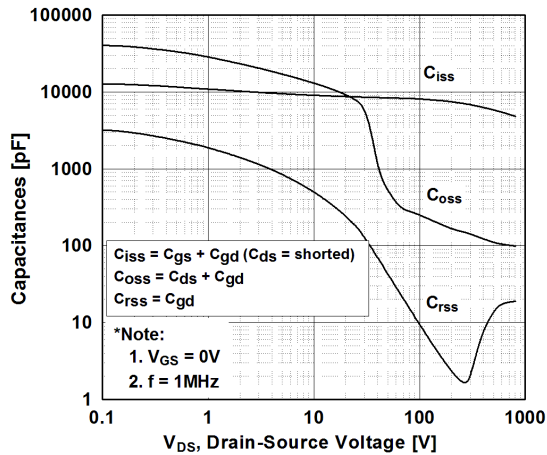


Figure 5. Capacitance Characteristics

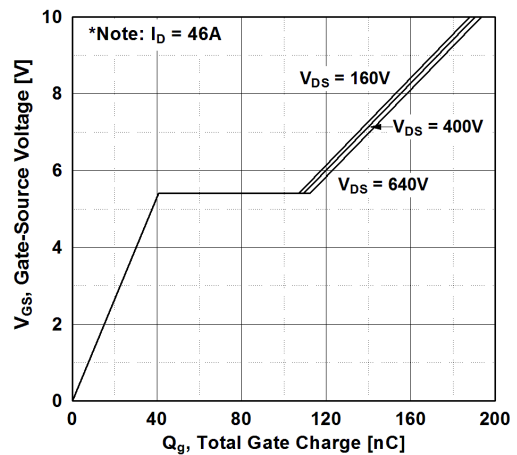


Figure 6. Gate Charge Characteristics

TYPICAL CHARACTERISTICS

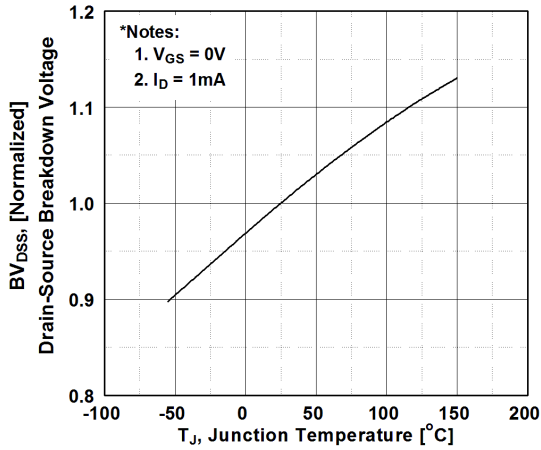


Figure 7. Breakdown Voltage Variation vs. Temperature

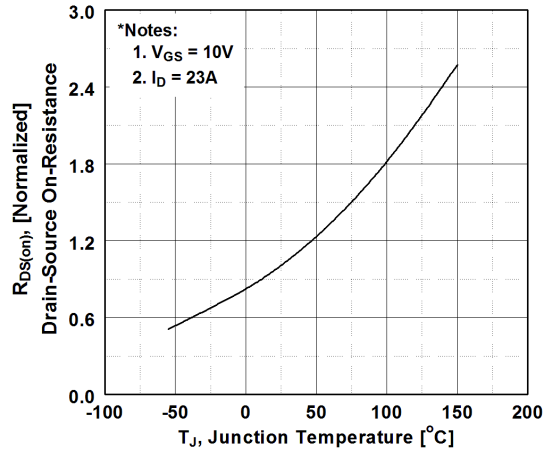


Figure 8. On-Resistance Variation vs. Temperature

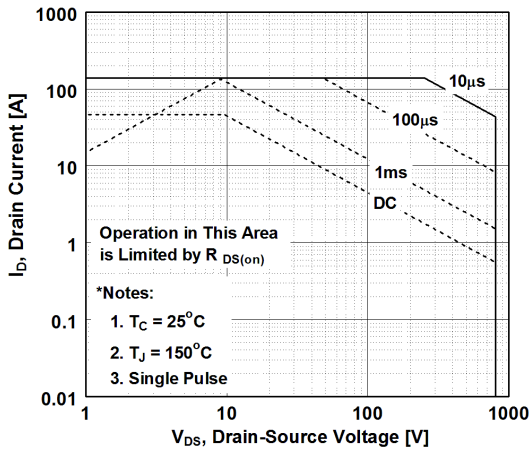


Figure 9. Maximum Safe Operating Area

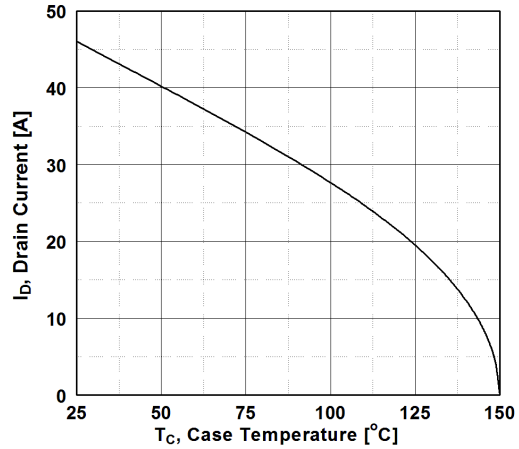


Figure 10. Maximum Drain Current vs. Case Temperature

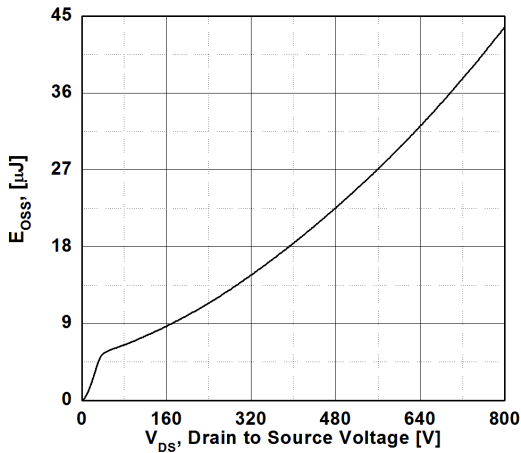


Figure 11. E_{oss} vs. Drain to Source Voltage

TYPICAL CHARACTERISTICS

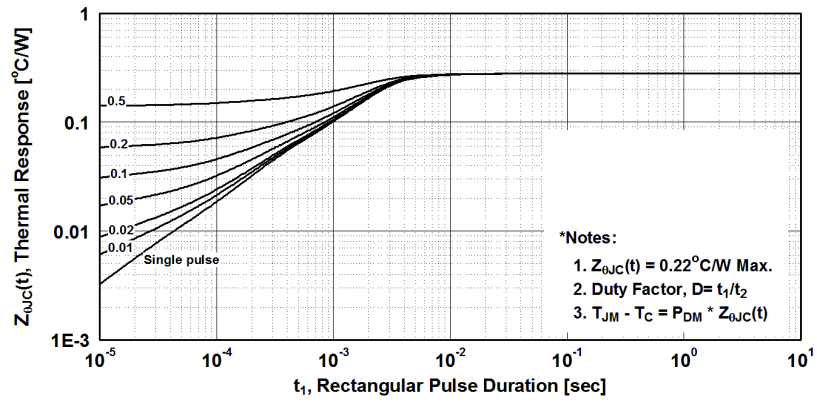


Figure 12. Transient Thermal Response Curve



Figure 13. Gate Charge Test Circuit & Waveform



Figure 14. Resistive Switching Test Circuit & Waveforms



Figure 15. Unclamped Inductive Switching Test Circuit & Waveforms

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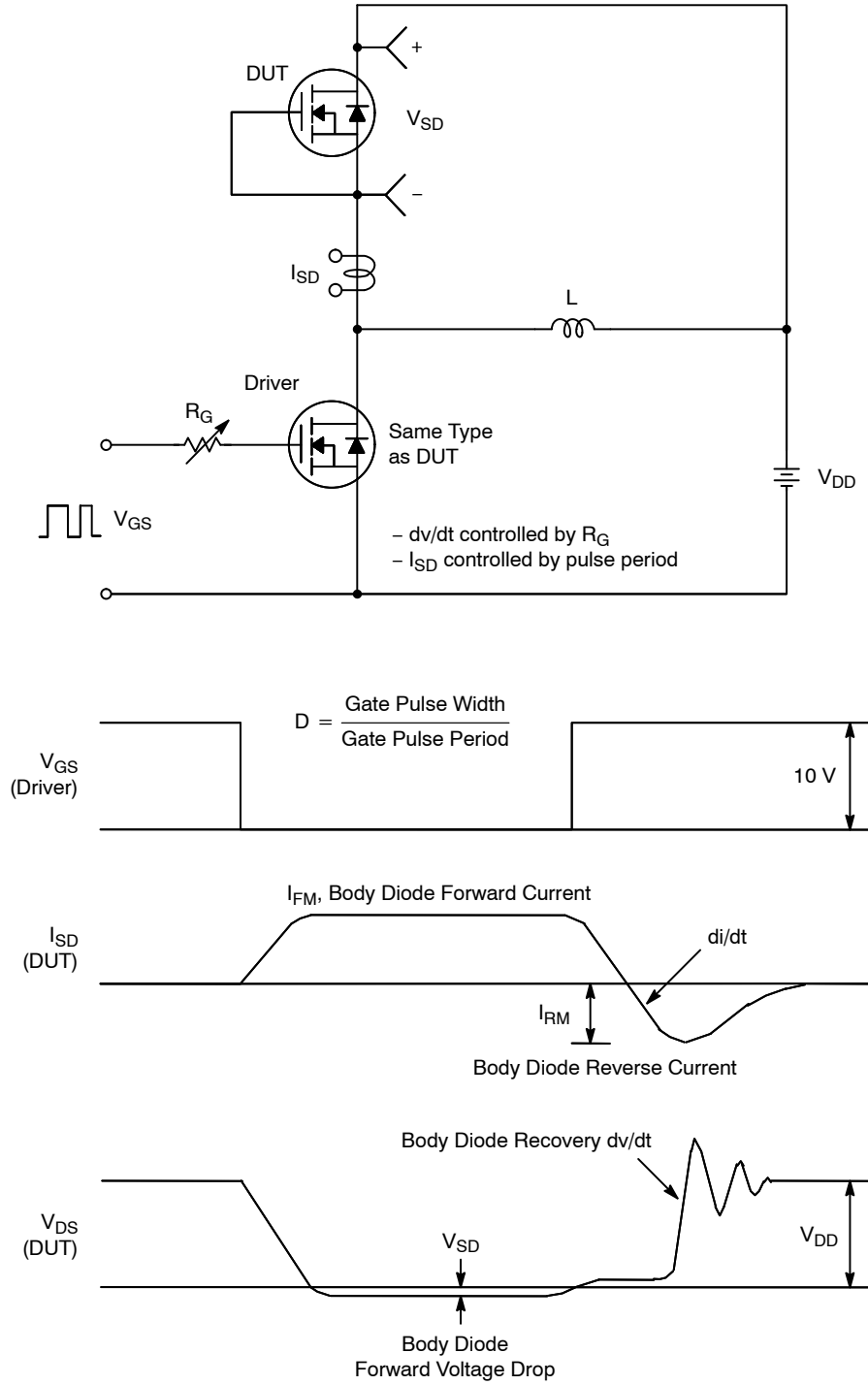


Figure 16. Peak Diode Recovery dv/dt Test Circuit & Waveforms

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MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

ON Semiconductor®



TO-247-3LD
CASE 340CH
ISSUE A

DATE 09 OCT 2019



NOTES: UNLESS OTHERWISE SPECIFIED.

- A. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
- B. ALL DIMENSIONS ARE IN MILLIMETERS.
- C. DRAWING CONFORMS TO ASME Y14.5 - 2009.
- D. DIMENSION A1 TO BE MEASURED IN THE REGION DEFINED BY L1.
- E. LEAD FINISH IS UNCONTROLLED IN THE REGION DEFINED BY L1.

GENERIC MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
G = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	4.58	4.70	4.82
A1	2.29	2.475	2.66
A2	1.40	1.50	1.60
D	20.32	20.57	20.82
E	15.37	15.62	15.87
E2	4.96	5.08	5.20
e	~	5.56	~
L	19.75	20.00	20.25
L1	3.69	3.81	3.93
∅P	3.51	3.58	3.65
Q	5.34	5.46	5.58
S	5.34	5.46	5.58
b	1.17	1.26	1.35
b2	1.53	1.65	1.77
b4	2.42	2.54	2.66
c	0.51	0.61	0.71
D1	13.08	~	~
D2	0.51	0.93	1.35
E1	12.81	~	~
∅P1	6.61	6.73	6.85

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