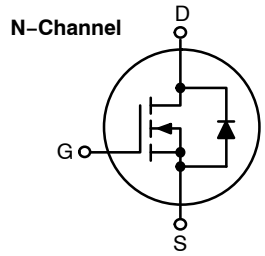
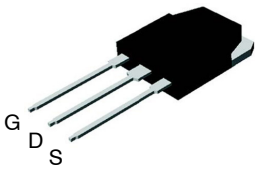
MOSFET – N-Channel, UniFET™, FRFET®

500 V, 24 A, 200 mΩ

FDA24N50F

V_{DS}	$R_{DS(ON)}$ MAX	I_D MAX
500 V	200 mΩ @ 10 V	24 A





TO−3P−3LD / EIAJ SC−65, ISOLATED CASE 340BZ

Description

UniFET MOSFET is **onsemi**'s high voltage MOSFET family based on planar stripe and DMOS technology. This MOSFET is tailored to reduce on−state resistance, and to provide better switching performance and higher avalanche energy strength. The body diode's reverse recovery performance of UniFET FRFET MOSFET has been enhanced by lifetime control. Its trr is less than 100 ns and the reverse dv/dt immunity is 15 V/ns while normal planar MOSFETs have over 200 ns and 4.5 V/ns respectively. Therefore, it can remove additional component and improve system reliability in certain applications in which the performance of MOSFET's body diode is significant. This device family is suitable for switching power converter applications such as power factor correction (PFC), flat panel display (FPD) TV power, ATX and electronic lamp ballasts.

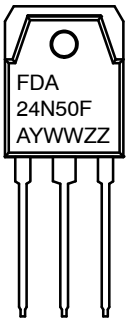
Features

- $R_{DS(on)}$ = 166 mΩ (Typ.) @ V_{GS} = 10 V, I_D = 12 A
- Low Gate Charge (Typ. 65 nC)
- Low C_{rss} (Typ. 32 pF)
- 100% Avalanche Tested
- Improved dv/dt Capability
- RoHS Compliant

Applications

- PDP TV
- Uninterruptible Power Supply
- AC−DC Power Supply

MARKING DIAGRAM



FDA24N50F	= Specific Device Code
A	= Assembly Site
YWW	= Date Code (Year & Work Week)
ZZ	= Assembly Lot Number

ORDERING INFORMATION

Device	Package	Shipping
FDA24N50F	TO−3P−3LD	450 Units / Tube

MOSFET MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Symbol	Parameter		Value	Unit
V_{DSS}	Drain to Source Voltage		500	V
V_{GSS}	Gate to Source Voltage		±30	V
I_D	Drain Current	– Continuous (T_C = 25°C)	24	A
		– Continuous (T_C = 100°C)	14	
I_{DM}		– Pulsed (Note 1)	96	
E_{AS}	Single Pulsed Avalanche Energy (Note 2)		1872	mJ
I_{AR}	Avalanche Current (Note 1)		24	A
E_{AR}	Repetitive Avalanche Energy (Note 1)		27	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)		20	V/ns
P_D	Power Dissipation	T_C = 25°C	270	W
		–Derate above = 25°C	2.2	W/°C
T_J, T_{STG}	Operating and Storage Temperature Range		–55 to +150	°C
T_L	Maximum Lead Temperature for Soldering, 1/8” from Case for 5 Seconds		300	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Repetitive rating: pulse−width limited by maximum junction temperature.
2. L = 6.5 mH, I_{AS} = 24 A, V_{DD} = 50 V, R_G = 25 Ω, starting T_J = 25°C.
3. I_{SD} ≤ 24 A, di/dt ≤ 200 A/μs, V_{DD} ≤ BV_{DSS}, starting T_J = 25°C.

THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	0.46	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max.	40	

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 250 μA, V_{GS} = 0 V, T_J = 25°C	500	–	–	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, referenced to 25°C	–	0.6	–	V/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 500 V, V_{GS} = 0 V	–	–	1	μA
		V_{DS} = 400 V, T_C = 125°C	–	–	10	
I_{GSS}	Gate to Body Leakage Current	V_{GS} = ±30 V, V_{DS} = 0 V	–	–	±100	nA
ON CHARACTERISTICS						
$V_{GS(th)}$	Gate Threshold Voltage	V_{GS} = V_{DS}, I_D = 250 μA	3.0	–	5.0	V
$R_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = 10 V, I_D = 12 A	–	0.166	0.200	Ω
g_{FS}	Forward Transconductance	V_{DS} = 20 V, I_D = 12 A	–	30	–	S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = 25 V, V_{GS} = 0 V, f = 1 MHz	–	3240	4310	pF
C_{oss}	Output Capacitance		–	450	600	pF
C_{rss}	Reverse Transfer Capacitance		–	32	48	pF
$Q_{g(tot)}$	Total Gate Charge at 10 V	V_{DS} = 400 V, I_D = 24 A, V_{GS} = 10 V (Note 4)	–	65	85	nC
Q_{gs}	Gate to Source Gate Charge		–	18	–	nC
Q_{gd}	Gate to Drain “Miller” Charge		–	26	–	nC
SWITCHING CHARACTERISTICS						
$t_{d(on)}$	Turn−On Delay Time	V_{DD} = 250 V, I_D = 24 A, V_{GS} = 10 V, R_G = 25 Ω (Note 4)	–	49	108	ns
t_r	Turn−On Rise Time		–	105	220	ns
$t_{d(off)}$	Turn−Off Delay Time		–	165	340	ns
t_f	Turn−Off Fall Time		–	87	185	ns
DRAIN−SOURCE DIODE CHARACTERISTICS						
I_S	Maximum Continuous Drain to Source Diode Forward Current		–	–	24	A
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current		–	–	96	A
V_{SD}	Drain to Source Diode Forward Voltage	V_{GS} = 0 V, I_{SD} = 24 A	–	–	1.4	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0 V, I_{SD} = 24 A, dI_F/dt = 100 A/μs	–	264	–	ns
Q_{rr}	Reverse Recovery Charge		–	1.4	–	μC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Essentially independent of operating temperature typical characteristics.

TYPICAL PERFORMANCE CHARACTERISTICS

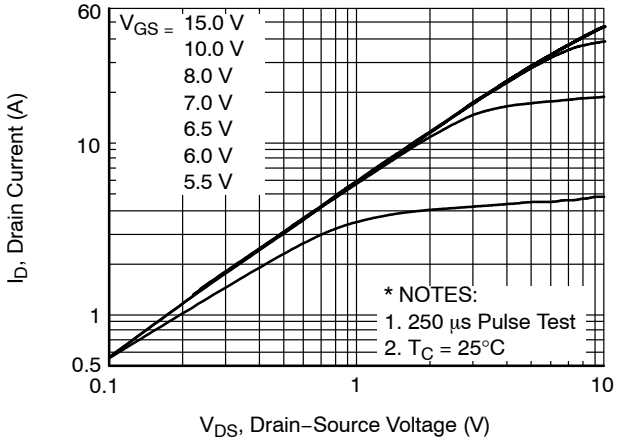


Figure 1. On−Region Characteristics

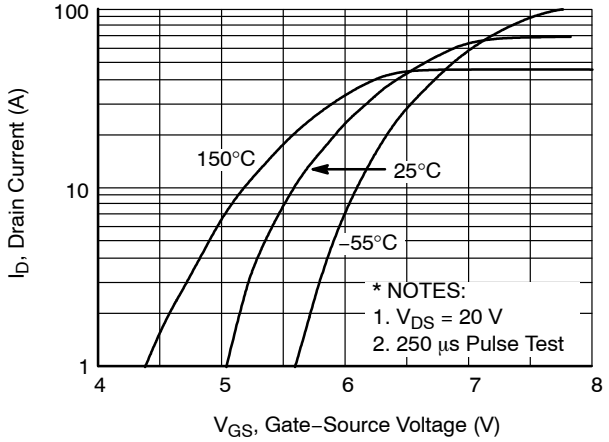


Figure 2. Transfer Characteristics

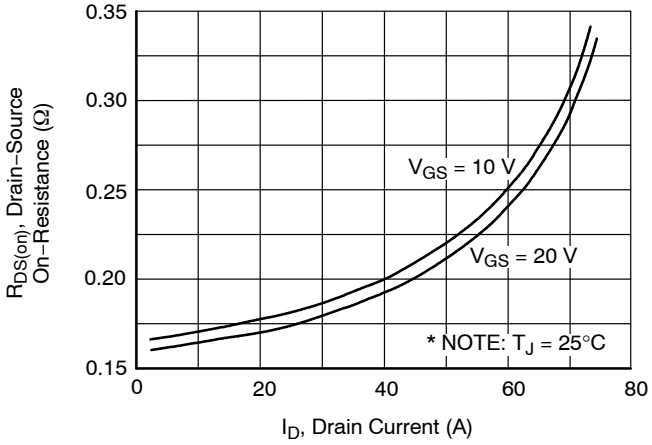


Figure 3. On−Resistance Variation vs. Drain Current and Gate Voltage

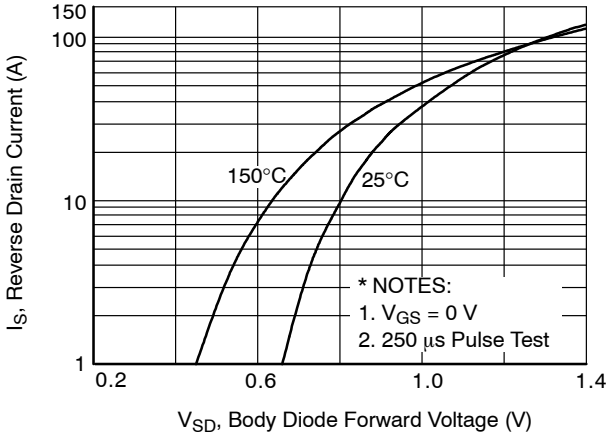


Figure 4. Body Diode Forward Voltage Variation vs. Source Current And Temperature

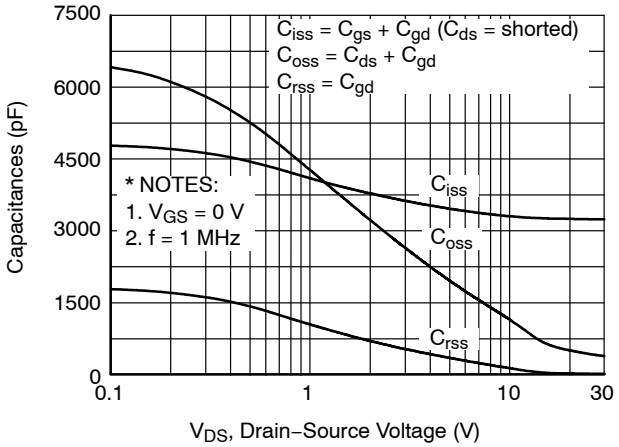


Figure 5. Capacitance Characteristics

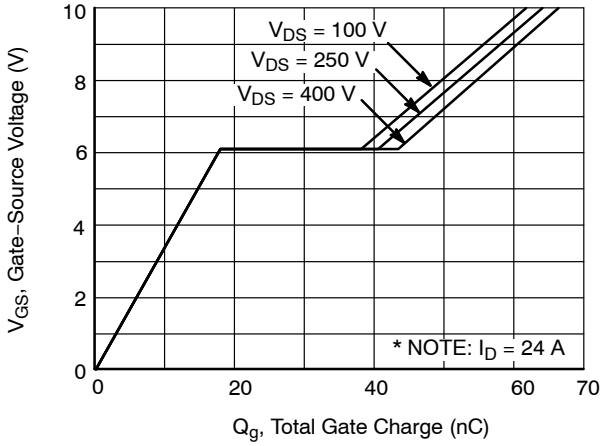


Figure 6. Gate Charge Characteristics

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

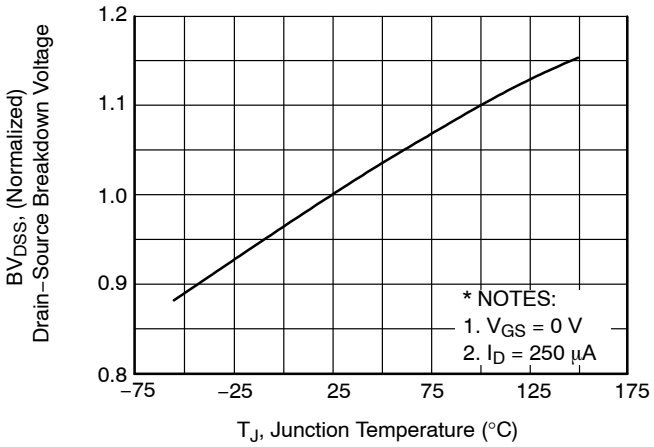


Figure 7. Breakdown Voltage Variation vs. Temperature

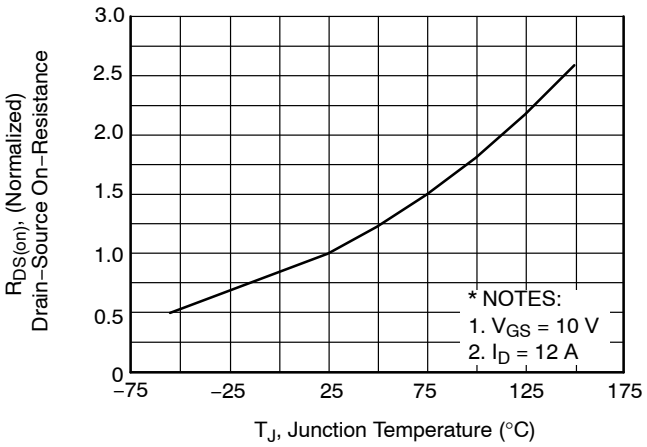


Figure 8. On−Resistance Variation vs. Temperature

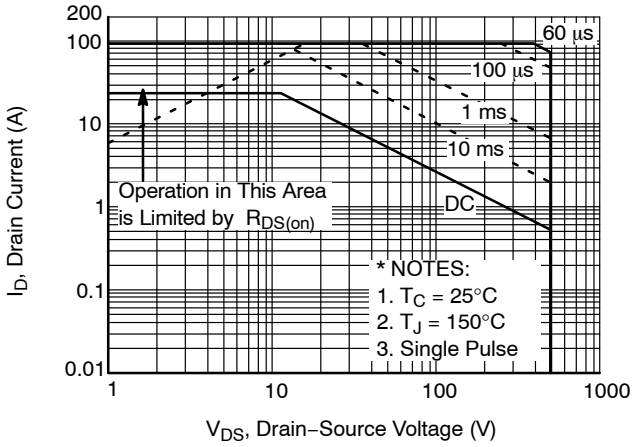


Figure 9. Maximum Safe Operating Area

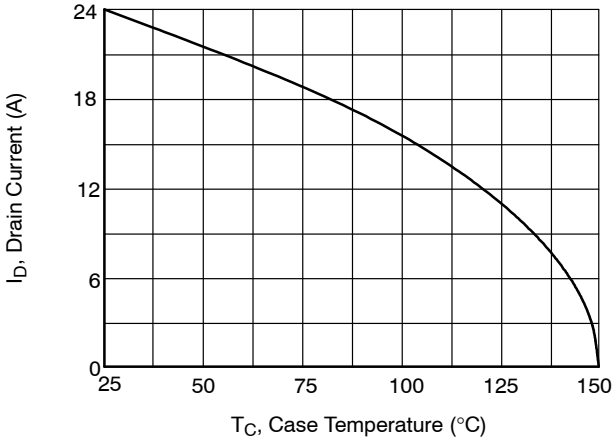


Figure 10. Maximum Drain Current vs. Case Temperature

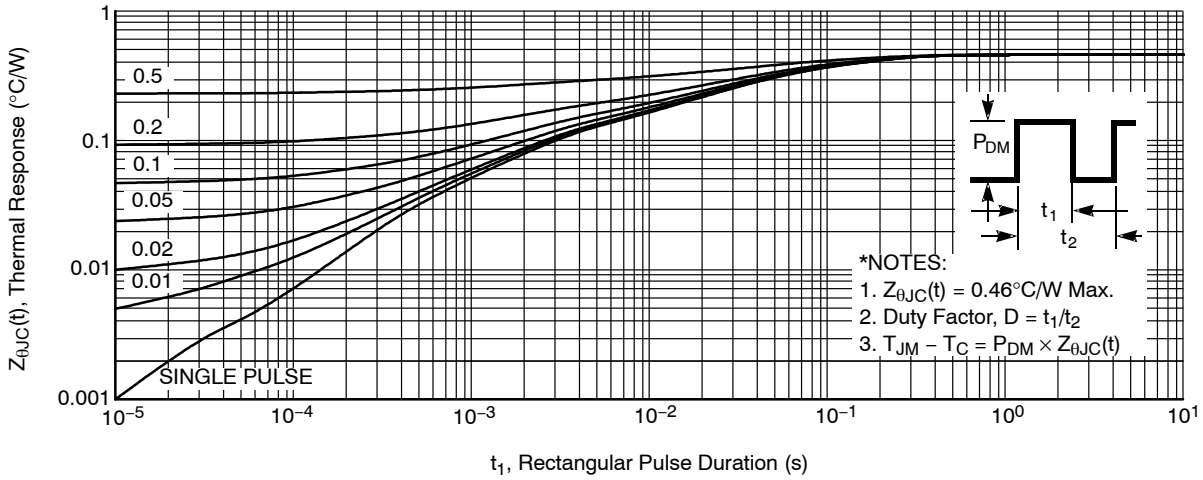


Figure 11. Transient Thermal Response Curve

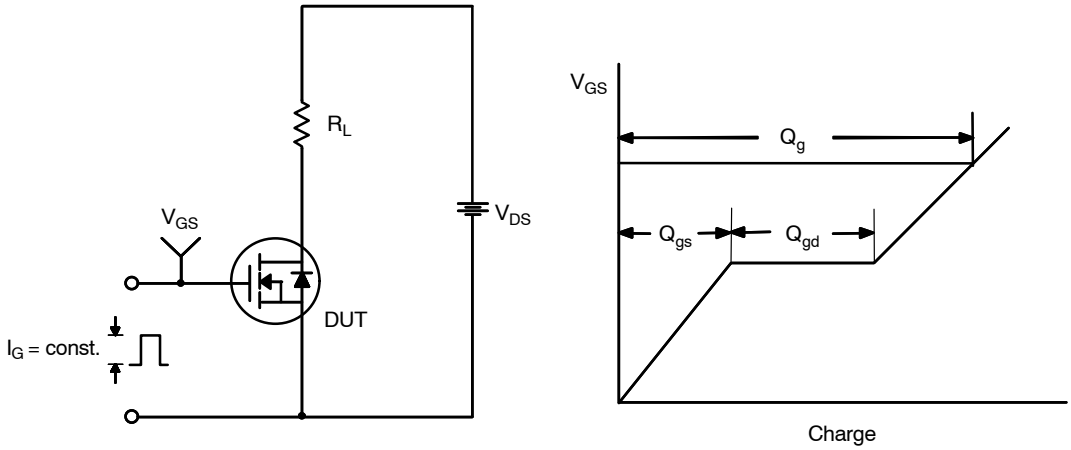


Figure 12. Gate Charge Test Circuit & Waveform

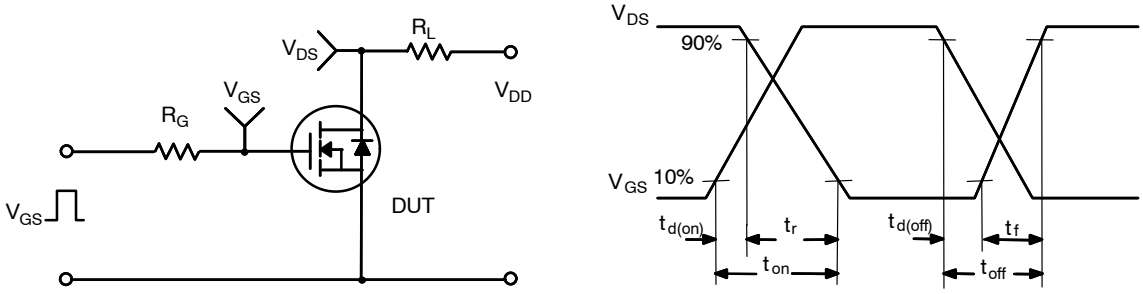


Figure 13. Resistive Switching Test Circuit & Waveforms

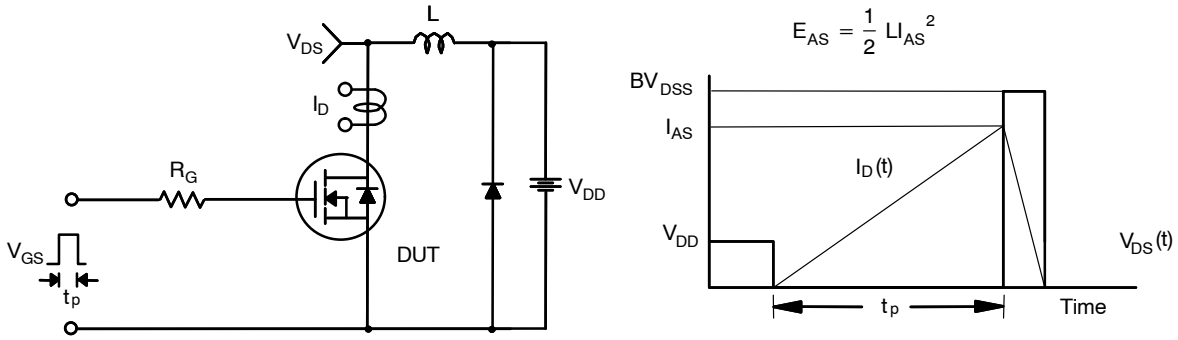


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms

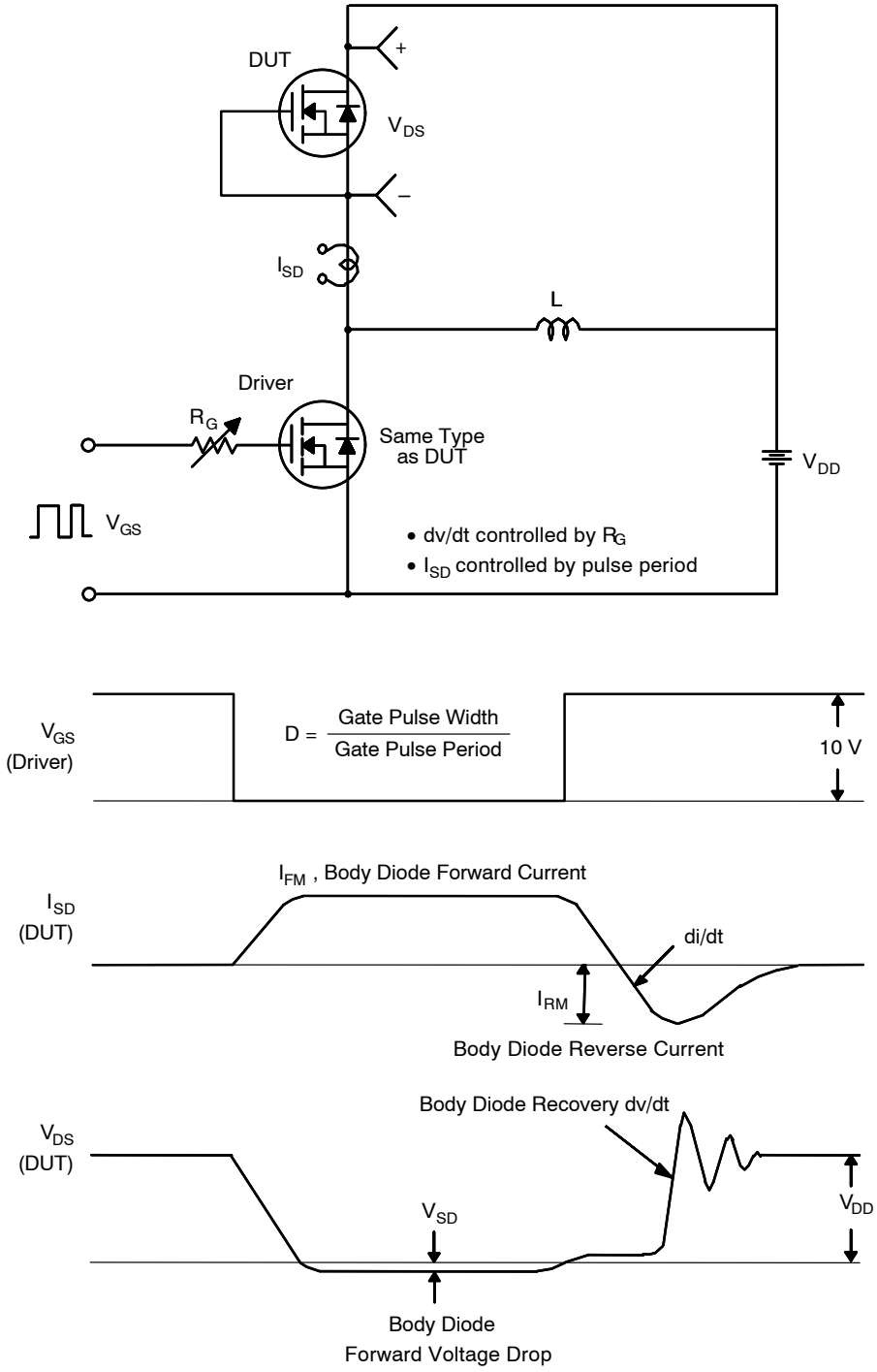


Figure 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms

TO−3P−3LD / EIAJ SC−65, ISOLATED
CASE 340BZ
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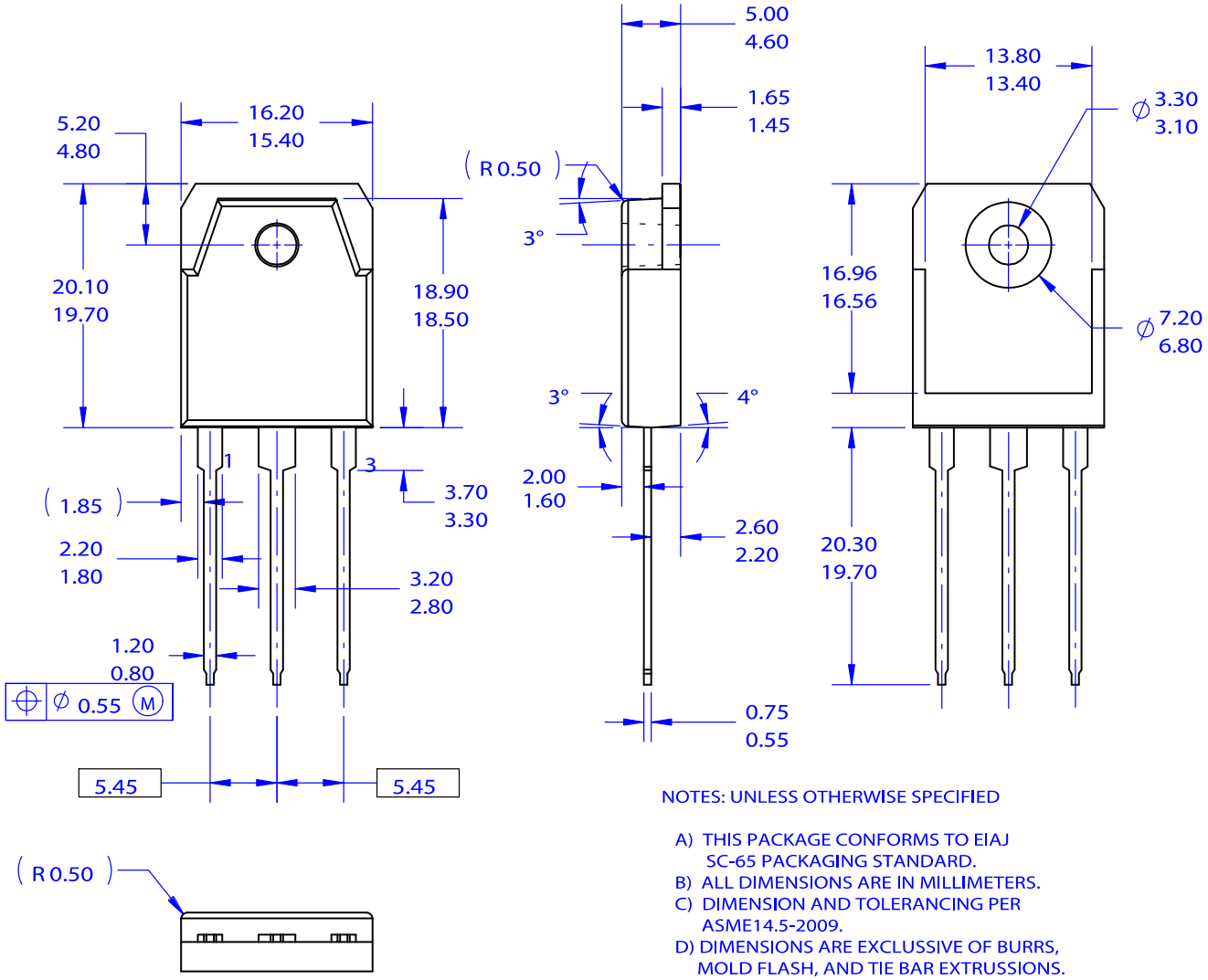
DATE 31 OCT 2016



NOTES: UNLESS OTHERWISE SPECIFIED

A) THIS PACKAGE CONFORMS TO EIAJ SC-65 PACKAGING STANDARD.
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSION AND TOLERANCING PER ASME14.5-2009.
D) DIMENSIONS ARE EXCLUSSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSSIONS.

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