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FDA33N25

N-Channel UniFET™ MOSFET

250 V, 33 A, 94 mΩ

Features

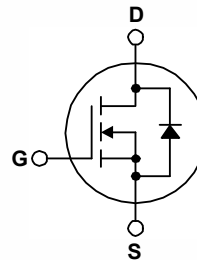
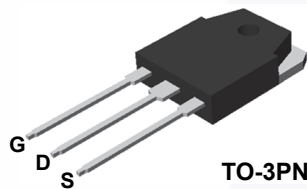
- $R_{DS(on)} = 88 \text{ m}\Omega$ (Typ.) @ $V_{GS} = 10 \text{ V}$, $I_D = 16.5 \text{ A}$
- Low Gate Charge (Typ. 36 nC)
- Low C_{rss} (Typ. 35 pF)
- 100% Avalanche Tested
- RoHS Compliant

Applications

- PDP TV
- Uninterruptible Power Supply
- AC-DC Power Supply

Description

UniFET™ MOSFET is Fairchild Semiconductor's high voltage MOSFET family based on planar stripe and DMOS technology. This MOSFET is tailored to reduce on-state resistance, and to provide better switching performance and higher avalanche energy strength. This device family is suitable for switching power converter applications such as power factor correction (PFC), flat panel display (FPD) TV power, ATX and electronic lamp ballasts.



MOSFET Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	FDA33N25	Unit
V_{DSS}	Drain to Source Voltage	250	V
V_{GSS}	Gate to Source Voltage	±30	V
I_D	Drain Current	- Continuous ($T_C = 25^\circ\text{C}$)	33
		- Continuous ($T_C = 100^\circ\text{C}$)	21
I_{DM}	Drain Current	- Pulsed (Note 1)	132
E_{AS}	Single Pulsed Avalanche Energy	(Note 2)	918
I_{AR}	Avalanche Current	(Note 1)	33
E_{AR}	Repetitive Avalanche Energy	(Note 1)	24.6
dv/dt	Peak Diode Recovery dv/dt	(Note 3)	4.5
P_D	Power Dissipation	($T_C = 25^\circ\text{C}$)	245
		- Derate Above 25°C	1.96
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +150	$^\circ\text{C}$
T_L	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 Seconds	300	$^\circ\text{C}$

Thermal Characteristics

Symbol	Parameter	FDA33N25	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	0.51	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max.	40	

Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FDA33N25	FDA33N25	TO-3PN	Tube	N/A	N/A	30 units

Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
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Off Characteristics

BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 250 \mu\text{A}$, $V_{GS} = 0 \text{ V}$, $T_J = 25^\circ\text{C}$	250	-	-	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250 \mu\text{A}$, Referenced to 25°C	-	0.34	-	$\text{V}/^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 250 \text{ V}$, $V_{GS} = 0 \text{ V}$	-	-	1	μA
		$V_{DS} = 200 \text{ V}$, $T_C = 125^\circ\text{C}$	-	-	10	
I_{GSS}	Gate to Body Leakage Current	$V_{GS} = \pm 30 \text{ V}$, $V_{DS} = 0 \text{ V}$	-	-	± 100	nA

On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = 250 \mu\text{A}$	3.0	-	5.0	V
$R_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10 \text{ V}$, $I_D = 16.5 \text{ A}$	-	0.088	0.094	Ω
g_{FS}	Forward Transconductance	$V_{DS} = 20 \text{ V}$, $I_D = 16.5 \text{ A}$	-	24.2	-	S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 25 \text{ V}$, $V_{GS} = 0 \text{ V}$, $f = 1 \text{ MHz}$	-	1655	2200	pF
C_{oss}	Output Capacitance		-	315	420	pF
C_{rss}	Reverse Transfer Capacitance		-	35	55	pF
$Q_{g(tot)}$	Total Gate Charge at 10V	$V_{DS} = 200 \text{ V}$, $I_D = 33 \text{ A}$, $V_{GS} = 10 \text{ V}$	-	36	46.8	nC
Q_{gs}	Gate to Source Gate Charge		-	10.8	-	nC
Q_{gd}	Gate to Drain "Miller" Charge		(Note 4)	-	16	-

Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 125 \text{ V}$, $I_D = 33 \text{ A}$, $V_{GS} = 10 \text{ V}$, $R_G = 25 \Omega$	-	33	76	ns
t_r	Turn-On Rise Time		-	142	293	ns
$t_{d(off)}$	Turn-Off Delay Time		-	77	165	ns
t_f	Turn-Off Fall Time		(Note 4)	-	68	146

Drain-Source Diode Characteristics

I_S	Maximum Continuous Drain to Source Diode Forward Current	-	-	33	A	
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current	-	-	132	A	
V_{SD}	Drain to Source Diode Forward Voltage	$V_{GS} = 0 \text{ V}$, $I_{SD} = 33 \text{ A}$	-	-	1.4	V
t_{rr}	Reverse Recovery Time	$V_{GS} = 0 \text{ V}$, $I_{SD} = 33 \text{ A}$, $di_F/dt = 100 \text{ A}/\mu\text{s}$	-	256	-	ns
Q_{rr}	Reverse Recovery Charge		-	2.3	-	μC

Notes:

1. Repetitive rating: pulse-width limited by maximum junction temperature.
2. $L = 1.35 \text{ mH}$, $I_{AS} = 33 \text{ A}$, $V_{DD} = 50 \text{ V}$, $R_G = 25 \Omega$, starting $T_J = 25^\circ\text{C}$.
3. $I_{SD} \leq 33 \text{ A}$, $di/dt \leq 200 \text{ A}/\mu\text{s}$, $V_{DD} \leq BV_{DSS}$, starting $T_J = 25^\circ\text{C}$.
4. Essentially independent of operating temperature typical Characteristics

Typical Performance Characteristics

Figure 1. On-Region Characteristics

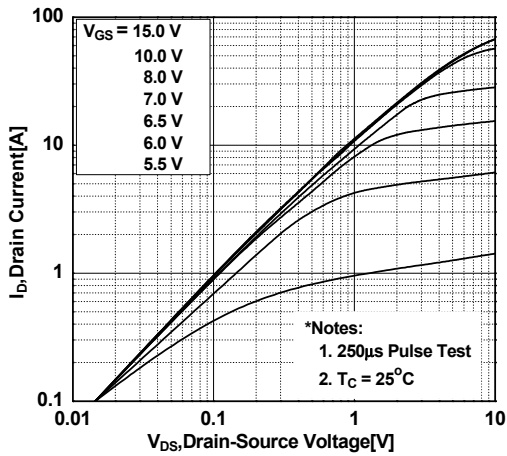


Figure 2. Transfer Characteristics

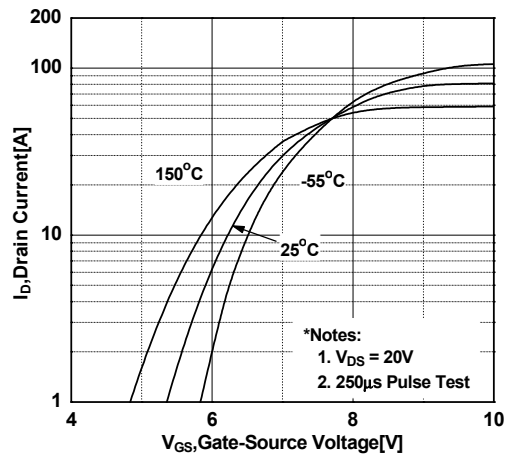


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

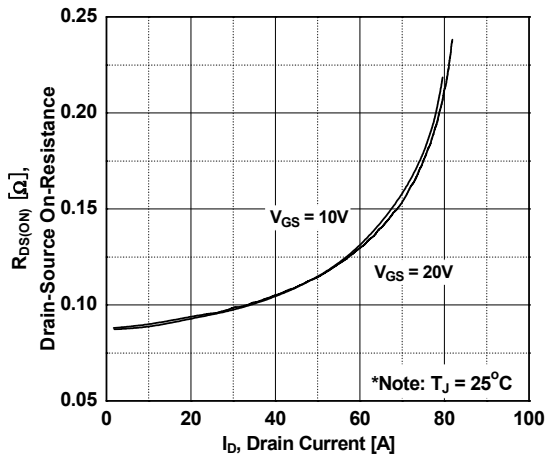


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

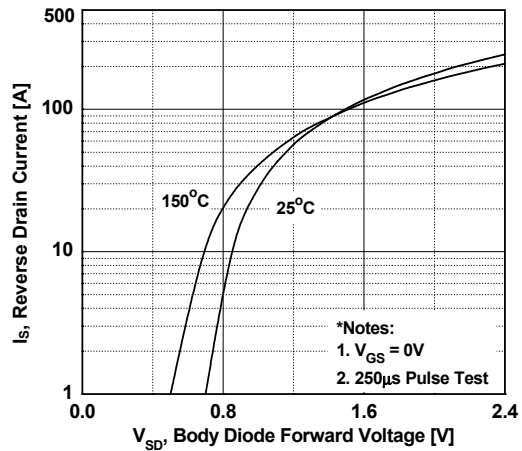


Figure 5. Capacitance Characteristics

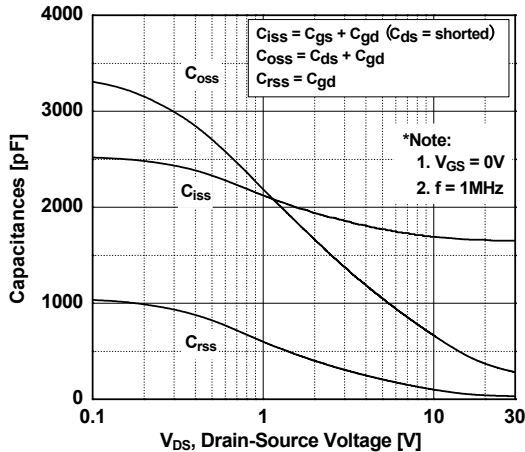
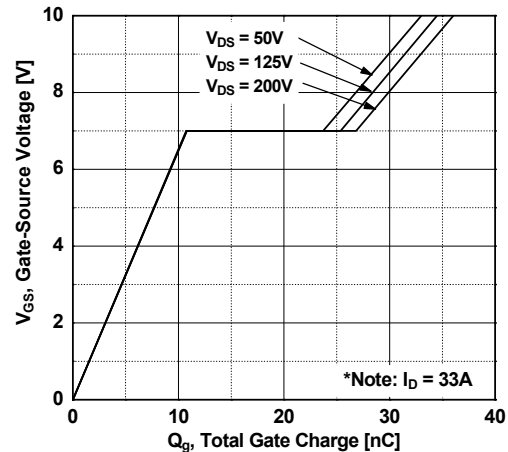


Figure 6. Gate Charge Characteristics



Typical Performance Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

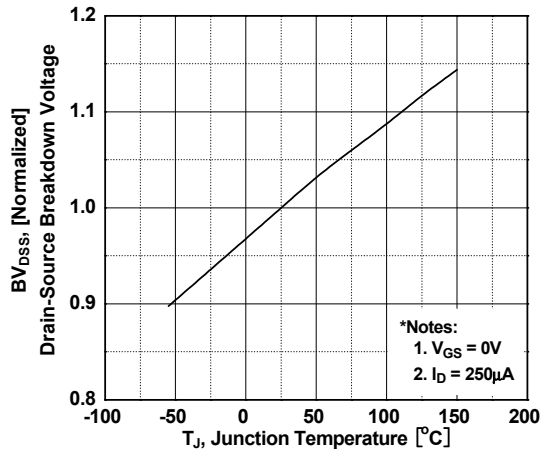


Figure 8. On-Resistance Variation vs. Temperature

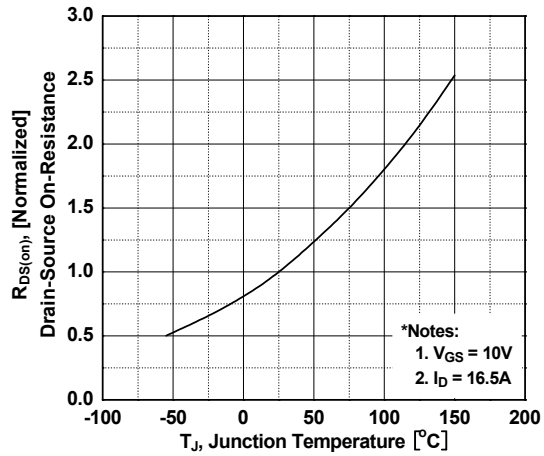


Figure 9. Maximum Safe Operating Area

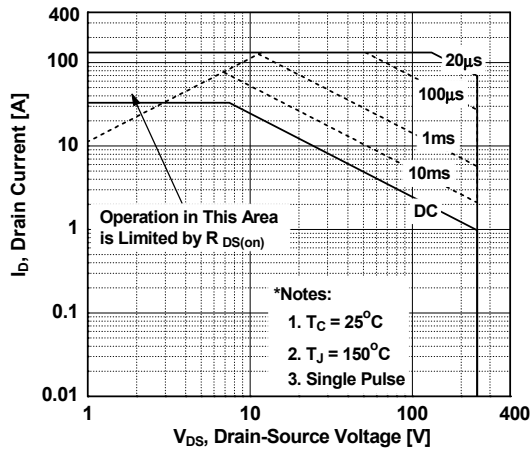


Figure 10. Maximum Drain Current vs. Case Temperature

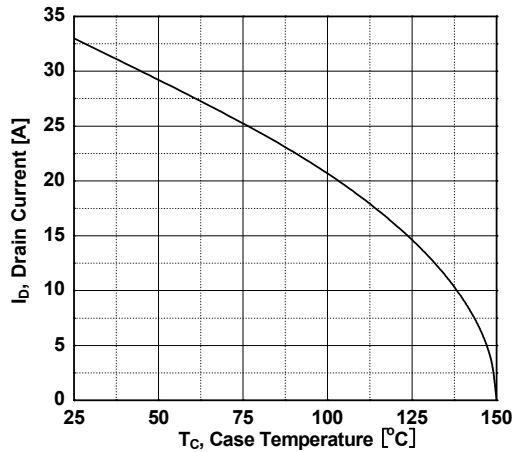


Figure 11. Transient Thermal Response Curve

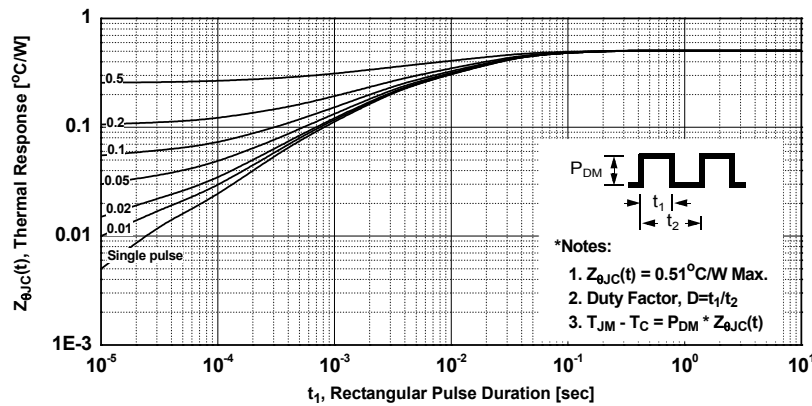




Figure 12. Gate Charge Test Circuit & Waveform



Figure 13. Resistive Switching Test Circuit & Waveforms

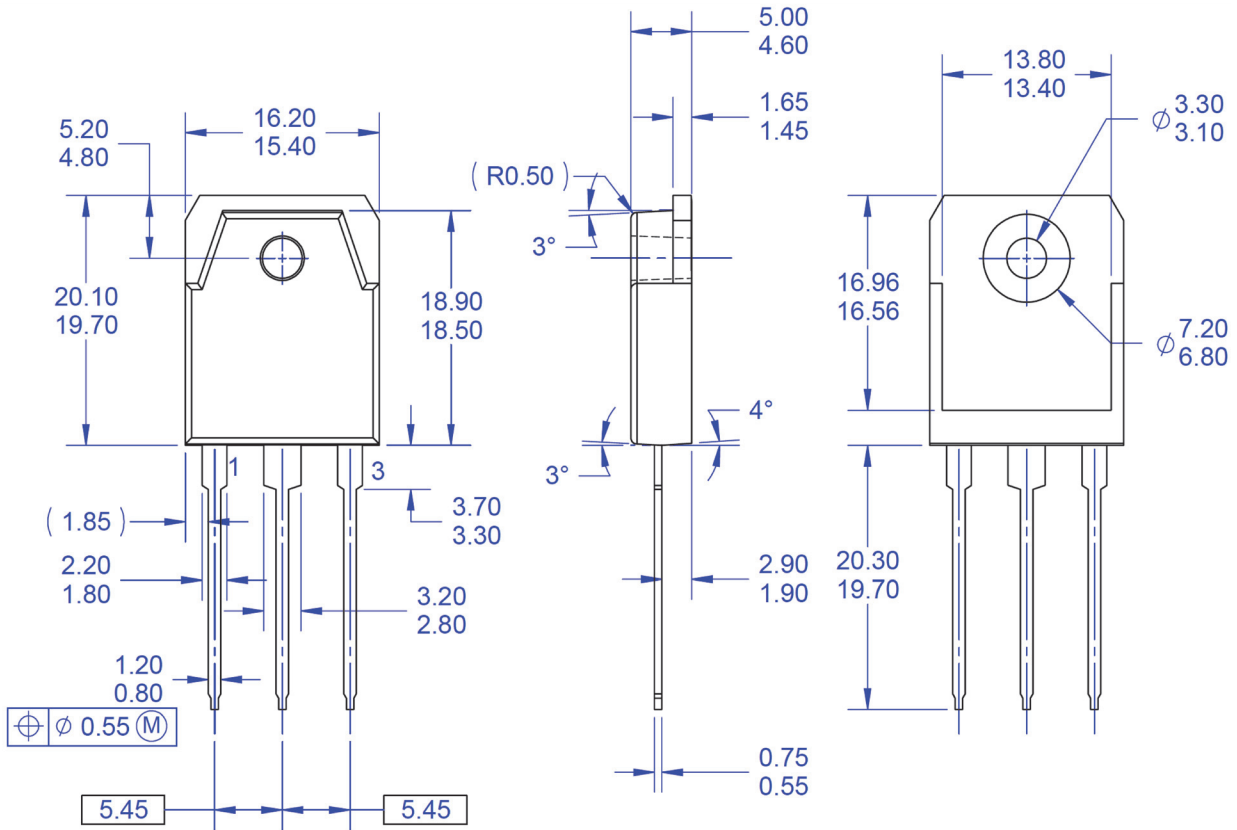


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms



Figure 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms

Mechanical Dimensions



NOTES: UNLESS OTHERWISE SPECIFIED

- A) THIS PACKAGE CONFORMS TO EIAJ SC-65 PACKAGING STANDARD.
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSION AND TOLERANCING PER ASME14.5-2009.
- D) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
- E) DRAWING FILE NAME: TO3PN03AREV1.
- F) FAIRCHILD SEMICONDUCTOR.

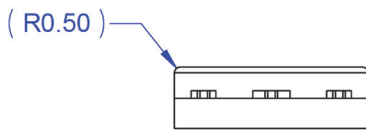


Figure 16. TO3PN, 3-Lead, Plastic, EIAJ SC-65

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Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
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