# MOSFET – P-Channel, POWERTRENCH®

## 1.8 V Specified

# FDC606P

### General Description

This P−Channel 1.8 V specified MOSFET uses **onsemi**’s low voltage POWERTRENCH process. It has been optimized for battery power management applications.

### Features

- −6 A, −12 V
  - $R_{DS(on)}$ = 26 mΩ @ $V_{GS}$ = −4.5 V
  - $R_{DS(on)}$ = 35 mΩ @ $V_{GS}$ = −2.5 V
  - $R_{DS(on)}$ = 53 mΩ @ $V_{GS}$ = −1.8 V
- Fast Switching Speed
- High Performance Trench Technology for Extremely Low $R_{DS(on)}$
- This is a Pb−Free and Halide Free Device

### Applications

- Battery Management
- Load Switch
- Battery Protection

### ABSOLUTE MAXIMUM RATINGS ($T_A$ = 25°C unless otherwise noted)

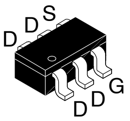
| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DSS}$ | Drain−Source Voltage | −12 | V |
| $V_{GSS}$ | Gate−Source Voltage | ±8 | V |
| $I_D$ | Drain Current<br>−Continuous (Note 1a.)<br>−Pulsed | <br>−6<br>−20 | A |
| $P_D$ | Maximum Power Dissipation<br>(Note 1a.)<br>(Note 1b.) | <br>1.6<br>0.8 | W |
| $T_J$, $T_{STG}$ | Operating and Storage Junction Temperature Range | −55 to +150 | °C |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

### THERMAL CHARACTERISTICS

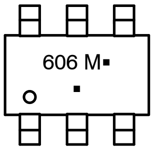
| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $R_{\theta JA}$ | Thermal Resistance, Junction−to−Ambient (Note 1a.) | 78 | °C/W |
| $R_{\theta JC}$ | Thermal Resistance, Junction−to−Case (Note 1) | 30 | °C/W |

| $V_{DSS}$ | $R_{DS(on)}$ MAX | $I_D$ MAX |
|---|---|---|
| −12 V | 26 mΩ @ −4.5 V | −6 A |
| | 35 mΩ @ −2.5 V | |
| | 53 mΩ @ −1.8 V | |



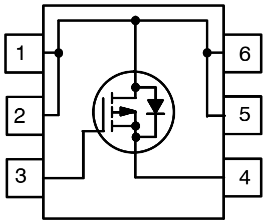
**TSOT23 6−Lead**
**(SUPERSOT™−6)**
**CASE 419BL**

### MARKING DIAGRAM



606 = Specific Device Code
M = Date Code
▪ = Pb−Free Package
(Note: Microdot may be in either location)

### PIN ASSIGNMENT



### ORDERING INFORMATION

| Device | Package | Shipping† |
|---|---|---|
| FDC606P | TSOT−23−6<br>(SUPERSOT™−6)<br>(Pb−Free) | 3000 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

## ELECTRICAL CHARACTERISTICS ($T_A$ = 25°C unless otherwise noted)

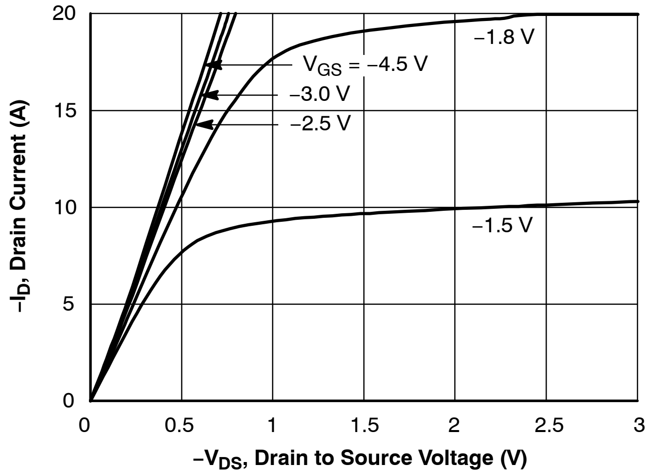
| Symbol | Parameter | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| $BV_{DSS}$ | Drain–Source Breakdown Voltage | $V_{GS}$ = 0 V, $I_D$ = –250 μA | –12 | – | – | V |
| $\frac{\Delta BV_{DSS}}{\Delta T_J}$ | Breakdown Voltage Temperature Coefficient | $I_D$ = –250 μA, Referenced to 25°C | – | –3 | – | mV/°C |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | $V_{DS}$ = –10 V, $V_{GS}$ = 0 V | – | – | –1 | μA |
| $I_{GSSF}$ | Gate–Body Leakage, Forward | $V_{GS}$ = 8 V, $V_{DS}$ = 0 V | – | – | 100 | nA |
| $I_{GSSR}$ | Gate–Body Leakage, Reverse | $V_{GS}$ = –8 V, $V_{DS}$ = 0 V | – | – | –100 | nA |
| **ON CHARACTERISTICS** (Note 2) | | | | | | |
| $V_{GS(th)}$ | Gate Threshold Voltage | $V_{DS}$ = $V_{GS}$, $I_D$ = –250 μA | –0.4 | –0.5 | –1.5 | V |
| $\frac{\Delta V_{GS(th)}}{\Delta T_J}$ | Gate Threshold Voltage Temperature Coefficient | $I_D$ = –250 μA, Referenced to 25°C | – | 2.5 | – | mV/°C |
| $R_{DS(on)}$ | Static Drain–Source On–Resistance | $V_{GS}$ = –4.5 V, $I_D$ = –6 A<br>$V_{GS}$ = –2.5 V, $I_D$ = –5 A<br>$V_{GS}$ = –1.8 V, $I_D$ = –4 A<br>$V_{GS}$ = –4.5 V, $I_D$ = –6 A, $T_J$ = 125°C | –<br>–<br>–<br>– | 21<br>26<br>34<br>28 | 26<br>35<br>53<br>35 | mΩ |
| $I_{D(on)}$ | On–State Drain Current | $V_{GS}$ = –4.5 V, $V_{DS}$ = –5 V | –20 | – | – | A |
| $g_{FS}$ | Forward Transconductance | $V_{GS}$ = –5 V, $I_D$ = –6 A | – | 25 | – | S |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| $C_{iss}$ | Input Capacitance | $V_{DS}$ = –6 V, $V_{GS}$ = 0 V, f = 1.0 MHz | – | 1699 | – | pF |
| $C_{oss}$ | Output Capacitance | | – | 679 | – | pF |
| $C_{rss}$ | Reverse Transfer Capacitance | | – | 423 | – | pF |
| **SWITCHING CHARACTERISTICS** (Note 2) | | | | | | |
| $t_{d(on)}$ | Turn–On Delay Time | $V_{DD}$ = –6 V, $I_D$ = –1 A,<br>$V_{GS}$ = –4.5 V, $R_{GEN}$ = 6 Ω | – | 11 | 19 | ns |
| $t_r$ | Turn–On Rise Time | | – | 10 | 20 | ns |
| $t_{d(off)}$ | Turn–Off Delay Time | | – | 89 | 142 | ns |
| $t_f$ | Turn–Off Fall Time | | – | 70 | 112 | ns |
| $Q_{g(TOT)}$ | Total Gate Charge | $V_{DS}$ = –6 V, $I_D$ = –6 A,<br>$V_{GS}$ = –4.5 V | – | 18 | 25 | nC |
| $Q_{gs}$ | Gate–Source Charge | | – | 3 | – | nC |
| $Q_{gd}$ | Gate–Drain “Miller” Charge | | – | 4.2 | – | nC |
| **DRAIN–SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS** | | | | | | |
| $I_S$ | Maximum Continuous Drain–Source Diode Forward Current | | – | – | –1.3 | A |
| $V_{SD}$ | Drain–Source Diode Forward Voltage | $V_{GS}$ = 0 V, $I_S$ = –1.3 A (Note 2) | – | –0.6 | –1.2 | V |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTES:

1. $R_{\theta JA}$ is the sum of the junction–to–case and case–to–ambient resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user’s board design.
   a. 78°C/W when mounted on a 1in$^2$ pad of 2oz copper on FR–4 board.
   b. 156°C/W when mounted on a minimum pad.
2. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

## TYPICAL CHARACTERISTICS



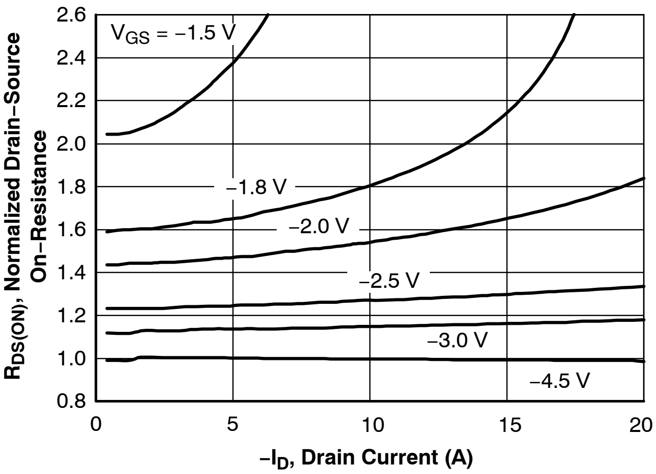
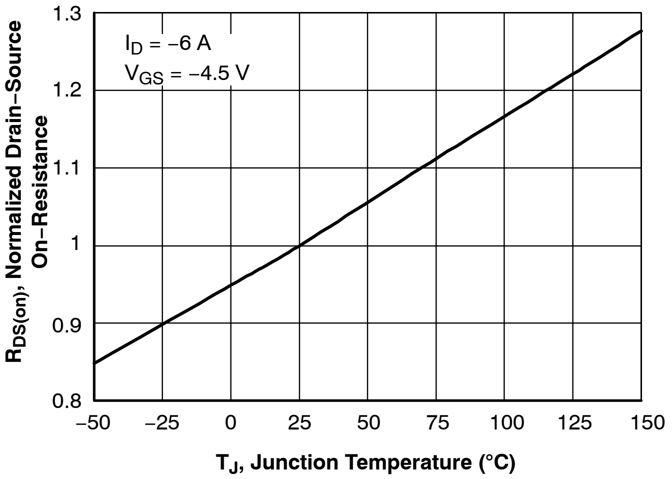


Figure 1. On−Region Characteristics

Figure 2. On−Resistance Variation with Drain Current and Gate Voltage



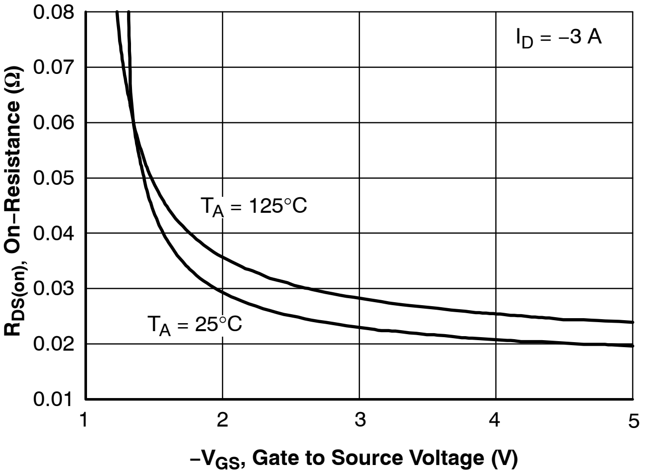
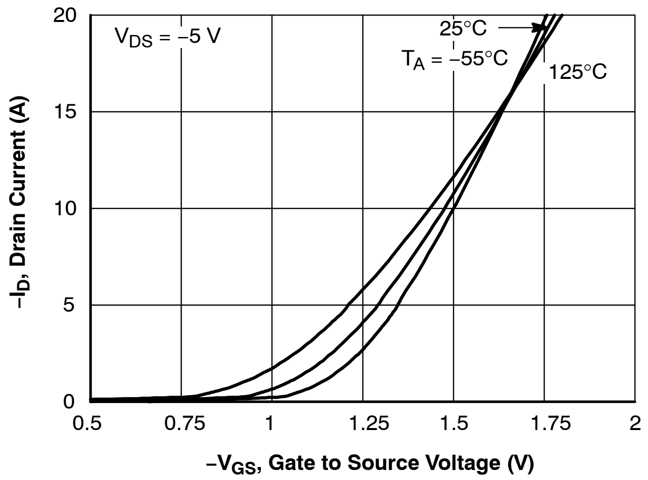


Figure 3. On−Resistance Variation with Temperature

Figure 4. On−Resistance Variation with Gate−to−Source Voltage



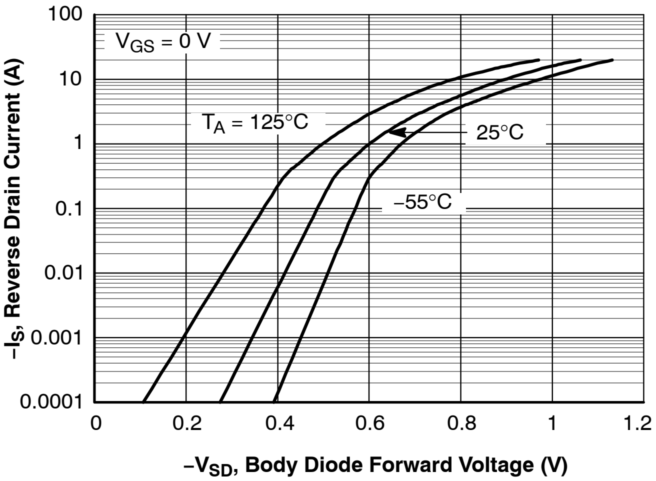


Figure 5. Transfer Characteristics

Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature

## TYPICAL CHARACTERISTICS (continued)

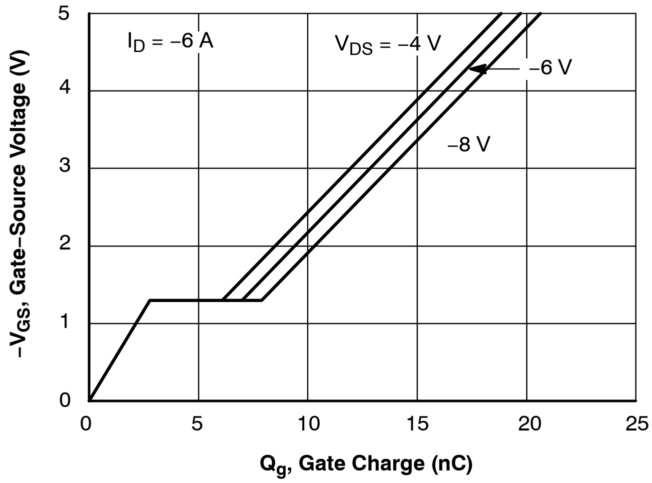


Figure 7. Gate Charge Characteristics

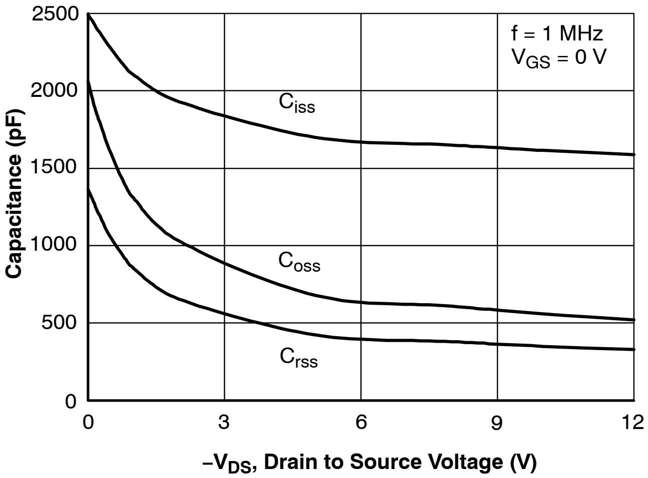


Figure 8. Capacitance Characteristics

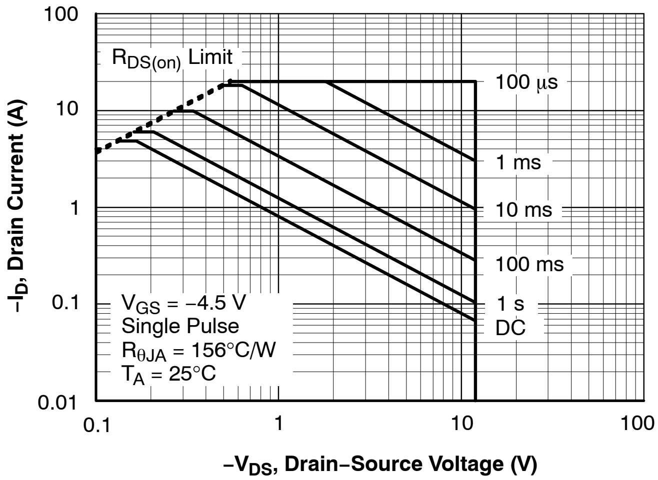


Figure 9. Maximum Safe Operating Area

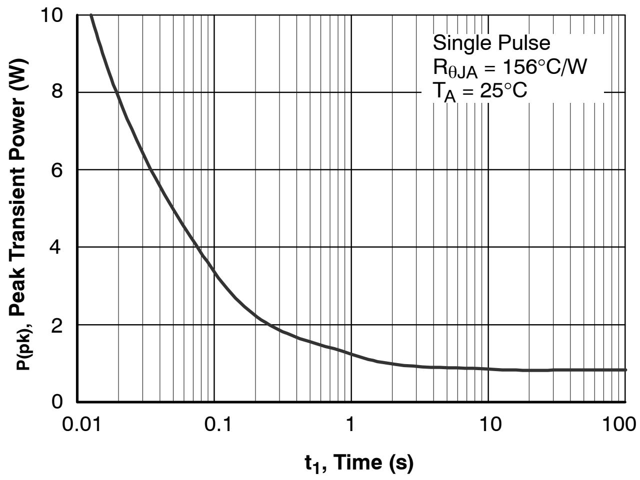


Figure 10. Single Pulse Maximum Power Dissipation

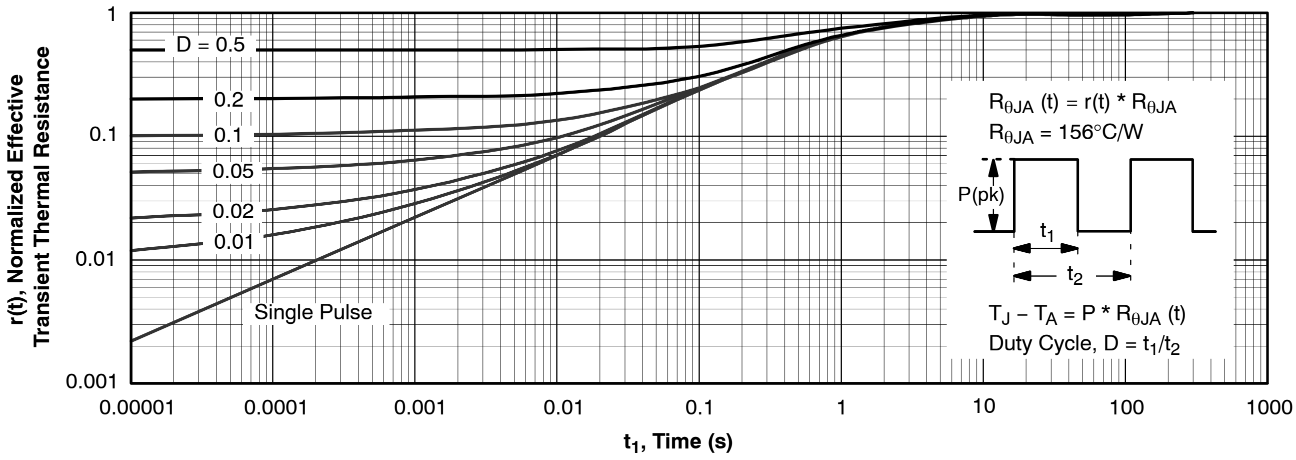


Figure 11. Transient Thermal Response Curve

NOTE: Thermal characterization performed using the conditions described in Note 1b.
Transient thermal response will change depending on the circuit board design.

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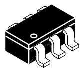
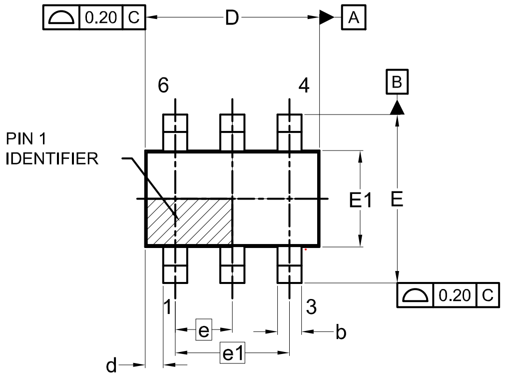
# MECHANICAL CASE OUTLINE
## PACKAGE DIMENSIONS



**SCALE 2:1**

**TSOT23 6−Lead**
CASE 419BL
ISSUE A

DATE 31 AUG 2020

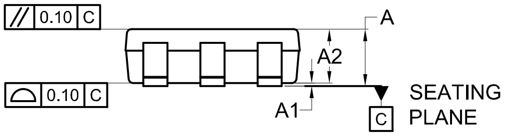


TOP VIEW

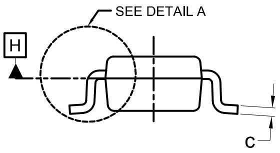
NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.25MM PER END. DIMENSIONS D AND E1 ARE DETERMINED AT DATUM H.
4. SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

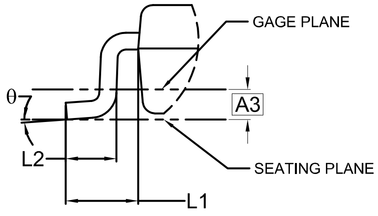
| DIM | MILLIMETERS | | |
|---|---|---|---|
| | MIN. | NOM. | MAX. |
| A | 0.90 | 1.00 | 1.10 |
| A1 | 0.00 | 0.05 | 0.10 |
| A2 | 0.70 | 0.85 | 1.00 |
| A3 | 0.25 BSC | | |
| b | 0.25 | 0.38 | 0.50 |
| c | 0.10 | 0.18 | 0.26 |
| D | 2.80 | 2.95 | 3.10 |
| d | 0.30 REF | | |
| E | 2.50 | 2.75 | 3.00 |
| E1 | 1.30 | 1.50 | 1.70 |
| e | 0.95 BSC | | |
| e1 | 1.90 BSC | | |
| L1 | 0.60 REF | | |
| L2 | 0.20 | 0.40 | 0.60 |
| ϴ | 0° | --- | 10° |



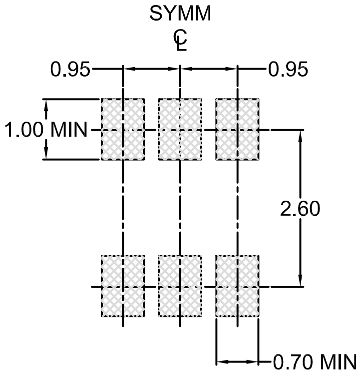
FRONT VIEW



SIDE VIEW



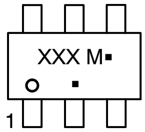
DETAIL A



LAND PATTERN
RECOMMENDATION

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

### GENERIC MARKING DIAGRAM*



XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present. Some products may not follow the Generic Marking.

| | | |
|---|---|---|
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