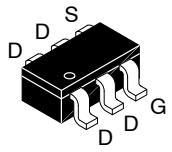
MOSFET – Single N-Channel, Logic Level, POWERTRENCH®

30 V, 6.1 A, 27 mΩ

FDC855N

V_{DS}	$r_{DS(on)}$ MAX	I_D MAX
30 V	27 mΩ @ 10 V	6.1 A
	36 mΩ @ 4.5 V	5.3 A



TSOT23 6−Lead
SUPERSOT™ −6
CASE 419BL

General Description

This N−Channel Logic Level MOSFET is an efficient solution for low voltage and battery powered applications. Utilizing **onsemi**'s advanced POWERTRENCH process, this device possesses minimized on−state resistance to optimize the power consumption. They are ideal for applications where in−line power loss is critical.

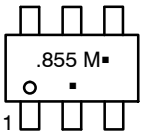
Features

- Max $r_{DS(on)}$ = 27 mΩ at V_{GS} = 10 V, I_D = 6.1 A
- Max $r_{DS(on)}$ = 36 mΩ at V_{GS} = 4.5 V, I_D = 5.3 A
- SUPERSOT™ −6 Package: Small Footprint (72% smaller than Standard SO−8) Low Profile (1 mm thick)
- This Device is Pb−Free and is RoHS Compliant

Application

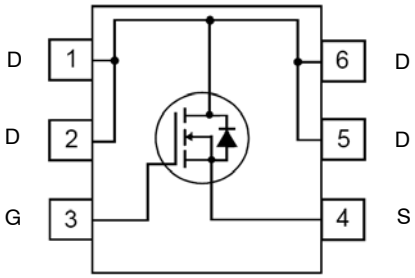
- Power Management in Notebook, Hard Disk Drive

MARKING DIAGRAM



.855 = Specific Device Code
M = Date Code
▪ = Pb−Free Package
(Note: Microdot may be in either location)

PINOUT



ORDERING INFORMATION

See detailed ordering and shipping information on page 5 of this data sheet.

MOSFET MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Symbol	Parameter		Ratings	Units
V_{DS}	Drain to Source Voltage		30	V
V_{GS}	Gate to Source Voltage		±20	V
I_D	Drain Current	Continuous (Note 1a)	6.1	A
		Pulsed	20	A
P_D	Power Dissipation (Steady State)	(Note 1a)	1.6	W
		(Note 1b)	0.8	
T_J, T_{STG}	Operating and Storage Junction Temperature Range		−55 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

Symbol	Parameter	Ratings	Units
$R_{\theta JC}$	Thermal Resistance, Junction to Case (Note 1)	30	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	78	°C/W

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 250 μA, V_{GS} = 0 V	30	–	–	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, referenced to 25°C	–	24	–	mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 24 V, V_{GS} = 0 V	–	–	1	μA
		V_{DS} = 24 V, V_{GS} = 0 V, T_C = 125°C	–	–	250	
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±20 V, V_{DS} = 0 V	–	–	±100	nA
ON CHARACTERISTICS						
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 250 μA	1.0	2.0	3.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = 250 μA, referenced to 25°C	–	–6	–	mV/°C
$r_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = 10 V, I_D = 6.1 A	–	20.7	27.0	mΩ
		V_{GS} = 4.5 V, I_D = 5.3 A	–	28.2	36.0	
		V_{GS} = 10 V, I_D = 6.1 A, T_J = 125°C	–	30.1	39.3	
g_{FS}	Forward Transconductance	V_{DD} = 10 V, I_D = 6.1 A	–	20	–	S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = 15 V, V_{GS} = 0 V, f = 1 MHz	–	493	655	pF
C_{oss}	Output Capacitance		–	108	145	pF
C_{rss}	Reverse Transfer Capacitance		–	62	95	pF
R_g	Gate Resistance	f = 1 MHz	–	1.0	–	Ω
SWITCHING CHARACTERISTICS						
$t_{d(on)}$	Turn–On Delay Time	V_{DD} = 15 V, I_D = 6.1 A, V_{GS} = 10 V, R_{GEN} = 6 Ω	–	6	12	ns
t_r	Rise Time		–	2	10	ns
$t_{d(off)}$	Turn–Off Delay Time		–	14	23	ns
t_f	Fall Time		–	2	10	ns
Q_g	Total Gate Charge at 10 V	V_{GS} = 0 V to 10 V, V_{DD} = 15 V, I_D = 6.1 A	–	9.2	13	nC
	Total Gate Charge at 5 V	V_{GS} = 0 V to 5 V, V_{DD} = 15 V, I_D = 6.1 A	–	4.9	7.0	nC
Q_{gs}	Gate to Source Charge	V_{DD} = 15 V, I_D = 6.1 A	–	1.7	–	nC
Q_{gd}	Gate to Drain “Miller” Charge		–	3.1	–	nC
DRAIN–SOURCE DIODE CHARACTERISTICS						
V_{SD}	Source–Drain Diode Forward Voltage	V_{GS} = 0 V, I_S = 1.3 A (Note 2)	–	0.80	1.2	V
t_{rr}	Reverse Recovery Time	I_F = 6.1 A, di/dt = 100 A/μs	–	17	31	ns
Q_{rr}	Reverse Recovery Charge		–	6	12	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. $R_{\theta JA}$ is the sum of the junction–to–case and case–to–ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user’s board design.

a. 78°C/W when mounted on a 1 in^2 pad of 2 oz. copper

b. 156°C/W when mounted on a minimum pad of 2 oz. copper

2. Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0 %.

TYPICAL CHARACTERISTICS

(T_J = 25°C unless otherwise noted)

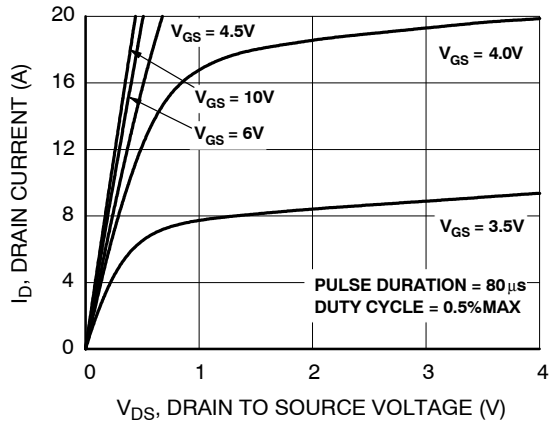


Figure 1. On−Region Characteristics

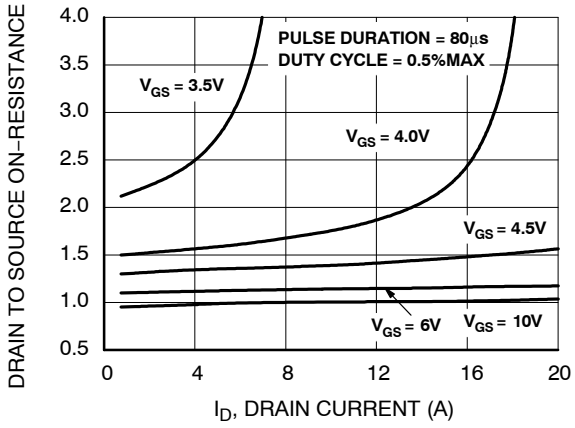


Figure 2. Normalized On−Resistance vs Drain Current and Gate Voltage

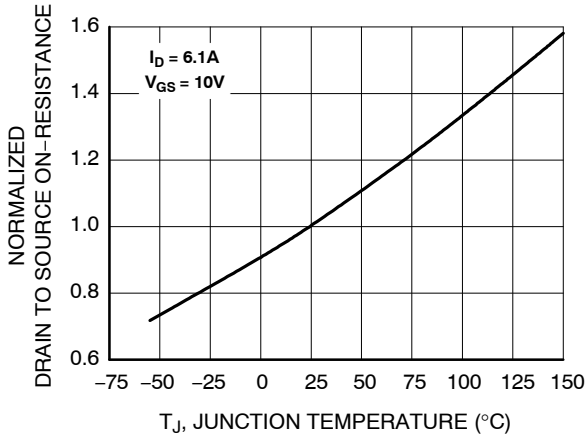


Figure 3. Normalized On−Resistance vs Junction Temperature

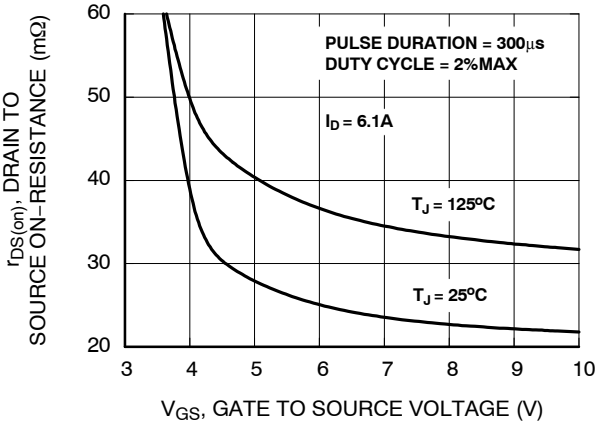


Figure 4. On−Resistance vs Gate to Source Voltage

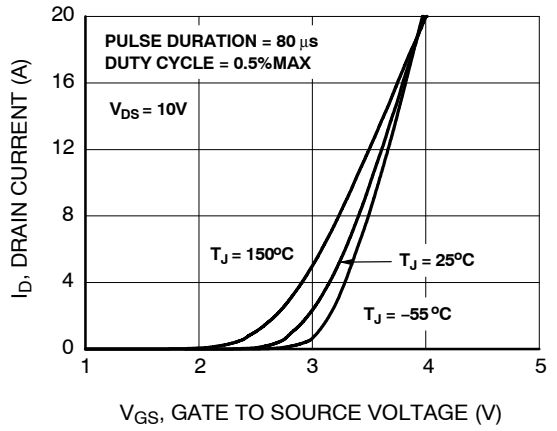


Figure 5. Transfer Characteristics

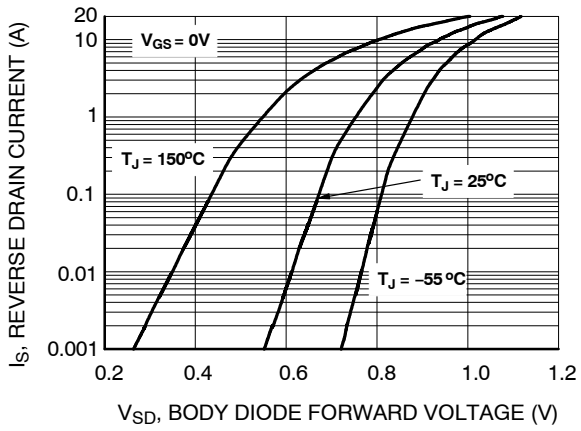


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

TYPICAL CHARACTERISTICS (continued)

(T_J = 25°C unless otherwise noted)

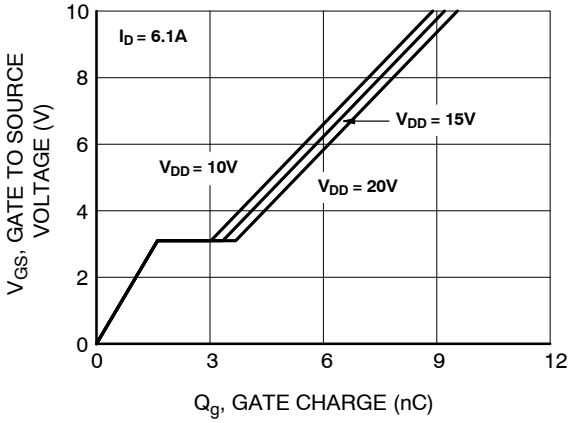


Figure 7. Gate Charge Characteristics

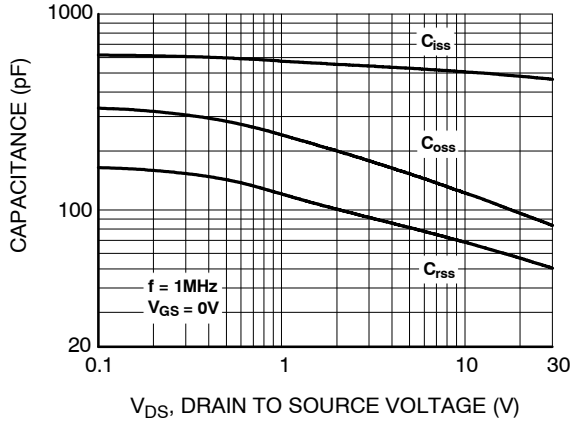


Figure 8. Capacitance vs Drain to Source Voltage

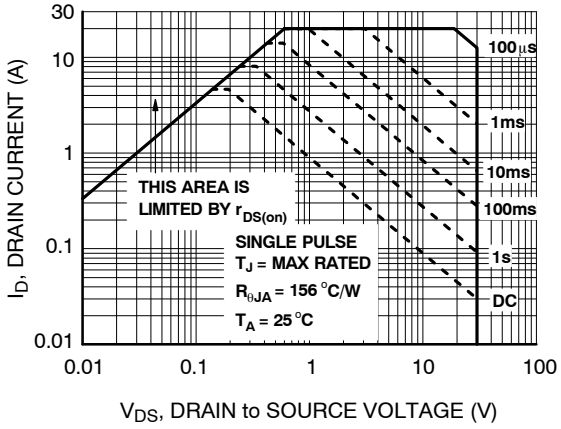


Figure 9. Forward Bias Safe Operating Area

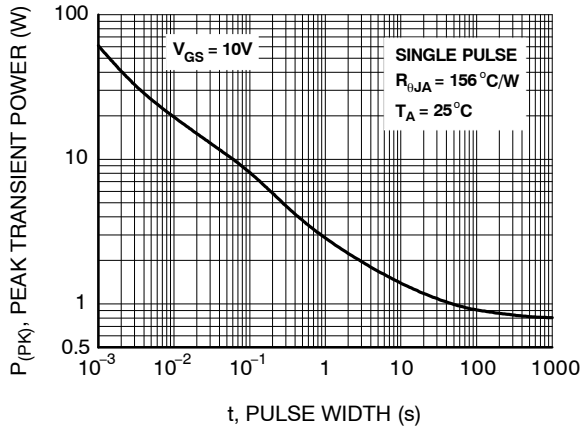


Figure 10. Single Pulse Maximum Power Dissipation

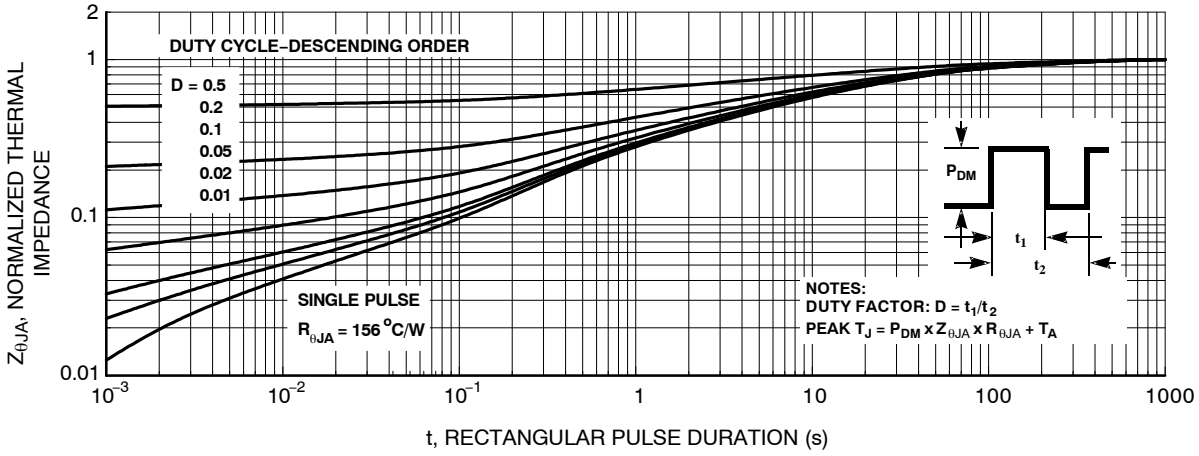


Figure 11. Transient Thermal Response Curve

ORDERING INFORMATION

Device	Device Marking	Package Type	Shipping†
FDC855N	.855	TSOT−23−6 (Pb−free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

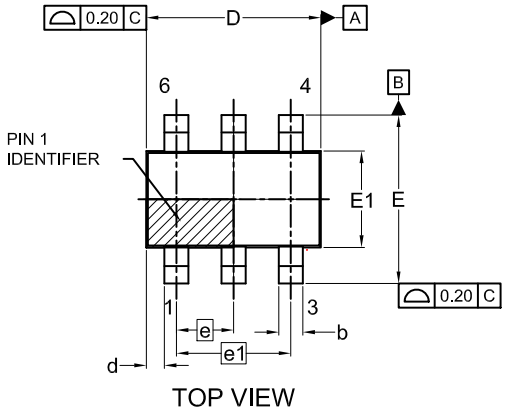
ON Semiconductor®

1

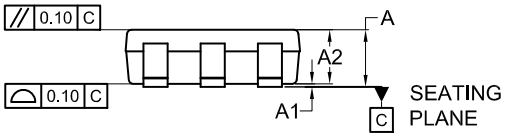
SCALE 2:1

TSOT23 6−Lead
CASE 419BL
ISSUE A

DATE 31 AUG 2020

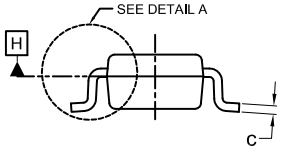


TOP VIEW

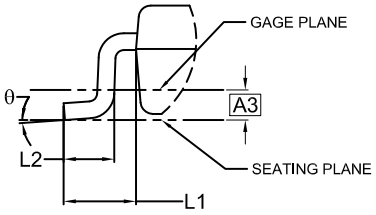


FRONT VIEW

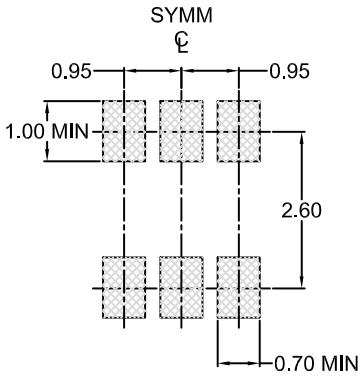
NOTE 4



SIDE VIEW



DETAIL A



LAND PATTERN
RECOMMENDATION

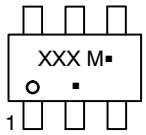
*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.25MM PER END. DIMENSIONS D AND E1 ARE DETERMINED AT DATUM H.
4. SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.90	1.00	1.10
A1	0.00	0.05	0.10
A2	0.70	0.85	1.00
A3		0.25 BSC	
b	0.25	0.38	0.50
c	0.10	0.18	0.26
D	2.80	2.95	3.10
d		0.30 REF	
E	2.50	2.75	3.00
E1	1.30	1.50	1.70
e		0.95 BSC	
e1		1.90 BSC	
L1		0.60 REF	
L2	0.20	0.40	0.60
θ	0°	---	10°

GENERIC MARKING DIAGRAM*



XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present. Some products may not follow the Generic Marking.

DOCUMENT NUMBER:	**98AON83292G**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	**TSOT23 6−Lead**	**PAGE 1 OF 1**

ADDITIONAL INFORMATION

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onsemi Website: www.onsemi.com

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