

# MOSFET – P-Channel, POWERTRENCH®

**-40 V, -50 A, 12.3 mΩ**

## FDD4141-F085

### General Description

This P-Channel MOSFET has been produced using onsemi's proprietary POWERTRENCH technology to deliver low  $R_{DS(on)}$  and optimized  $BV_{DSS}$  capability to offer superior performance benefit in the applications. and optimized switching performance capability reducing power dissipation losses in converter/inverter applications.

### Features

- Typ  $R_{DS(on)}$  = 12.3 mΩ at  $V_{GS} = -10$  V,  $I_D = -12.7$  A
- Typ  $R_{DS(on)}$  = 18.0 mΩ at  $V_{GS} = -4.5$  V,  $I_D = -10.4$  A
- High Performance Trench Technology for Extremely Low  $R_{DS(on)}$
- AEC-Q101 Qualified and PPAP Capable
- This Device is Pb-Free and is RoHS Compliant

### Applications

- Inverter
- Power Supplies

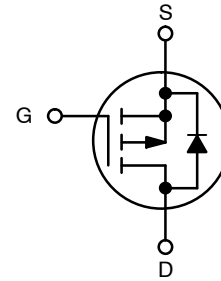
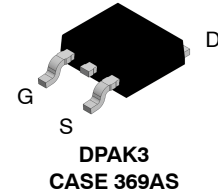
### MOSFET MAXIMUM RATINGS ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Ratings	Unit
$V_{DS}$	Drain to Source Voltage	-40	V
$V_{GS}$	Gate to Source Voltage	±20	V
$I_D$	Drain Current -Continuous (Package limited) $T_C = 25^\circ\text{C}$ -Continuous (Silicon limited) $T_C = 25^\circ\text{C}$ -Continuous $T_A = 25^\circ\text{C}$ (Note 1a) -Pulsed	-50 -58 -10.8 -100	A
$E_{AS}$	Single Pulse Avalanche Energy (Note 3)	337	mJ
$P_D$	Power Dissipation - $T_C = 25^\circ\text{C}$ - $T_A = 25^\circ\text{C}$ (Note 1a)	69 2.4	W
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to +175	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

### THERMAL CHARACTERISTICS

Symbol	Parameter	Ratings	Unit
$R_{\theta JC}$	Maximum Thermal Resistance, Junction to Case	1.8	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Maximum Thermal Resistance, Junction to Ambient	52	



P-Channel MOSFET

### MARKING DIAGRAM



- &Z = Assembly Plant Code
- &3 = Date Code (Year & Week)
- &T = Traceability Code
- FDD4141 = Specific Device Code

### ORDERING INFORMATION

See detailed ordering and shipping information on page 3 of this data sheet.

# FDD4141-F085

## ELECTRICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
<b>OFF CHARACTERISTICS</b>						
$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = -250\ \mu\text{A}$ , $V_{GS} = 0\ \text{V}$	-40	-	-	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = -250\ \mu\text{A}$ , referenced to $25^\circ\text{C}$	-	-29	-	mV/ $^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = -32\ \text{V}$ , $V_{GS} = 0\ \text{V}$	-	-	-1	$\mu\text{A}$
$I_{GSS}$	Gate to Source Leakage Current	$V_{GS} = \pm 20\ \text{V}$ , $V_{DS} = 0\ \text{V}$	-	-	$\pm 100$	nA

## ON CHARACTERISTICS

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$ , $I_D = -250\ \mu\text{A}$	-1	-1.8	-3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = -250\ \mu\text{A}$ , referenced to $25^\circ\text{C}$	-	5.8	-	mV/ $^\circ\text{C}$
$R_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = -10\ \text{V}$ , $I_D = -12.7\ \text{A}$	-	10.1	12.3	m $\Omega$
		$V_{GS} = -4.5\ \text{V}$ , $I_D = -10.4\ \text{A}$	-	14.5	18.0	
		$V_{GS} = -10\ \text{V}$ , $I_D = -12.7\ \text{A}$ , $T_J = 175^\circ\text{C}$	-	17.3	19.4	
$g_{FS}$	Forward Transconductance	$V_{DS} = -5\ \text{V}$ , $I_D = -12.7\ \text{A}$	-	38	-	S

## DYNAMIC CHARACTERISTICS

$C_{iss}$	Input Capacitance	$V_{DS} = -20\ \text{V}$ , $V_{GS} = 0\ \text{V}$ , $f = 1\ \text{MHz}$	-	2085	2775	pF
$C_{oss}$	Output Capacitance		-	360	480	pF
$C_{rss}$	Reverse Transfer Capacitance		-	210	310	pF
$R_g$	Gate Resistance	$f = 1\ \text{MHz}$	-	4.6	-	$\Omega$

## SWITCHING CHARACTERISTICS

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = -20\ \text{V}$ , $I_D = -12.7\ \text{A}$ , $V_{GS} = -10\ \text{V}$ , $R_{GEN} = 6\ \Omega$	-	10	19	ns
$t_r$	Rise Time		-	7	13	ns
$t_{d(off)}$	Turn-Off Delay Time		-	38	60	ns
$t_f$	Fall Time		-	15	27	ns
$Q_g$	Total Gate Charge	$V_{GS} = 0\ \text{V}$ to $-10\ \text{V}$ $V_{DD} = -20\ \text{V}$ , $I = -12.7\ \text{A}$	-	36	50	nC
		$V_{GS} = 0\ \text{V}$ to $-5\ \text{V}$ $V_{DD} = -20\ \text{V}$ , $I_D = -12.7\ \text{A}$	-	19	27	nC
$Q_{gs}$	Gate to Source Charge	$V_{DD} = -20\ \text{V}$ , $I_D = -12.7\ \text{A}$	-	7	-	nC
$Q_{gd}$	Gate to Drain "Miller" Charge	$V_{DD} = -20\ \text{V}$ , $I_D = -12.7\ \text{A}$	-	8	-	nC

## DRAIN-SOURCE DIODE CHARACTERISTICS

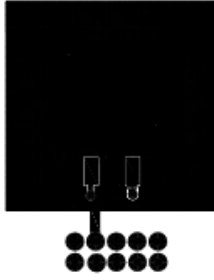
$V_{SD}$	Source to Drain Diode Forward Voltage	$V_{GS} = 0\ \text{V}$ , $I_S = -12.7\ \text{A}$ (Note 2)	-	-0.8	-1.2	V
$t_{rr}$	Reverse Recovery Time	$I_F = -12.7\ \text{A}$ , $di/dt = 100\ \text{A}/\mu\text{s}$	-	29	44	ns
$Q_{rr}$	Reverse Recovery Charge		-	26	40	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

# FDD4141-F085

**NOTES:**

1.  $R_{\theta JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta JA}$  is determined by the user's board design.



a) 52°C/W when mounted on a 1 in<sup>2</sup> pad of 2 oz copper.



b) 100°C/W when mounted on a minimum pad.

2. Pulse Test: Pulse Width < 300  $\mu$ s, Duty cycle < 2.0%.
3. Starting  $T_J = 25^\circ\text{C}$ ,  $L = 3 \text{ mH}$ ,  $I_{AS} = 15 \text{ A}$ ,  $V_{DD} = 40 \text{ V}$ ,  $V_{GS} = 10 \text{ V}$ .

**PACKAGE MARKING AND ORDERING INFORMATION**

Device Marking	Device	Package	Reel Size <sup>†</sup>	Tape Width	Quantity
FDD4141	FDD4141-F085	DPAK3	13"	16 mm	2500 Units

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

TYPICAL CHARACTERISTICS

( $T_J = 25^\circ\text{C}$  unless otherwise noted)

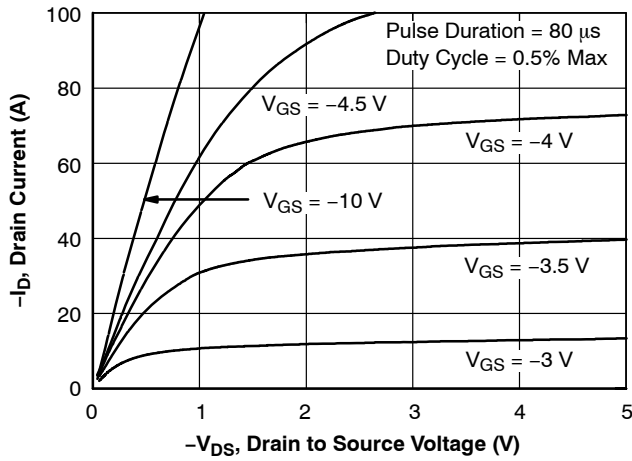


Figure 1. On-Region Characteristics

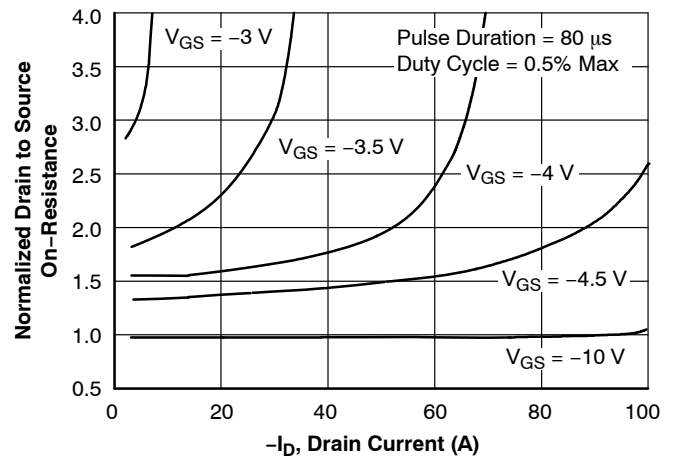


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

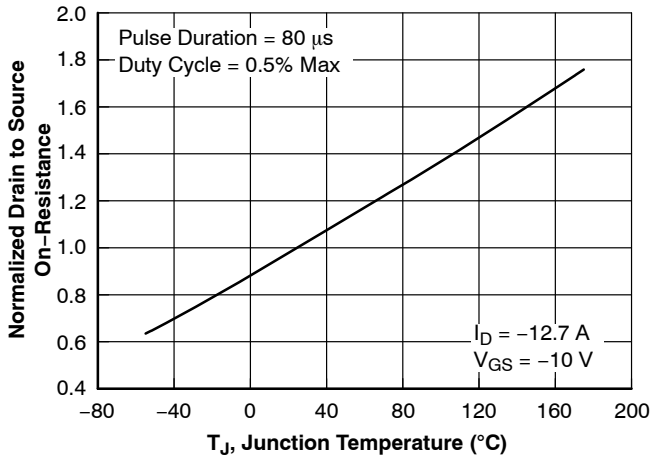


Figure 3. Normalized On-Resistance vs Junction Temperature

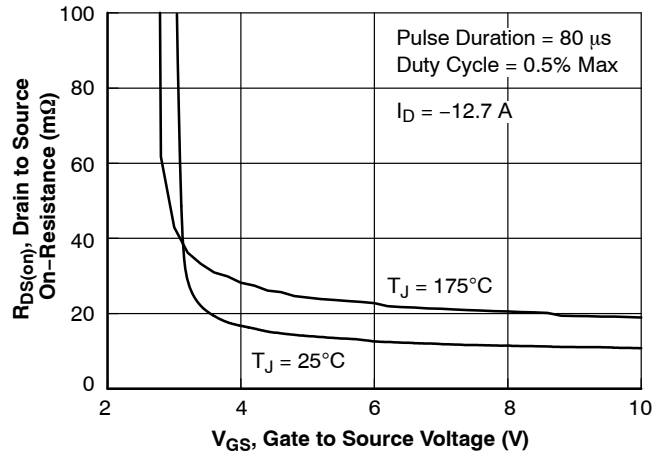


Figure 4. On-Resistance vs Gate to Source Voltage

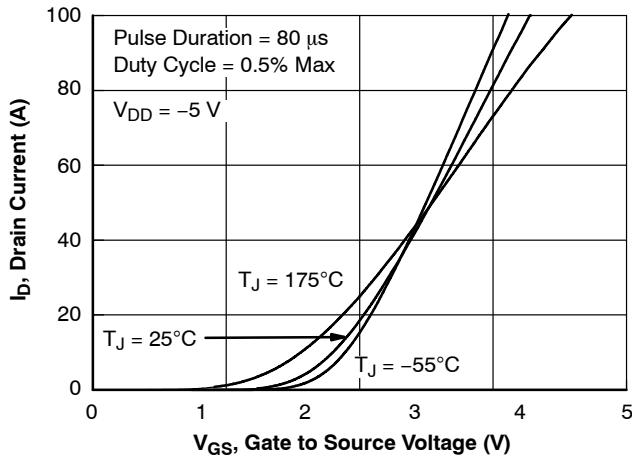


Figure 5. Transfer Characteristics

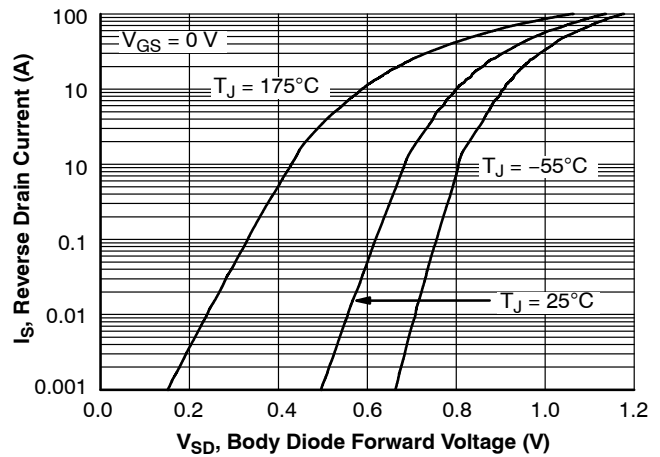


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

TYPICAL CHARACTERISTICS (continued)

( $T_J = 25^\circ\text{C}$  unless otherwise noted)

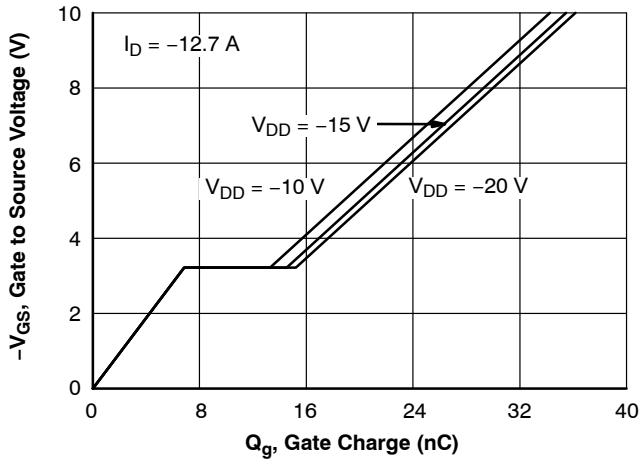


Figure 7. Gate Charge Characteristics

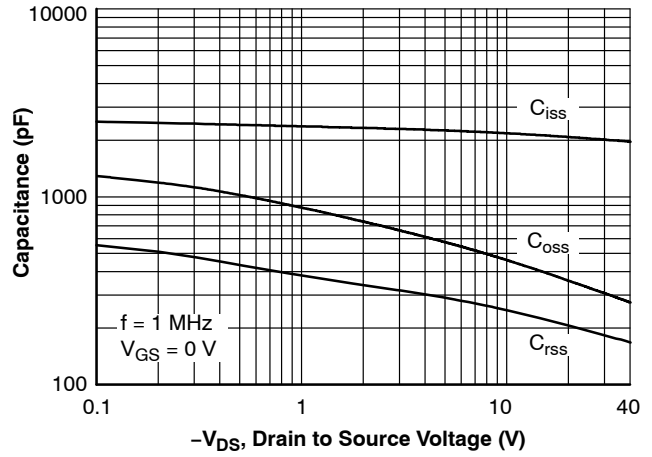


Figure 8. Capacitance vs Drain to Source Voltage

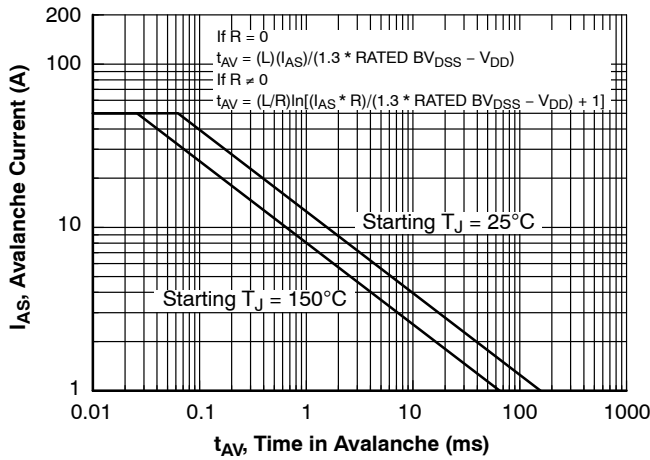


Figure 9. Unclamped Inductive Switching Capability

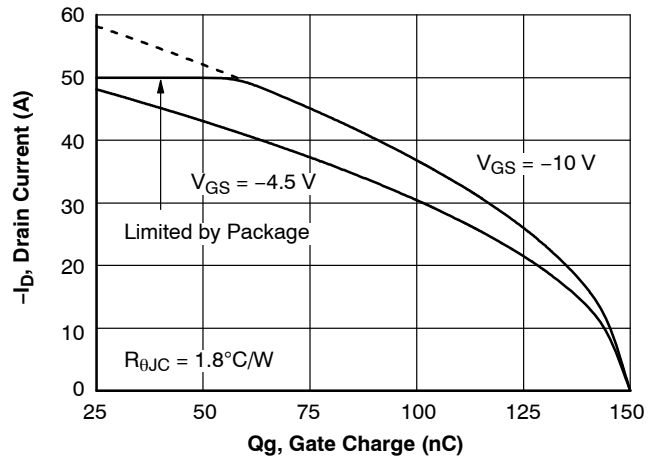


Figure 10. Maximum Continuous Drain Current vs Case Temperature

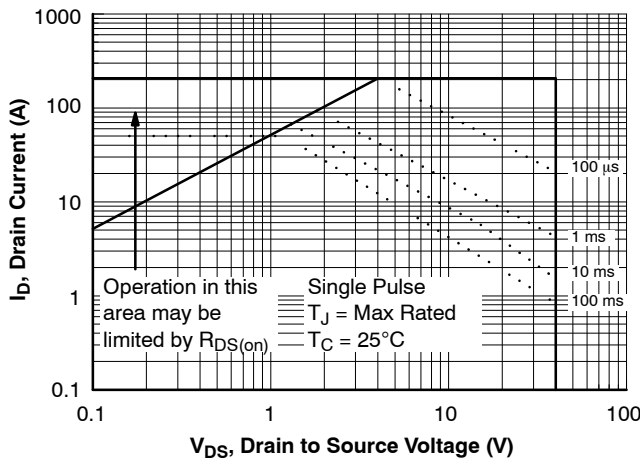


Figure 11. Forward Bias Safe Operating Area

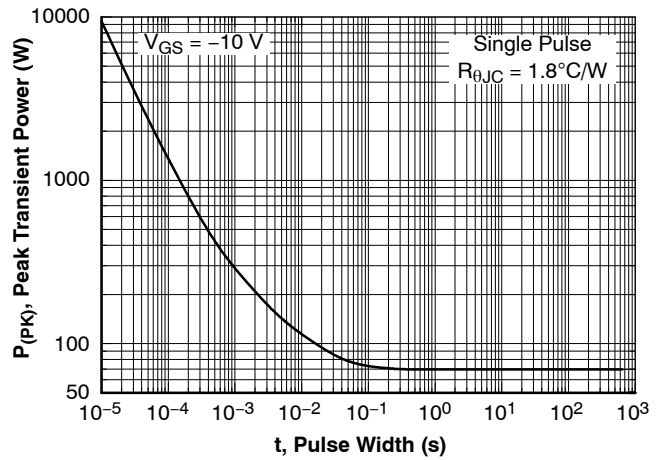


Figure 12. Single Pulse Maximum Power Dissipation

TYPICAL CHARACTERISTICS

( $T_J = 25^\circ\text{C}$  unless otherwise noted)

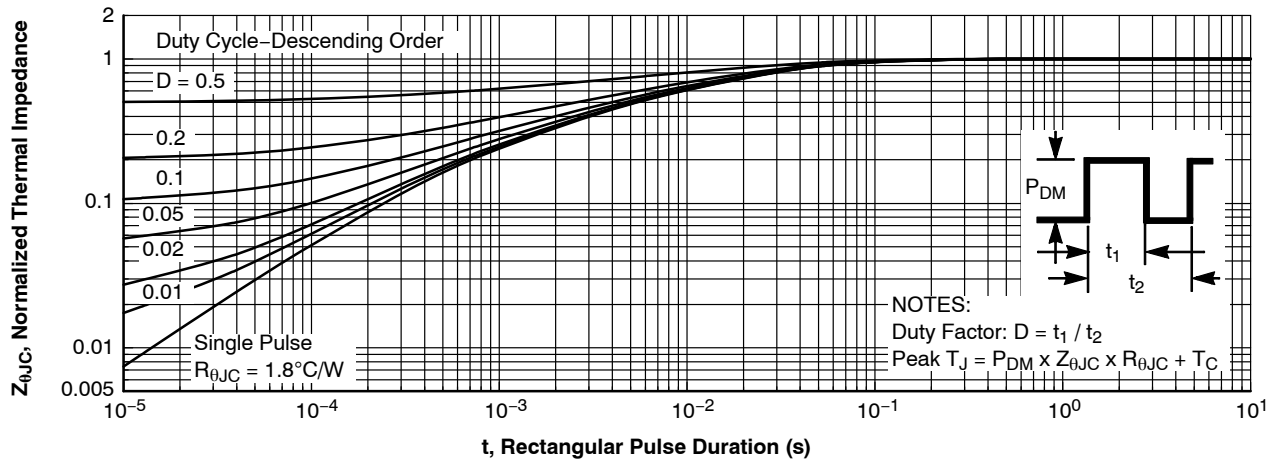


Figure 13. Transient Thermal Response Curve

# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

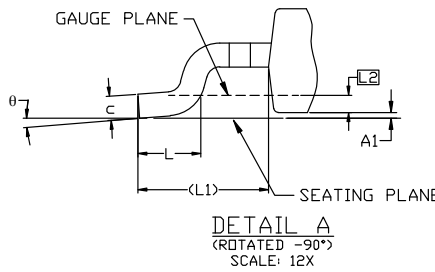


## DPAK3 6.10x6.54x2.29, 4.57P CASE 369AS ISSUE B

DATE 20 DEC 2023



- NOTES: UNLESS OTHERWISE SPECIFIED
- A) THIS PACKAGE CONFORMS TO JEDEC, TO-252, ISSUE F, VARIATION AA.
  - B) ALL DIMENSIONS ARE IN MILLIMETERS.
  - C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2018.
  - D) SUPPLIER DEPENDENT MOLD LOCKING HOLES OR CHAMFERED CORNERS OR EDGE PROTRUSION.
  - E) FOR DIODE PRODUCTS, L4 IS 0.25 MM MAX PLASTIC BODY STUB WITHOUT CENTER LEAD.
  - F) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR EXTRUSIONS.
  - G) LAND PATTERN RECOMMENDATION IS BASED ON IPC7351A STD TD228P991X239-3N.



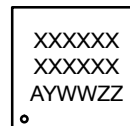
DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	2.18	2.29	2.39
A1	0.00	-	0.127
b	0.64	0.77	0.89
b2	0.76	0.95	1.14
b3	5.21	5.34	5.46
c	0.45	0.53	0.61
c2	0.45	0.52	0.58
D	5.97	6.10	6.22
D1	5.21	---	---
E	6.35	6.54	6.73
E1	4.32	---	---
e	2.286 BSC		
e1	4.572 BSC		
H	9.40	9.91	10.41
L	1.40	1.59	1.78
L1	2.90 REF		
L2	0.51 BSC		
L3	0.89	1.08	1.27
L4	---	---	1.02
θ	0°	---	10°



### LAND PATTERN RECOMMENDATION

\*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERM/D.

### GENERIC MARKING DIAGRAM\*



\*This information is generic. Please refer to device data sheet for actual part marking. Pb-free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

XXXX = Specific Device Code  
 A = Assembly Location  
 Y = Year  
 WW = Work Week  
 ZZ = Assembly Lot Code

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<b>DESCRIPTION:</b>	<b>DPAK3 6.10x6.54x2.29, 4.57P</b>	<b>PAGE 1 OF 1</b>

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