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FDD5N50NZ

N-Channel UniFET™ II MOSFET

500 V, 4 A, 1.5 Ω

Features

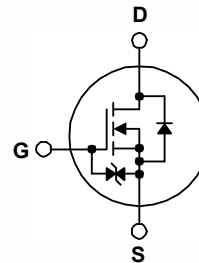
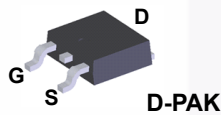
- $R_{DS(on)} = 1.38 \Omega$ (Typ.) @ $V_{GS} = 10 V, I_D = 2 A$
- Low Gate Charge (Typ. 9 nC)
- Low C_{rss} (Typ. 4 pF)
- 100% Avalanche Tested
- Improved dv/dt Capability
- ESD Improved Capability
- RoHS Compliant

Applications

- LCD/LED/PDP TV
- Lighting
- Uninterruptible Power Supply

Description

UniFET™ II MOSFET is Fairchild Semiconductor's high voltage MOSFET family based on advanced planar stripe and DMOS technology. This advanced MOSFET family has the smallest on-state resistance among the planar MOSFET, and also provides superior switching performance and higher avalanche energy strength. In addition, internal gate-source ESD diode allows UniFET™ II MOSFET to withstand over 2kV HBM surge stress. This device family is suitable for switching power converter applications such as power factor correction (PFC), flat panel display (FPD) TV power, ATX and electronic lamp ballasts.



Absolute Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted.

| Symbol | Parameter | FDD5N50NZTM | Unit |
|----------------|--|--|------------------|
| V_{DSS} | Drain to Source Voltage | 500 | V |
| V_{GSS} | Gate to Source Voltage | ±25 | V |
| I_D | Drain Current | - Continuous ($T_C = 25^\circ\text{C}$) | 4 |
| | | - Continuous ($T_C = 100^\circ\text{C}$) | 2.4 |
| I_{DM} | Drain Current | - Pulsed (Note 1) | 16 |
| E_{AS} | Single Pulsed Avalanche Energy | (Note 2) | 304 |
| I_{AR} | Avalanche Current | (Note 1) | 4 |
| E_{AR} | Repetitive Avalanche Energy | (Note 1) | 6.2 |
| dv/dt | Peak Diode Recovery dv/dt | (Note 3) | 10 |
| P_D | Power Dissipation | ($T_C = 25^\circ\text{C}$) | 62 |
| | | - Derate Above 25°C | 0.5 |
| T_J, T_{STG} | Operating and Storage Temperature Range | -55 to +150 | $^\circ\text{C}$ |
| T_L | Maximum Lead Temperature for Soldering, 1/8" from Case for 5 Seconds | 300 | $^\circ\text{C}$ |

Thermal Characteristics

| Symbol | Parameter | FDD5N50NZTM | Unit |
|-----------------|---|-------------|---------------------------|
| $R_{\theta JC}$ | Thermal Resistance, Junction to Case, Max. | 2.0 | $^\circ\text{C}/\text{W}$ |
| $R_{\theta JA}$ | Thermal Resistance, Junction to Ambient, Max. | 90 | |

Package Marking and Ordering Information

| Part Number | Top Mark | Package | Packing Method | Reel Size | Tape Width | Quantity |
|-------------|-----------|---------|----------------|-----------|------------|------------|
| FDD5N50NZTM | FDD5N50NZ | DPAK | Tape and Reel | 330 mm | 16 mm | 2500 units |

Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted.

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|--------|-----------|-----------------|------|------|------|------|
|--------|-----------|-----------------|------|------|------|------|

Off Characteristics

| | | | | | | |
|--------------------------------|---|---|-----|-----|----------|---------------------------|
| BV_{DSS} | Drain to Source Breakdown Voltage | $I_D = 250 \mu\text{A}, V_{GS} = 0 \text{ V}, T_J = 25^\circ\text{C}$ | 500 | - | - | V |
| $\Delta BV_{DSS} / \Delta T_J$ | Breakdown Voltage Temperature Coefficient | $I_D = 250 \mu\text{A}$, Referenced to 25°C | - | 0.5 | - | $\text{V}/^\circ\text{C}$ |
| I_{DSS} | Zero Gate Voltage Drain Current | $V_{DS} = 500 \text{ V}, V_{GS} = 0 \text{ V}$ | - | - | 1 | μA |
| | | $V_{DS} = 400 \text{ V}, T_C = 125^\circ\text{C}$ | - | - | 10 | |
| I_{GSS} | Gate to Body Leakage Current | $V_{GS} = \pm 25 \text{ V}, V_{DS} = 0 \text{ V}$ | - | - | ± 10 | μA |

On Characteristics

| | | | | | | |
|--------------|--------------------------------------|--|-----|------|-----|----------|
| $V_{GS(th)}$ | Gate Threshold Voltage | $V_{GS} = V_{DS}, I_D = 250 \mu\text{A}$ | 3.0 | - | 5.0 | V |
| $R_{DS(on)}$ | Static Drain to Source On Resistance | $V_{GS} = 10 \text{ V}, I_D = 2 \text{ A}$ | - | 1.38 | 1.5 | Ω |
| g_{FS} | Forward Transconductance | $V_{DS} = 20 \text{ V}, I_D = 2 \text{ A}$ | - | 3.54 | - | S |

Dynamic Characteristics

| | | | | | | |
|--------------|-------------------------------|--|----------|-----|-----|----|
| C_{iss} | Input Capacitance | $V_{DS} = 25 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$ | - | 330 | 440 | pF |
| C_{oss} | Output Capacitance | | - | 50 | 70 | pF |
| C_{rss} | Reverse Transfer Capacitance | | - | 4 | 6 | pF |
| $Q_{g(tot)}$ | Total Gate Charge at 10V | $V_{DS} = 400 \text{ V}, I_D = 4 \text{ A}, V_{GS} = 10 \text{ V}$ | - | 9 | 12 | nC |
| Q_{gs} | Gate to Source Gate Charge | | - | 2 | - | nC |
| Q_{gd} | Gate to Drain "Miller" Charge | | (Note 4) | - | 4 | - |

Switching Characteristics

| | | | | | | |
|--------------|---------------------|---|----------|----|----|----|
| $t_{d(on)}$ | Turn-On Delay Time | $V_{DD} = 250 \text{ V}, I_D = 4 \text{ A}, V_{GS} = 10 \text{ V}, R_G = 25 \Omega$ | - | 12 | 35 | ns |
| t_r | Turn-On Rise Time | | - | 22 | 55 | ns |
| $t_{d(off)}$ | Turn-Off Delay Time | | - | 28 | 65 | ns |
| t_f | Turn-Off Fall Time | | (Note 4) | - | 21 | 50 |

Drain-Source Diode Characteristics

| | | | | | | |
|----------|--|--|---|-----|-----|---------------|
| I_S | Maximum Continuous Drain to Source Diode Forward Current | - | - | 4 | A | |
| I_{SM} | Maximum Pulsed Drain to Source Diode Forward Current | - | - | 16 | A | |
| V_{SD} | Drain to Source Diode Forward Voltage | $V_{GS} = 0 \text{ V}, I_{SD} = 4 \text{ A}$ | - | - | 1.4 | V |
| t_{rr} | Reverse Recovery Time | $V_{GS} = 0 \text{ V}, I_{SD} = 4 \text{ A}$ | - | 210 | - | ns |
| Q_{rr} | Reverse Recovery Charge | $di_F/dt = 100 \text{ A}/\mu\text{s}$ | - | 1.1 | - | μC |

Notes:

1. Repetitive rating: pulse-width limited by maximum junction temperature.
2. $L = 38 \text{ mH}, I_{AS} = 4 \text{ A}, V_{DD} = 50 \text{ V}, R_G = 25 \Omega$, starting $T_J = 25^\circ\text{C}$.
3. $I_{SD} \leq 4 \text{ A}, di/dt \leq 200 \text{ A}/\mu\text{s}, V_{DD} \leq BV_{DSS}$, starting $T_J = 25^\circ\text{C}$.
4. Essentially independent of operating temperature typical characteristics.

Typical Performance Characteristics

Figure 1. On-Region Characteristics

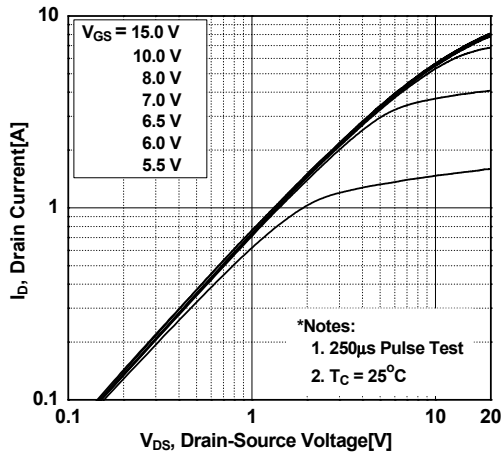


Figure 2. Transfer Characteristics

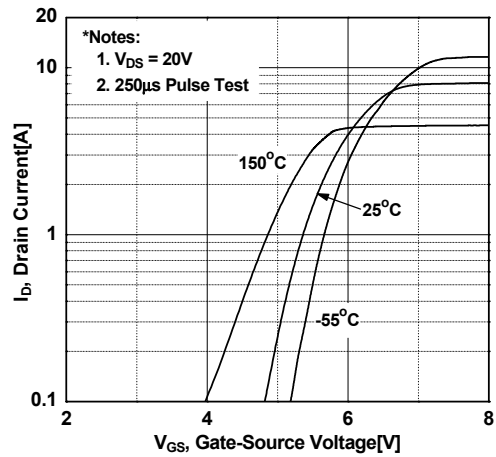


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

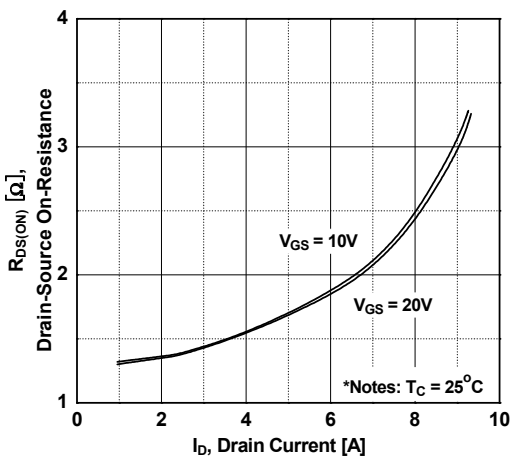


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

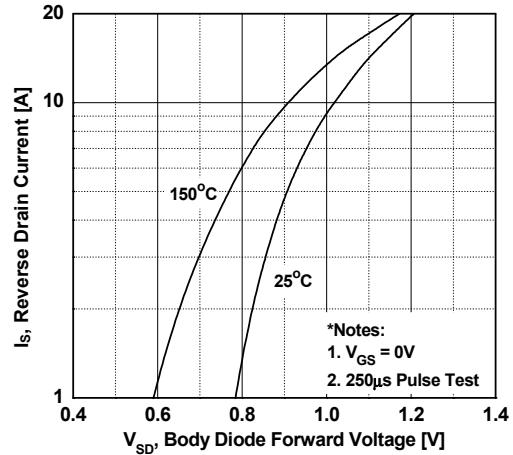


Figure 5. Capacitance Characteristics

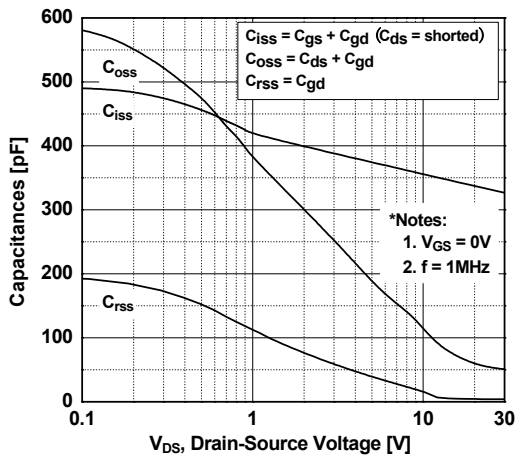
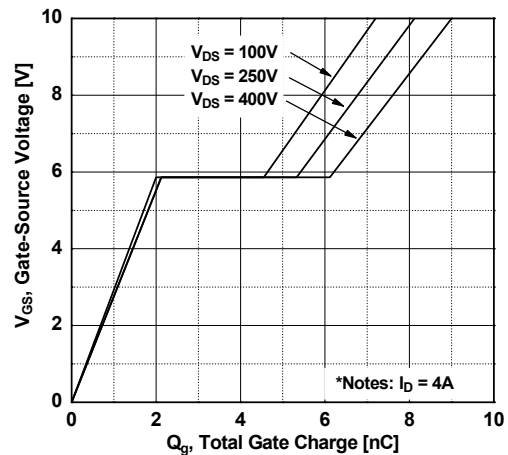


Figure 6. Gate Charge Characteristics



Typical Performance Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

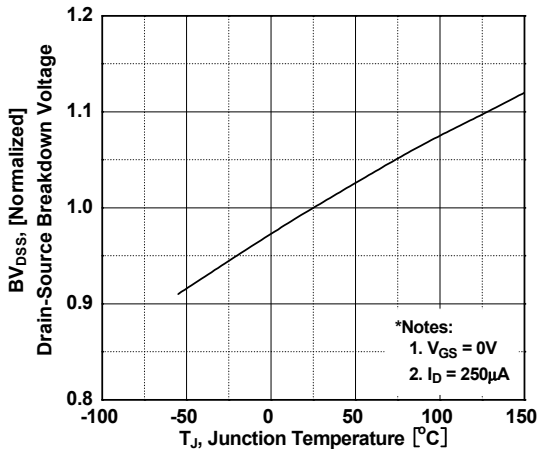


Figure 8. On-Resistance Variation vs. Temperature

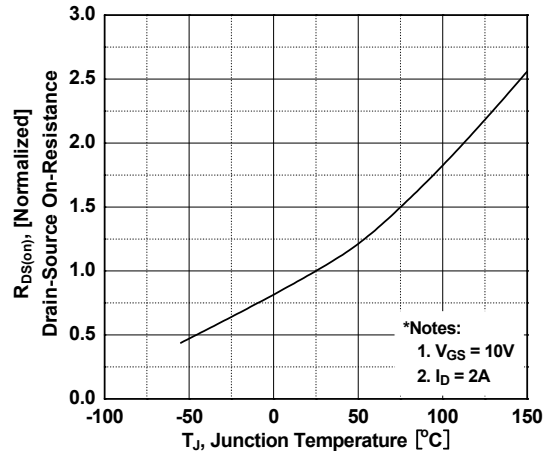


Figure 9. Maximum Safe Operating Area

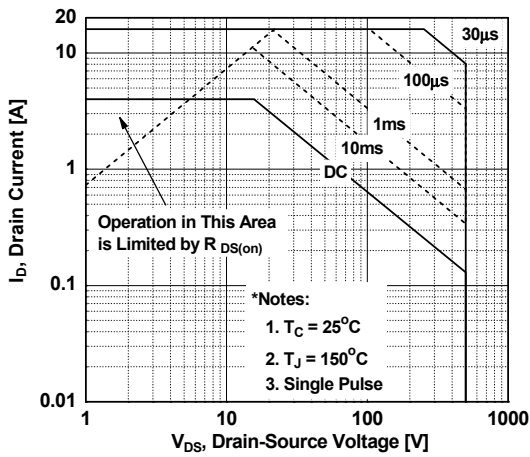


Figure 10. Maximum Drain Current vs. Case Temperature

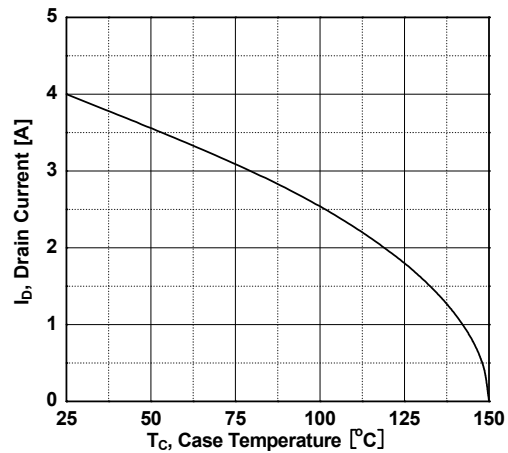


Figure 11. Transient Thermal Response Curve

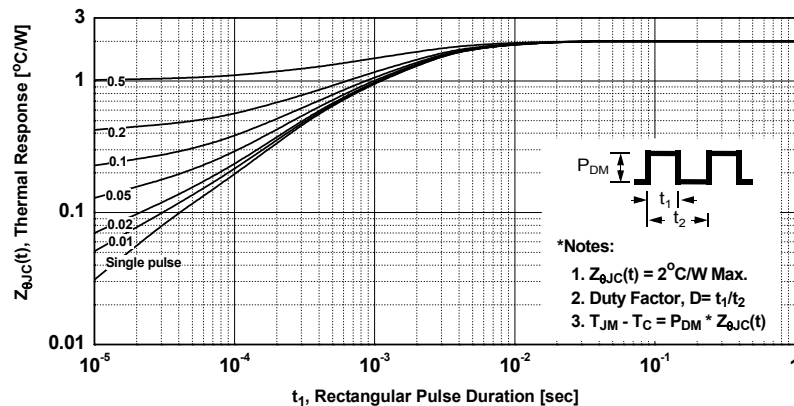




Figure 12. Gate Charge Test Circuit & Waveform



Figure 13. Resistive Switching Test Circuit & Waveforms

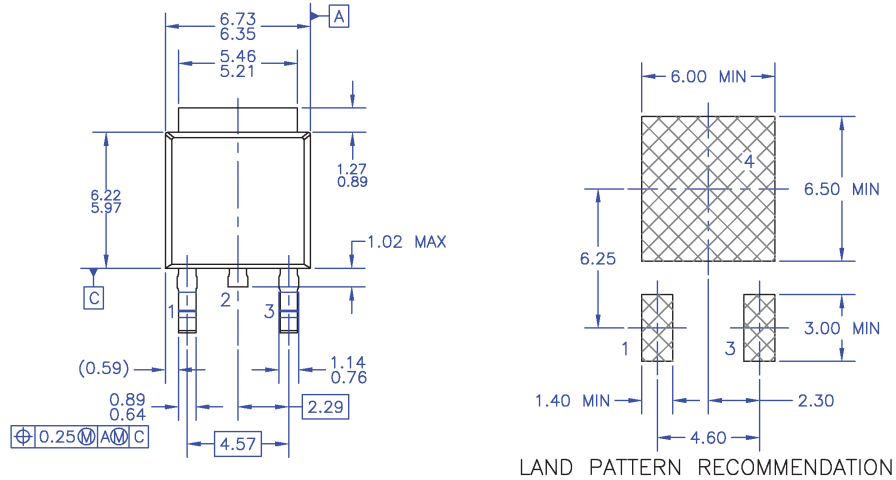


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms



Figure 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms

Mechanical Dimensions



- NOTES: UNLESS OTHERWISE SPECIFIED
- A) THIS PACKAGE CONFORMS TO JEDEC, TO-252, ISSUE C, VARIATION AA.
 - B) ALL DIMENSIONS ARE IN MILLIMETERS.
 - C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
 - D) HEAT SINK TOP EDGE COULD BE IN CHAMFERED CORNERS OR EDGE PROTRUSION.
 - E) PRESENCE OF TRIMMED CENTER LEAD IS OPTIONAL.
 - F) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR EXTRUSIONS.
 - G) LAND PATTERN RECOMMENDATION IS BASED ON IPC7351A STD TO220P1003X238-3N.
 - H) DRAWING NUMBER AND REVISION: MKT-T0252A03REV8

Figure 16. TO252 (D-PAK), Molded, 3-Lead, Option AA&AB

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