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March 2015

FDD6680AS

# FDD6680AS

## 30V N-Channel PowerTrench<sup>®</sup> SyncFET<sup>™</sup>

### General Description

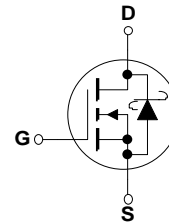
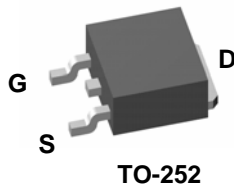
The FDD6680AS is designed to replace a single MOSFET and Schottky diode in synchronous DC:DC power supplies. This 30V MOSFET is designed to maximize power conversion efficiency, providing a low  $R_{DS(ON)}$  and low gate charge. The FDD6680AS includes an integrated Schottky diode using Fairchild's monolithic SyncFET technology. The performance of the FDD6680AS as the low-side switch in a synchronous rectifier is indistinguishable from the performance of the FDD6680A in parallel with a Schottky diode.

### Applications

- DC/DC converter
- Low side notebook

### Features

- 55 A, 30 V  $R_{DS(ON)}$  max= 10.5 m $\Omega$  @  $V_{GS} = 10$  V  
 $R_{DS(ON)}$  max= 13.0 m $\Omega$  @  $V_{GS} = 4.5$  V
- Includes SyncFET Schottky body diode
- Low gate charge (21nC typical)
- High performance trench technology for extremely low  $R_{DS(ON)}$
- High power and current handling capability



### Absolute Maximum Ratings $T_A=25^{\circ}\text{C}$ unless otherwise noted

Symbol	Parameter	Ratings	Unit
$V_{DSS}$	Drain-Source Voltage	30	V
$V_{GSS}$	Gate-Source Voltage	$\pm 20$	V
$I_D$	Drain Current – Continuous (Note 3)	55	A
	– Pulsed (Note 1a)	100	
$P_D$	Power Dissipation (Note 1)	60	W
		3.1	
		1.3	
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to +150	$^{\circ}\text{C}$

### Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Note 1)	2.1	$^{\circ}\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a)	40	$^{\circ}\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1b)	96	$^{\circ}\text{C}/\text{W}$

### Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
FDD6680AS	FDD6680AS	13"	16mm	2500 units

**Electrical Characteristics** $T_A = 25^\circ\text{C}$  unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
<b>Drain-Source Avalanche Ratings (Note 2)</b>						
$W_{DSS}$	Drain-Source Avalanche Energy	Single Pulse, $V_{DD} = 15\text{ V}$ , $I_D = 13.5\text{ A}$		54	205	mJ
$I_{AR}$	Drain-Source Avalanche Current				13.5	A
<b>Off Characteristics</b>						
$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}$ , $I_D = 1\text{ mA}$	30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 1\text{ mA}$ , Referenced to $25^\circ\text{C}$		29		mV/ $^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 24\text{ V}$ , $V_{GS} = 0\text{ V}$			500	$\mu\text{A}$
$I_{GSS}$	Gate-Body Leakage	$V_{GS} = \pm 20\text{ V}$ , $V_{DS} = 0\text{ V}$			$\pm 100$	nA
<b>On Characteristics (Note 2)</b>						
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$ , $I_D = 1\text{ mA}$	1	1.4	3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	$I_D = 1\text{ mA}$ , Referenced to $25^\circ\text{C}$		-3		mV/ $^\circ\text{C}$
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 10\text{ V}$ , $I_D = 12.5\text{ A}$ $V_{GS} = 4.5\text{ V}$ , $I_D = 10\text{ A}$ $V_{GS} = 10\text{ V}$ , $I_D = 12.5\text{ A}$ , $T_J = 125^\circ\text{C}$		8.6 10.3 12.5	10.5 13.0 16.0	m $\Omega$
$I_{D(on)}$	On-State Drain Current	$V_{GS} = 10\text{ V}$ , $V_{DS} = 5\text{ V}$	50			A
$g_{FS}$	Forward Transconductance	$V_{DS} = 15\text{ V}$ , $I_D = 12.5\text{ A}$		44		S
<b>Dynamic Characteristics</b>						
$C_{iss}$	Input Capacitance	$V_{DS} = 15\text{ V}$ , $V_{GS} = 0\text{ V}$ , $f = 1.0\text{ MHz}$		1200		pF
$C_{oss}$	Output Capacitance			350		pF
$C_{rss}$	Reverse Transfer Capacitance			120		pF
$R_G$	Gate Resistance	$V_{GS} = 15\text{ mV}$ , $f = 1.0\text{ MHz}$		1.6		$\Omega$
<b>Switching Characteristics (Note 2)</b>						
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 15\text{ V}$ , $I_D = 1\text{ A}$ , $V_{GS} = 10\text{ V}$ , $R_{GEN} = 6\ \Omega$		10	20	ns
$t_r$	Turn-On Rise Time			6	12	ns
$t_{d(off)}$	Turn-Off Delay Time			28	45	ns
$t_f$	Turn-Off Fall Time			12	22	ns
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 15\text{ V}$ , $I_D = 1\text{ A}$ , $V_{GS} = 4.5\text{ V}$ , $R_{GEN} = 6\ \Omega$		14	25	ns
$t_r$	Turn-On Rise Time			13	23	ns
$t_{d(off)}$	Turn-Off Delay Time			20	32	ns
$t_f$	Turn-Off Fall Time			11	20	ns
$Q_g(TOT)$	Total Gate Charge at $V_{gs}=10\text{V}$	$V_{DD} = 15\text{ V}$ , $I_D = 12.5\text{ A}$		21	29	nC
$Q_g$	Total Gate Charge at $V_{gs}=5\text{V}$			11	15	nC
$Q_{gs}$	Gate-Source Charge			3		nC
$Q_{gd}$	Gate-Drain Charge			4		nC
<b>Drain-Source Diode Characteristics and Maximum Ratings</b>						
$I_S$	Maximum Continuous Drain-Source Diode Forward Current				4.4	A
$V_{SD}$	Drain-Source Diode Forward Voltage	$V_{GS} = 0\text{ V}$ , $I_S = 4.4\text{ A}$ (Note 2) $V_{GS} = 0\text{ V}$ , $I_S = 7\text{ A}$ (Note 2)		0.5 0.6	0.7	V
$t_{rr}$	Diode Reverse Recovery Time	$I_F = 12.5\text{ A}$ , $dI_F/dt = 300\text{ A}/\mu\text{s}$ (Note 3)		17		nS
$Q_{rr}$	Diode Reverse Recovery Charge			11		nC

## Electrical Characteristics

$T_A = 25^\circ\text{C}$  unless otherwise noted

**Notes:**

1.  $R_{\theta JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.



a)  $R_{\theta JA} = 40^\circ\text{C/W}$  when mounted on a  $1\text{in}^2$  pad of 2 oz copper



b)  $R_{\theta JA} = 96^\circ\text{C/W}$  when mounted on a minimum pad.

Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width < 300 $\mu\text{s}$ , Duty Cycle < 2.0%

3. Maximum current is calculated as:
- $$\sqrt{\frac{P_D}{R_{DS(ON)}}}$$

where  $P_D$  is maximum power dissipation at  $T_C = 25^\circ\text{C}$  and  $R_{DS(on)}$  is at  $T_{J(max)}$  and  $V_{GS} = 10\text{V}$ . Package current limitation is 21A

## Typical Characteristics

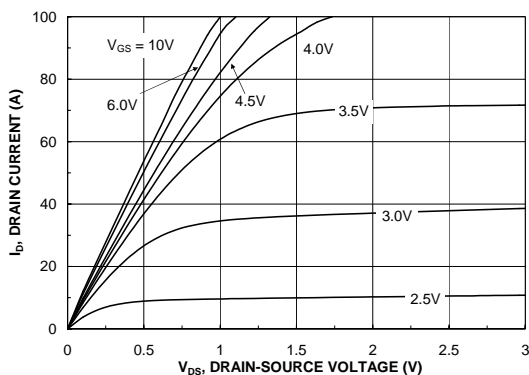


Figure 1. On-Region Characteristics.

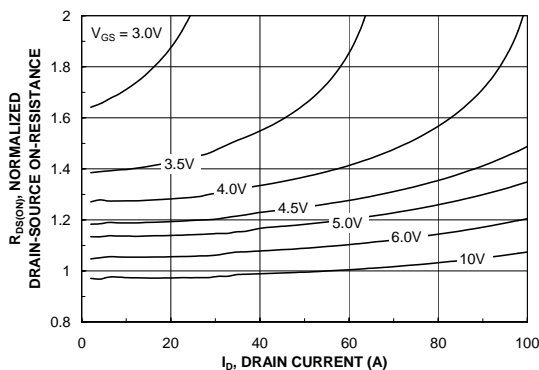


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

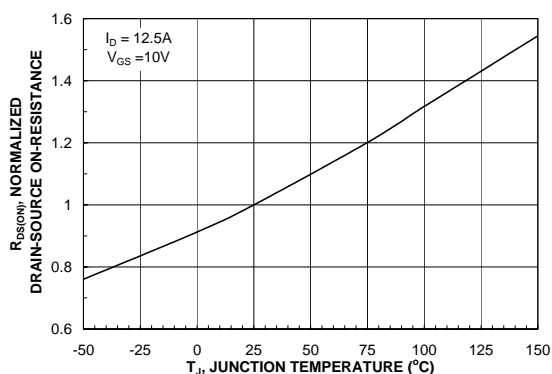


Figure 3. On-Resistance Variation with Temperature.

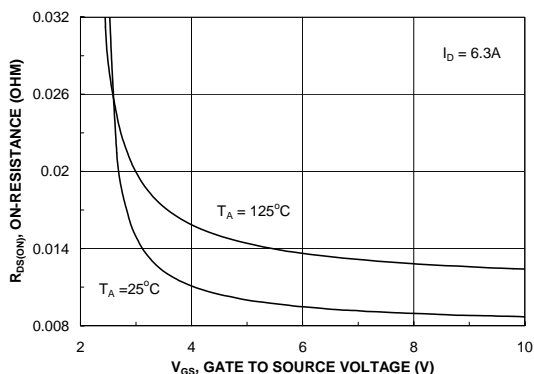


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

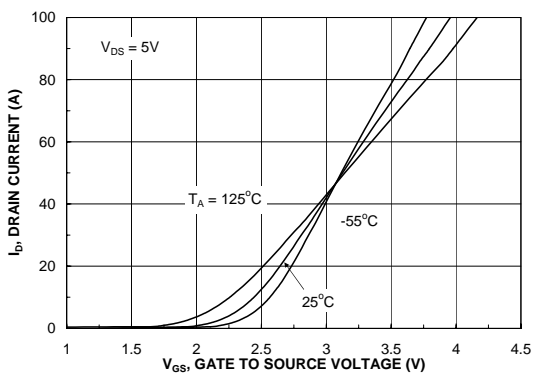


Figure 5. Transfer Characteristics.

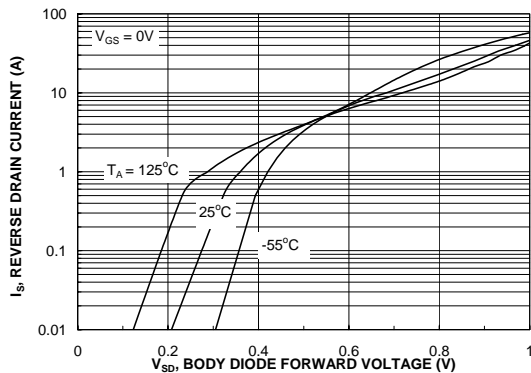


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics (continued)

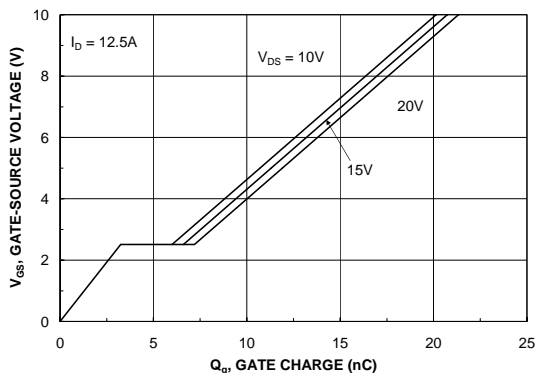


Figure 7. Gate Charge Characteristics.

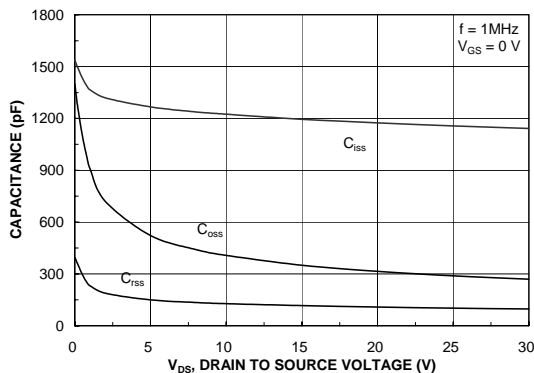


Figure 8. Capacitance Characteristics.

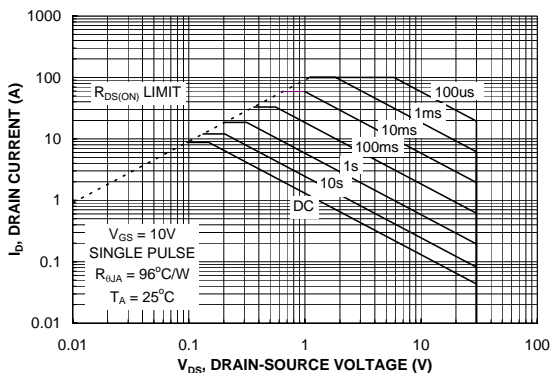


Figure 9. Maximum Safe Operating Area.

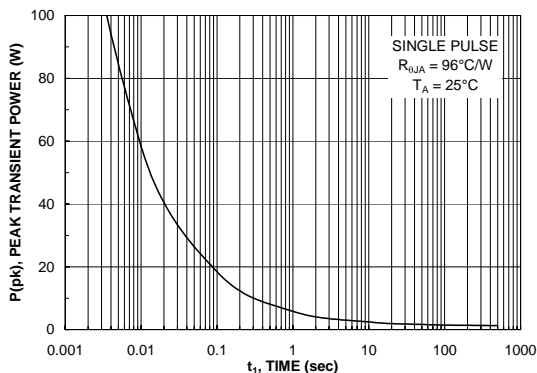


Figure 10. Single Pulse Maximum Power Dissipation.

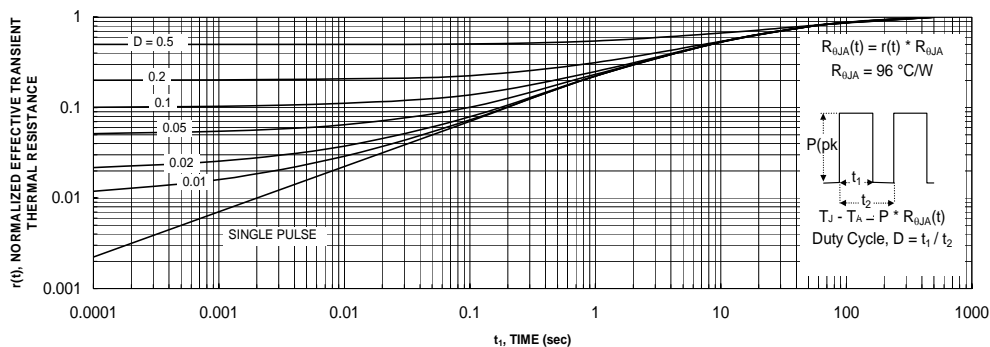


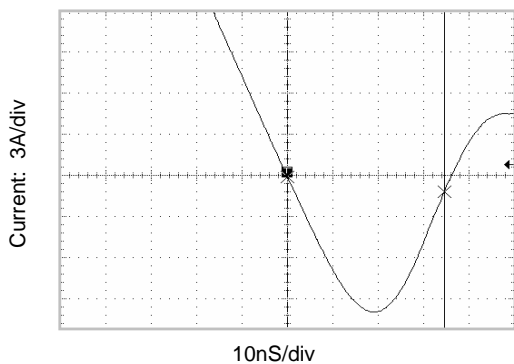
Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1b. Transient thermal response will change depending on the circuit board design.

**Typical Characteristics** (continued)

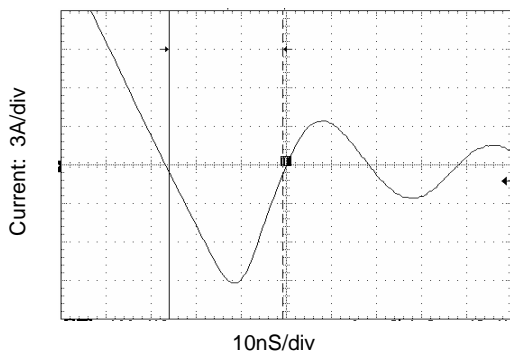
**SyncFET Schottky Body Diode Characteristics**

Fairchild's SyncFET process embeds a Schottky diode in parallel with PowerTrench MOSFET. This diode exhibits similar characteristics to a discrete external Schottky diode in parallel with a MOSFET. Figure 12 shows the reverse recovery characteristic of the FDD6680AS.



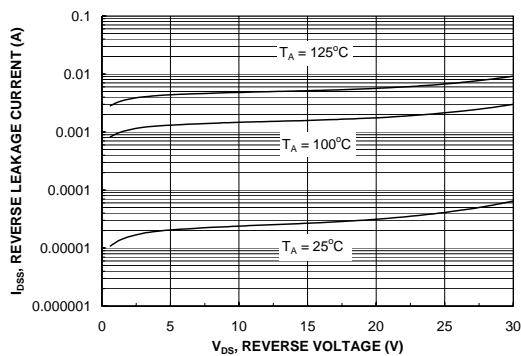
**Figure 12. FDD6680AS SyncFET body diode reverse recovery characteris**

For comparison purposes, Figure 13 shows the reverse recovery characteristics of the body diode of an equivalent size MOSFET produced without SyncFET (FDD6680).



**Figure 13. Non-SyncFET (FDD6680) body diode reverse recovery characteristic.**

Schottky barrier diodes exhibit significant leakage at high temperature and high reverse voltage. This will increase the power in the device.



**Figure 14. SyncFET body diode reverse leakage versus drain-source voltage and temperature.**

Typical Characteristics

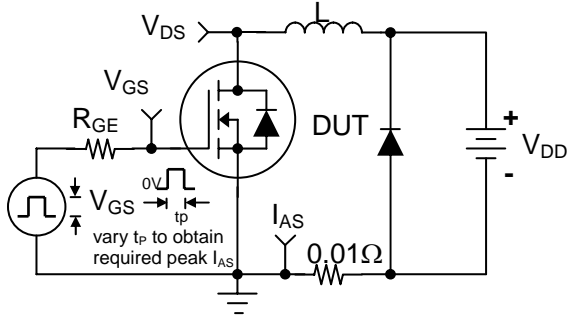


Figure 12. Unclamped Inductive Load Test Circuit

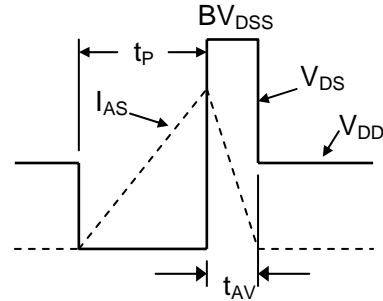


Figure 13. Unclamped Inductive Waveforms

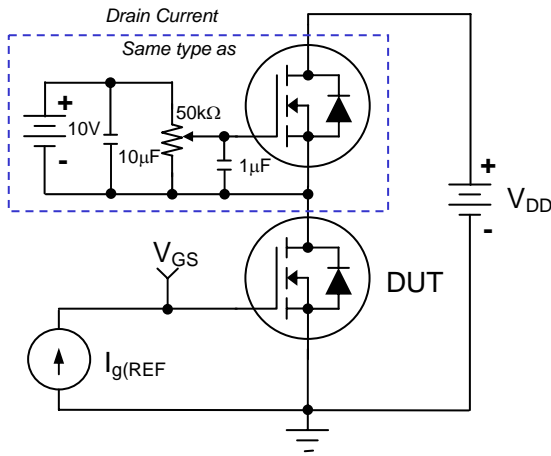


Figure 14. Gate Charge Test Circuit

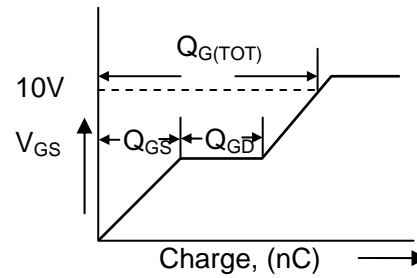


Figure 15. Gate Charge Waveform

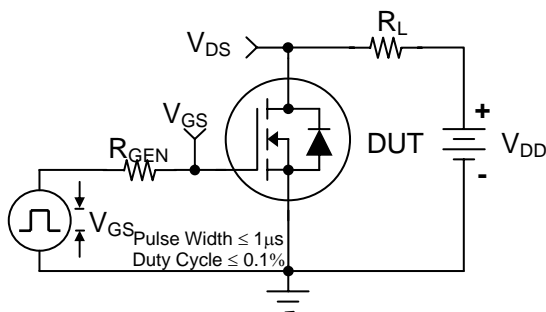


Figure 16. Switching Time Test Circuit

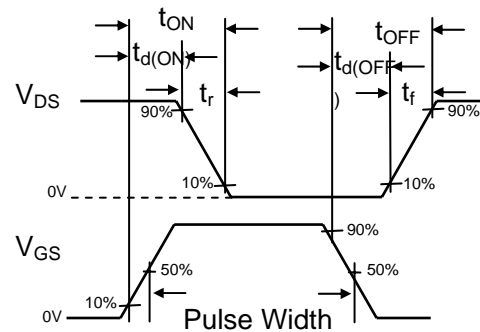
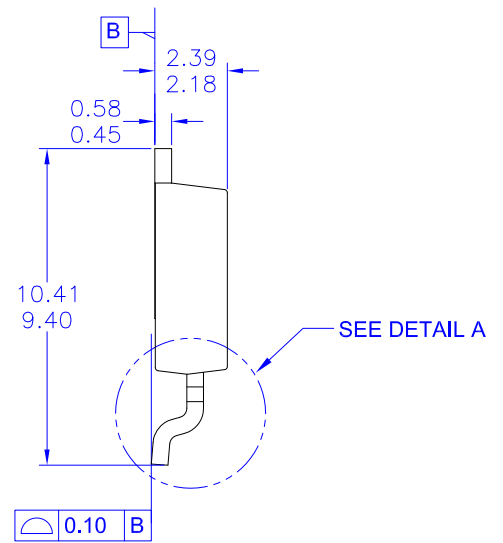
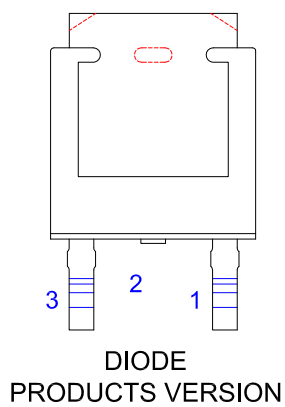
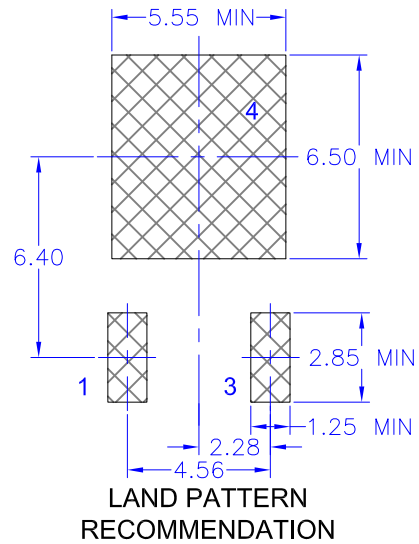


Figure 17. Switching Time Waveforms





NOTES: UNLESS OTHERWISE SPECIFIED  
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F) DIMENSIONS ARE EXCLUSIVE OF BURS, MOLD FLASH AND TIE BAR EXTRUSIONS.

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