

Digital FET, Dual N & P Channel

FDG6320C

General Description

These dual N & P-Channel logic level enhancement mode field effect transistors are produced using ON Semiconductor's proprietary, high cell density, DMOS technology, this very high density process is especially tailored to minimize on-state resistance. This device has been designed especially for low voltage applications as a replacement for bipolar digital transistors and small signal MOSFETS. Since bias resistors are not required, this dual digital FET can replace several different digital transistors, with different bias resistor values.

Features

- N-Ch 0.22 A, 0.25 V
 - ♦ $R_{DS(ON)} = 4.0 \Omega @ V_{GS} = 4.5 V$
 - ♦ $R_{DS(ON)} = 5.0 \Omega @ V_{GS} = 2.7 V$
- P-Ch -0.14 A, -25 V
 - ♦ $R_{DS(ON)} = 10 \Omega @ V_{GS} = -4.5 V$
 - ♦ $R_{DS(ON)} = 13 \Omega @ V_{GS} = -2.7 V$
- Very Small Package Outline SC70-6
- Very Low Level Gate Drive Requirements Allowing Direct Operation in 3 V Circuits ($V_{GS(th)} < 1.5 V$)
- Gate-Source Zener for ESD Ruggedness ($>6 kV$ Human Body Model)
- These Devices are Pb-Free and are RoHS Compliant

ABSOLUTE MAXIMUM RATINGS

 ($T_A = 25^\circ C$ unless otherwise noted)

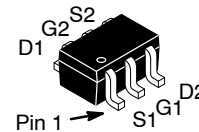
Symbol	Parameter	N-Channel	P-Channel	Units
V_{DSS}	Drain-Source Voltage	25	-25	V
V_{GSS}	Gate-Source Voltage	8	-8	V
I_D	Drain Current	Continuous	-0.22	A
		Pulsed	0.65	
P_D	Maximum Power Dissipation (Note 1)	0.3		W
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to 150		$^\circ C$
ESD	Electrostatic Discharge Rating MIL-STD-883D Human Body Model (100 pF / 1500 Ω)	6		kV

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.



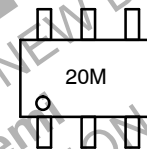
ON Semiconductor®

www.onsemi.com



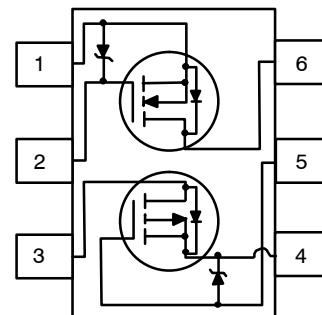
SC-88/SC70-6/SOT-363
CASE 419B-02

MARKING DIAGRAM



20 = Specific Device Code
M = Assembly Operation Month

PIN CONNECTIONS



ORDERING INFORMATION

See detailed ordering and shipping information on page 8 of this data sheet.

FDG6320C

THERMAL CHARACTERISTICS

Symbol	Parameter	Ratings	Unit
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1)	415	$^{\circ}\text{C/W}$

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design. $R_{\theta JA} = 415^{\circ}\text{C/W}$ on minimum pad mounting on FR-4 board in still air.

ELECTRICAL CHARACTERISTICS ($T_A = 25^{\circ}\text{C}$ unless otherwise noted)

Symbol	Parameter	Conditions	Type	Min	Typ	Max	Unit
--------	-----------	------------	------	-----	-----	-----	------

OFF CHARACTERISTICS

BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	N-Ch	25	–	–	V
		$V_{GS} = 0\text{ V}, I_D = -250\text{ }\mu\text{A}$	P-Ch	-25	–	–	
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$, Referenced to 25°C	N-Ch	–	25	–	$\text{mV}/^{\circ}\text{C}$
		$I_D = -250\text{ }\mu\text{A}$, Referenced to 25°C	P-Ch	–	-19	–	
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 20\text{ V}, V_{GS} = 0\text{ V}$	N-Ch	–	–	1	μA
		$V_{DS} = 20\text{ V}, V_{GS} = 0\text{ V}, T_J = 55^{\circ}\text{C}$		–	–	10	
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = -20\text{ V}, V_{GS} = 0\text{ V}$	P-Ch	–	–	-1	μA
		$V_{DS} = -20\text{ V}, V_{GS} = 0\text{ V}, T_J = 55^{\circ}\text{C}$		–	–	-10	
I_{GSS}	Gate-Body Leakage Current	$V_{GS} = 8\text{ V}, V_{DS} = 0\text{ V}$	N-Ch	–	–	100	nA
		$V_{GS} = -8\text{ V}, V_{DS} = 0\text{ V}$	P-Ch	–	–	-100	

ON CHARACTERISTICS (Note 2)

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	N-Ch	0.65	0.85	1.5	V
		$V_{DS} = V_{GS}, I_D = -250\text{ }\mu\text{A}$	P-Ch	-0.65	-0.82	-1.5	
$\Delta V_{GS(th)} / \Delta T_J$	Gate Threshold Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$, Referenced to 25°C	N-Ch	–	-2.1	–	$\text{mV}/^{\circ}\text{C}$
		$I_D = -250\text{ }\mu\text{A}$, Referenced to 25°C	P-Ch	–	2.1	–	
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 4.5\text{ V}, I_D = 0.22\text{ A}$	N-Ch	–	2.6	4	Ω
		$V_{GS} = 4.5\text{ V}, I_D = 0.22\text{ A}, T_J = 125^{\circ}\text{C}$		–	5.3	7	
		$V_{GS} = 2.7\text{ V}, I_D = 0.19\text{ A}$		–	3.7	5	
		$V_{GS} = -4.5\text{ V}, I_D = -0.14\text{ A}$	P-Ch	–	7.3	10	
		$V_{GS} = -4.5\text{ V}, I_D = -0.14\text{ A}, T_J = 125^{\circ}\text{C}$		–	11	17	
		$V_{GS} = -2.7\text{ V}, I_D = -0.05\text{ A}$		–	10.4	13	
$I_{D(on)}$	On-State Drain Current	$V_{GS} = 4.5\text{ V}, V_{DS} = 5\text{ V}$	N-Ch	0.22	–	–	A
		$V_{GS} = -4.5\text{ V}, V_{DS} = -5\text{ V}$	P-Ch	-0.14	–	–	
g_{FS}	Forward Transconductance	$V_{DS} = 5\text{ V}, I_D = 0.22\text{ A}$	N-Ch	–	0.2	–	S
		$V_{DS} = -5\text{ V}, I_D = -0.14\text{ A}$	P-Ch	–	0.12	–	

DYNAMIC CHARACTERISTICS

C_{iss}	Input Capacitance	N-Channel $V_{DS} = 10\text{ V}, V_{GS} = 0\text{ V}, f = 1.0\text{ MHz}$ P-Channel $V_{DS} = -10\text{ V}, V_{GS} = 0\text{ V}, f = 1.0\text{ MHz}$	N-Ch	–	9.5	–	pF
			P-Ch	–	12	–	
C_{oss}	Output Capacitance		N-Ch	–	6	–	
			P-Ch	–	7	–	
C_{rss}	Reverse Transfer Capacitance		N-Ch	–	1.3	–	
			P-Ch	–	1.5	–	

FDG6320C

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise noted) (continued)

Symbol	Parameter	Conditions	Type	Min	Typ	Max	Unit
--------	-----------	------------	------	-----	-----	-----	------

SWITCHING CHARACTERISTICS (Note 2)

$t_{D(on)}$	Turn-On Delay Time	N-Channel $V_{DD} = 5\text{ V}$, $I_D = 0.5\text{ A}$, $V_{GS} = 4.5\text{ V}$, $R_{GEN} = 50\ \Omega$ P-Channel $V_{DD} = -5\text{ V}$, $I_D = -0.5\text{ A}$, $V_{GS} = -4.5\text{ V}$, $R_{GEN} = 50\ \Omega$	N-Ch	–	5	12	ns
			P-Ch	–	5	12	
t_r	Turn-On Rise Time		N-Ch	–	4.5	10	ns
			P-Ch	–	8	16	
$t_{D(off)}$	Turn-Off Delay Time		N-Ch	–	4	8	ns
			P-Ch	–	9	18	
t_f	Turn-Off Fall Time		N-Ch	–	3.2	7	ns
			P-Ch	–	5	12	
Q_g	Total Gate Charge	N-Channel $V_{DS} = 5\text{ V}$, $I_D = 0.22\text{ A}$, $V_{GS} = 4.5\text{ V}$ P-Channel $V_{DS} = -5\text{ V}$, $I_D = -0.14\text{ A}$, $V_{GS} = -4.5\text{ V}$	N-Ch	–	0.29	0.4	nC
			P-Ch	–	0.22	0.31	
Q_{gs}	Gate-Source Charge		N-Ch	–	0.12	–	nC
			P-Ch	–	0.12	–	
Q_{gd}	Gate-Drain Charge		N-Ch	–	0.03	–	nC
			P-Ch	–	0.05	–	

DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS

I_S	Maximum Continuous Source Current		N-Ch	–	–	0.25	A
			P-Ch	–	–	–0.25	
V_{SD}	Drain-Source Diode Forward Voltage	$V_{GS} = 0\text{ V}$, $I_S = 0.5\text{ A}$ (Note 2)	N-Ch	–	0.8	1.2	V
		$V_{GS} = 0\text{ V}$, $I_S = -0.5\text{ A}$ (Note 2)	P-Ch	–	–0.8	–1.2	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Pulse Test: Pulse Width $\leq 300\ \mu\text{s}$, Duty Cycle $\leq 2.0\%$

TYPICAL PERFORMANCE CHARACTERISTICS: N-CHANNEL

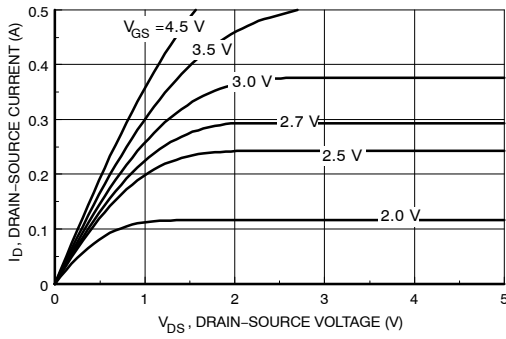


Figure 1. On-Region Characteristics

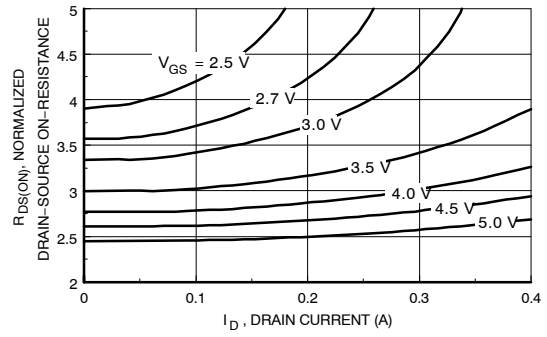


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage

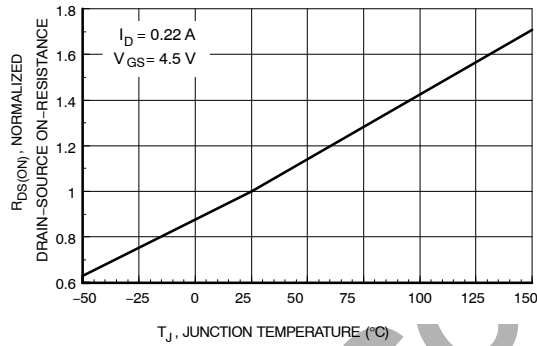


Figure 3. On-Resistance Variation with Temperature

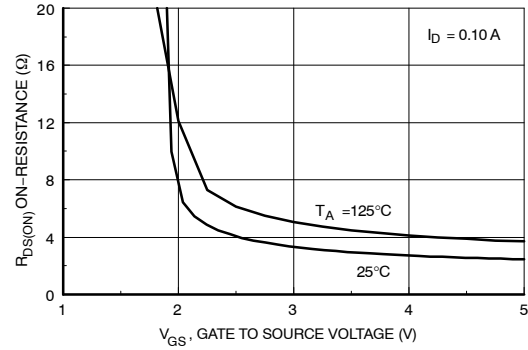


Figure 4. On-Resistance Variation with Gate-to-Source Voltage

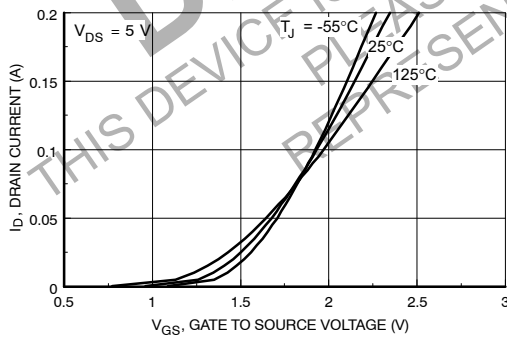


Figure 5. Transfer Characteristics

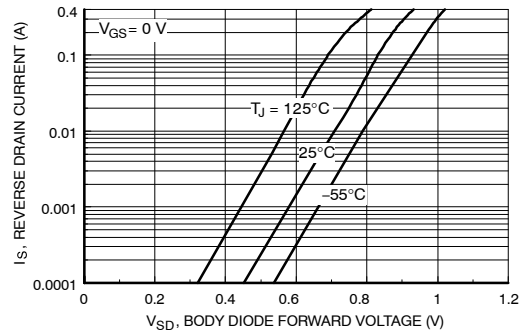


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature

TYPICAL PERFORMANCE CHARACTERISTICS: N-CHANNEL (continued)

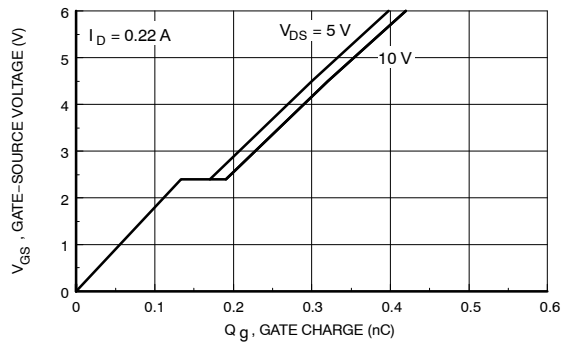


Figure 7. Gate Charge Characteristics

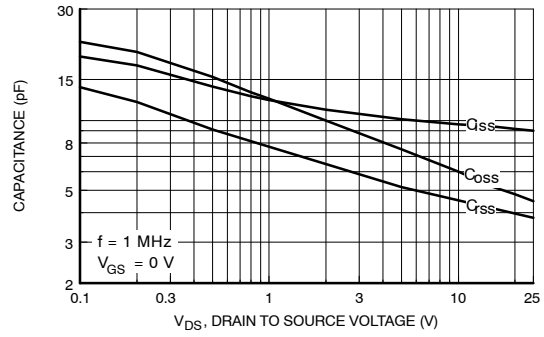


Figure 8. Capacitance Characteristics

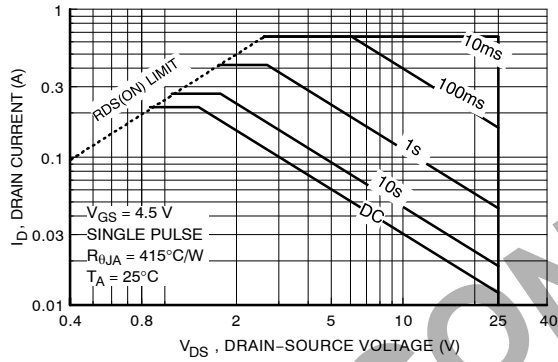


Figure 9. Maximum Safe Operating Area

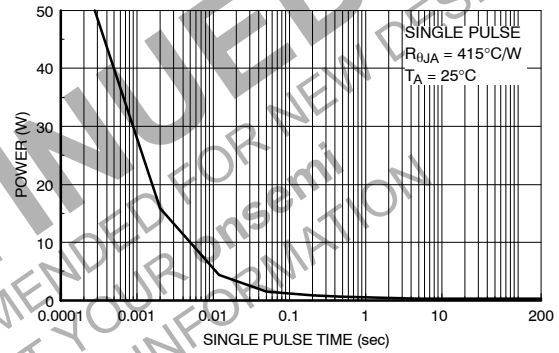


Figure 10. Single Pulse Maximum Power Dissipation

TYPICAL PERFORMANCE CHARACTERISTICS: P-CHANNEL

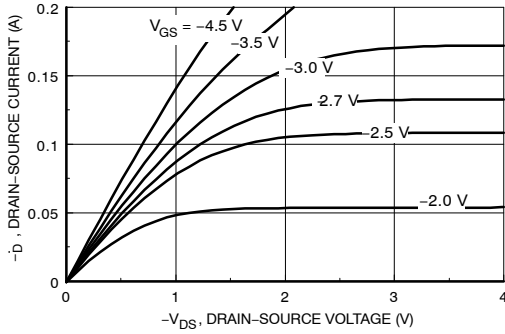


Figure 11. On-Region Characteristics

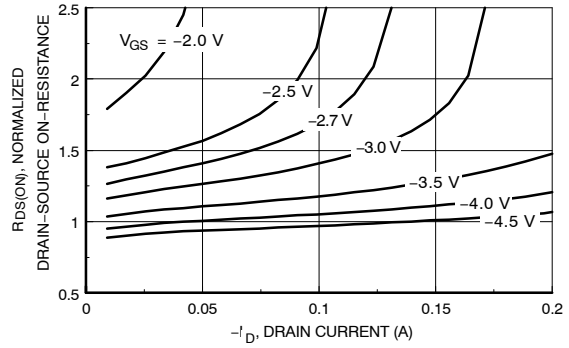


Figure 12. On-Resistance Variation with Drain Current and Gate Voltage

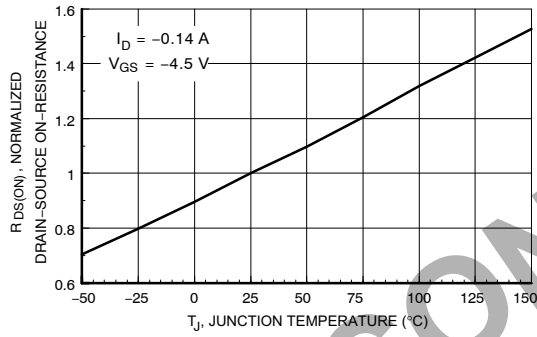


Figure 13. On-Resistance Variation with Temperature

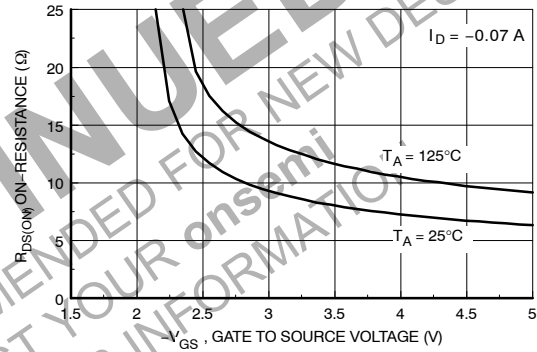


Figure 14. On-Resistance Variation with Gate-to-Source Voltage

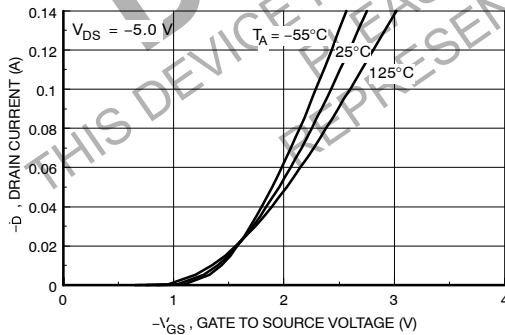


Figure 15. Transfer Characteristics

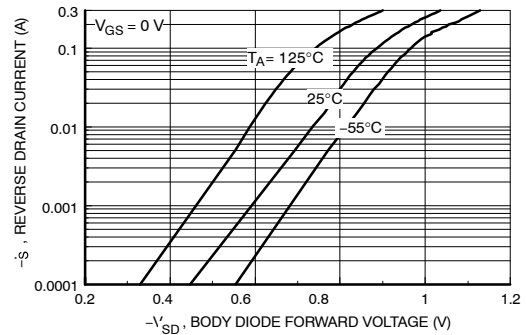


Figure 16. Body Diode Forward Voltage Variation with Source Current and Temperature

TYPICAL PERFORMANCE CHARACTERISTICS: P-CHANNEL (continued)

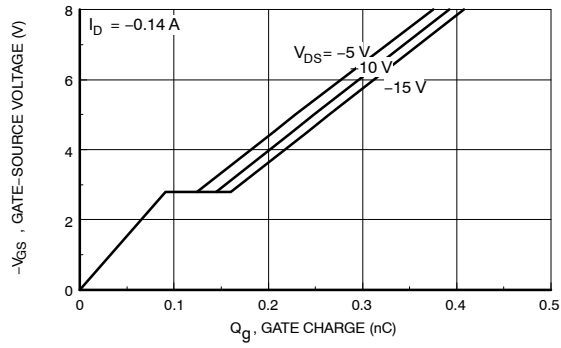


Figure 17. Gate Charge Characteristics

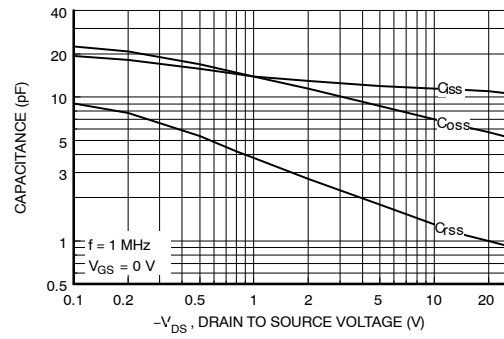


Figure 18. Capacitance Characteristics

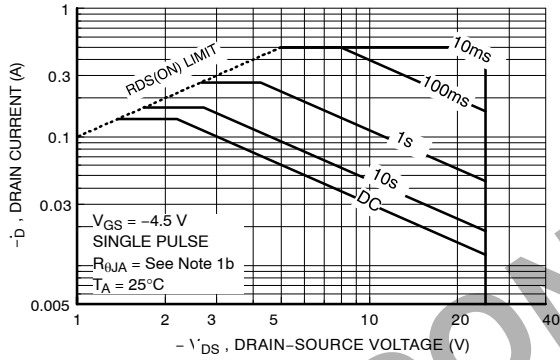


Figure 19. Maximum Safe Operating Area

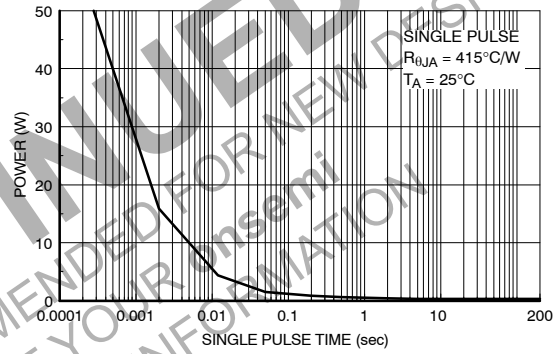
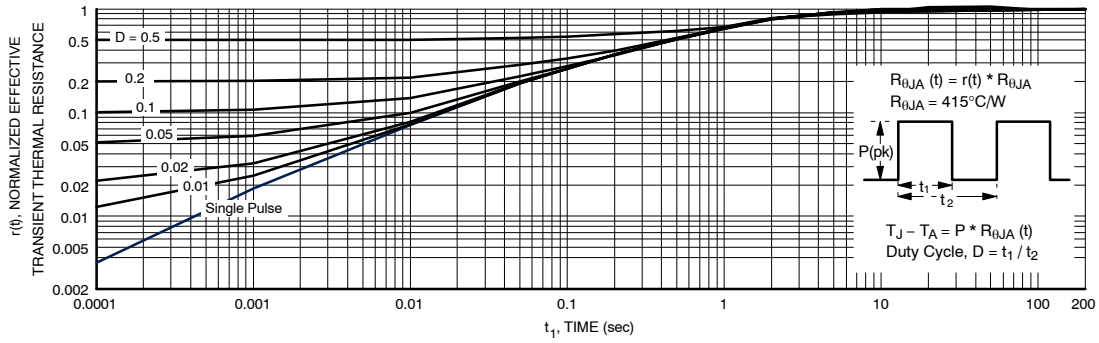


Figure 20. Single Pulse Maximum Power Dissipation

TYPICAL PERFORMANCE CHARACTERISTICS: N & P-CHANNEL



Thermal characterization performed using the conditions described in Note 1.
 Transient thermal response will change depending on the circuit board design.

Figure 21. Transient Thermal Response Curve

ORDERING INFORMATION

Device Order Number	Device Marking	Package Type	Shipping†
FDG6320C	20	SC-88/SC70-6/SOT-363 (Pb-Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

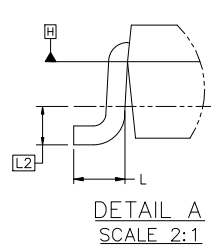
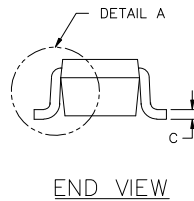
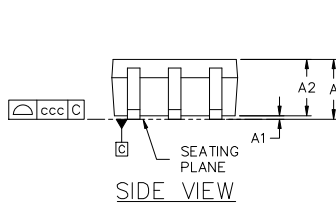
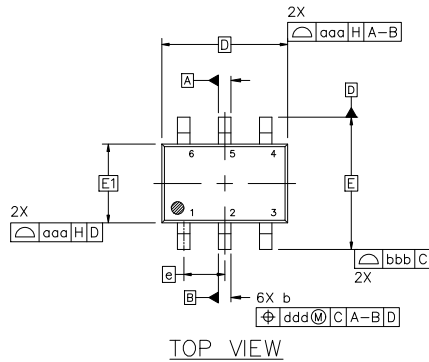


SC-88 2.00x1.25x0.90, 0.65P
CASE 419B-02
ISSUE Z

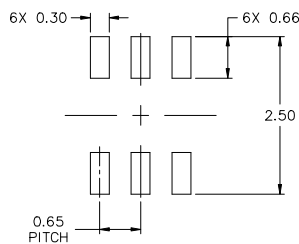
DATE 18 APR 2024

NOTES:

1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5-2018.
2. ALL DIMENSION ARE IN MILLIMETERS.
3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.20 PER END.
4. DIMENSIONS D AND E1 AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY AND DATUM H.
5. DATUMS A AND B ARE DETERMINED AT DATUM H.
6. DIMENSIONS b AND c APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.08 AND 0.15 FROM THE TIP.
7. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 TOTAL IN EXCESS OF DIMENSION b AT MAXIMUM MATERIAL CONDITION. THE DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT.



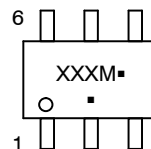
DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	---	---	1.10
A1	0.00	---	0.10
A2	0.70	0.90	1.00
b	0.15	0.20	0.25
c	0.08	0.15	0.22
D	2.00 BSC		
E	2.10 BSC		
E1	1.25 BSC		
e	0.65 BSC		
L	0.26	0.36	0.46
L2	0.15 BSC		
aaa	0.15		
bbb	0.30		
ccc	0.10		
ddd	0.10		



RECOMMENDED MOUNTING FOOTPRINT*

* FOR ADDITIONAL INFORMATION ON OUR Pb-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ONSEMI SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

GENERIC
MARKING DIAGRAM*



XXX = Specific Device Code
M = Date Code*
▪ = Pb-Free Package

(Note: Microdot may be in either location)

*Date Code orientation and/or position may vary depending upon manufacturing location.

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

DOCUMENT NUMBER:	98ASB42985B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	SC-88 2.00x1.25x0.90, 0.65P	PAGE 1 OF 2

onsemi and onsemi are trademarks of Semiconductor Components Industries, LLC dba onsemi or its subsidiaries in the United States and/or other countries. onsemi reserves the right to make changes without further notice to any products herein. onsemi makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. onsemi does not convey any license under its patent rights nor the rights of others.

SC-88 2.00x1.25x0.90, 0.65P
CASE 419B-02
ISSUE Z

DATE 18 APR 2024

STYLE 1: PIN 1. EMITTER 2 2. BASE 2 3. COLLECTOR 1 4. EMITTER 1 5. BASE 1 6. COLLECTOR 2	STYLE 2: CANCELLED	STYLE 3: CANCELLED	STYLE 4: PIN 1. CATHODE 2. CATHODE 3. COLLECTOR 4. EMITTER 5. BASE 6. ANODE	STYLE 5: PIN 1. ANODE 2. ANODE 3. COLLECTOR 4. EMITTER 5. BASE 6. CATHODE	STYLE 6: PIN 1. ANODE 2 2. N/C 3. CATHODE 1 4. ANODE 1 5. N/C 6. CATHODE 2
STYLE 7: PIN 1. SOURCE 2 2. DRAIN 2 3. GATE 1 4. SOURCE 1 5. DRAIN 1 6. GATE 2	STYLE 8: CANCELLED	STYLE 9: PIN 1. EMITTER 2 2. EMITTER 1 3. COLLECTOR 1 4. BASE 1 5. BASE 2 6. COLLECTOR 2	STYLE 10: PIN 1. SOURCE 2 2. SOURCE 1 3. GATE 1 4. DRAIN 1 5. DRAIN 2 6. GATE 2	STYLE 11: PIN 1. CATHODE 2 2. CATHODE 2 3. ANODE 1 4. CATHODE 1 5. CATHODE 1 6. ANODE 2	STYLE 12: PIN 1. ANODE 2 2. ANODE 2 3. CATHODE 1 4. ANODE 1 5. ANODE 1 6. CATHODE 2
STYLE 13: PIN 1. ANODE 2. N/C 3. COLLECTOR 4. EMITTER 5. BASE 6. CATHODE	STYLE 14: PIN 1. VREF 2. GND 3. GND 4. IOUT 5. VEN 6. VCC	STYLE 15: PIN 1. ANODE 1 2. ANODE 2 3. ANODE 3 4. CATHODE 3 5. CATHODE 2 6. CATHODE 1	STYLE 16: PIN 1. BASE 1 2. EMITTER 2 3. COLLECTOR 2 4. BASE 2 5. EMITTER 1 6. COLLECTOR 1	STYLE 17: PIN 1. BASE 1 2. EMITTER 1 3. COLLECTOR 2 4. BASE 2 5. EMITTER 2 6. COLLECTOR 1	STYLE 18: PIN 1. VIN1 2. VCC 3. VOUT2 4. VIN2 5. GND 6. VOUT1
STYLE 19: PIN 1. I OUT 2. GND 3. GND 4. V CC 5. V EN 6. V REF	STYLE 20: PIN 1. COLLECTOR 2. COLLECTOR 3. BASE 4. EMITTER 5. COLLECTOR 6. COLLECTOR	STYLE 21: PIN 1. ANODE 1 2. N/C 3. ANODE 2 4. CATHODE 2 5. N/C 6. CATHODE 1	STYLE 22: PIN 1. D1 (i) 2. GND 3. D2 (i) 4. D2 (c) 5. VBUS 6. D1 (c)	STYLE 23: PIN 1. Vn 2. CH1 3. Vp 4. N/C 5. CH2 6. N/C	STYLE 24: PIN 1. CATHODE 2. ANODE 3. CATHODE 4. CATHODE 5. CATHODE 6. CATHODE
STYLE 25: PIN 1. BASE 1 2. CATHODE 3. COLLECTOR 2 4. BASE 2 5. EMITTER 6. COLLECTOR 1	STYLE 26: PIN 1. SOURCE 1 2. GATE 1 3. DRAIN 2 4. SOURCE 2 5. GATE 2 6. DRAIN 1	STYLE 27: PIN 1. BASE 2 2. BASE 1 3. COLLECTOR 1 4. EMITTER 1 5. EMITTER 2 6. COLLECTOR 2	STYLE 28: PIN 1. DRAIN 2. DRAIN 3. GATE 4. SOURCE 5. DRAIN 6. DRAIN	STYLE 29: PIN 1. ANODE 2. ANODE 3. COLLECTOR 4. EMITTER 5. BASE/ANODE 6. CATHODE	STYLE 30: PIN 1. SOURCE 1 2. DRAIN 2 3. DRAIN 2 4. SOURCE 2 5. GATE 1 6. DRAIN 1

Note: Please refer to datasheet for style callout. If style type is not called out in the datasheet refer to the device datasheet pinout or pin assignment.

DOCUMENT NUMBER:	98ASB42985B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	SC-88 2.00x1.25x0.90, 0.65P	PAGE 2 OF 2

onsemi and onsemi are trademarks of Semiconductor Components Industries, LLC dba onsemi or its subsidiaries in the United States and/or other countries. onsemi reserves the right to make changes without further notice to any products herein. onsemi makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. onsemi does not convey any license under its patent rights nor the rights of others.

onsemi, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:

Technical Library: www.onsemi.com/design/resources/technical-documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support

For additional information, please contact your local Sales Representative at
www.onsemi.com/support/sales