

# MOSFET – Dual, N-Channel, Common Drain, POWERTRENCH®

20 V, 9.7 A, 16.5 mΩ

## FDMB2307NZ

### General Description

This device is designed specifically as a single package solution for Li-Ion battery pack protection circuit and other ultra-portable applications. It features two common drain N-channel MOSFETs, which enables bidirectional current flow, on onsemi's advanced POWERTRENCH process with state of the art MicroFET™ Leadframe, the FDMB2307NZ minimizes both PCB space and  $r_{S1S2(on)}$ .

### Features

- Max  $r_{S1S2(on)}$  = 16.5 mΩ at  $V_{GS} = 4.5$  V,  $I_D = 8$  A
- Max  $r_{S1S2(on)}$  = 18 mΩ at  $V_{GS} = 4.2$  V,  $I_D = 7.4$  A
- Max  $r_{S1S2(on)}$  = 21 mΩ at  $V_{GS} = 3.1$  V,  $I_D = 7$  A
- Max  $r_{S1S2(on)}$  = 24 mΩ at  $V_{GS} = 2.5$  V,  $I_D = 6.7$  A
- Low Profile – 0.8 mm Maximum – in the New Package MicroFET 2x3 mm
- HBM ESD Protection Level > 2 kV (Note 3)
- This Device is Pb-Free, Halide Free and is RoHS Compliant

### Applications

- Li-Ion Battery Pack

### MOSFET MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$ , unless otherwise noted)

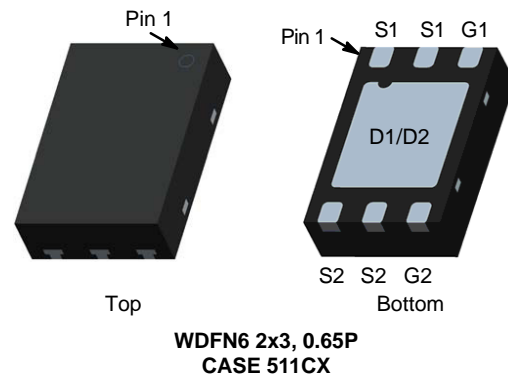
Symbol	Parameter	Ratings	Unit
$V_{S1S2}$	Source1 to Source2 Voltage	20	V
$V_{GS}$	Gate to Source Voltage (Note 4)	±12	V
$I_{S1S2}$	Source1 to Source2 Current –Continuous $T_A = 25^\circ\text{C}$ (Note 1a) –Pulsed	9.7 40	A
$P_D$	Power Dissipation $T_A = 25^\circ\text{C}$ (Note 1a) $T_A = 25^\circ\text{C}$ (Note 1b)	2.2 0.8	W
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	–55 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

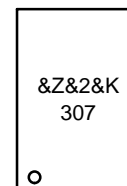
### THERMAL CHARACTERISTICS ( $T_A = 25^\circ\text{C}$ , unless otherwise noted)

Symbol	Parameter	Ratings	Unit
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	57	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1b)	161	

$V_{S1S2}$	$r_{S1S2(on)}$ MAX	$I_{S1S2}$ MAX
20 V	16.5 mΩ @ 4.5 V	9.7 A
	18 mΩ @ 4.2 V	
	21 mΩ @ 3.1 V	
	24 mΩ @ 2.5 V	

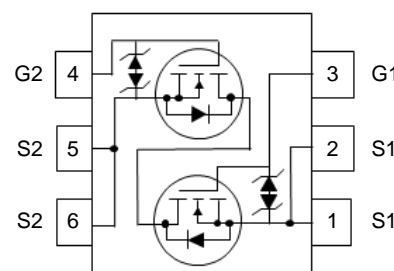


### MARKING DIAGRAM



&Z = Assembly Plant Code  
&2 = 2-Digit Date Code  
&K = 2-Digits Lot Run Traceability Code  
307 = Specific Device Code

### PIN ASSIGNMENT



### ORDERING INFORMATION

See detailed ordering and shipping information on page 5 of this data sheet.

# FDMB2307NZ

## ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = 25°C unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
--------	-----------	----------------	-----	-----	-----	------

### OFF CHARACTERISTICS

I <sub>S1S2</sub>	Zero Gate Voltage Source1 to Source2 Current	V <sub>S1S2</sub> = 16 V, V <sub>GS</sub> = 0 V	–	–	1	μA
I <sub>GSS</sub>	Gate to Source Leakage Current	V <sub>GS</sub> = 12 V, V <sub>S1S2</sub> = 0 V	–	–	10	μA

### ON CHARACTERISTICS

V <sub>GS(th)</sub>	Gate to Source Threshold Voltage	V <sub>GS</sub> = V <sub>S1S2</sub> , I <sub>S1S2</sub> = 250 μA	0.6	1	1.5	V
r <sub>S1S2(on)</sub>	Static Source1 to Source2 On Resistance	V <sub>GS</sub> = 4.5 V, I <sub>S1S2</sub> = 8 A	10.5	13.5	16.5	mΩ
		V <sub>GS</sub> = 4.2 V, I <sub>S1S2</sub> = 7.4 A	11	14	18	
		V <sub>GS</sub> = 3.1 V, I <sub>S1S2</sub> = 7 A	11.5	16	21	
		V <sub>GS</sub> = 2.5 V, I <sub>S1S2</sub> = 6.7 A	12	18	24	
		V <sub>GS</sub> = 4.5 V, I <sub>S1S2</sub> = 8 A, T <sub>J</sub> = 125°C	11	20	29	
g <sub>FS</sub>	Forward Transconductance	V <sub>S1S2</sub> = 5 V, I <sub>S1S2</sub> = 8 A	–	41	–	S

### DYNAMIC CHARACTERISTICS

C <sub>iss</sub>	Input Capacitance	V <sub>S1S2</sub> = 10 V, V <sub>GS</sub> = 0 V, f = 1 MHz	–	1760	2640	pF
C <sub>oss</sub>	Output Capacitance		–	229	345	pF
C <sub>rss</sub>	Reverse Transfer Capacitance		–	211	320	pF
R <sub>g</sub>	Gate Resistance (Note 5)		0.1	2.6	8	Ω

### SWITCHING CHARACTERISTICS

t <sub>d(on)</sub>	Turn-On Delay Time	V <sub>S1S2</sub> = 10 V, I <sub>S1S2</sub> = 8 A, V <sub>GS</sub> = 4.5 V, R <sub>GEN</sub> = 6 Ω	–	12	22	ns
t <sub>r</sub>	Rise Time		–	19	34	ns
t <sub>d(off)</sub>	Turn-Off Delay Time		–	32	51	ns
t <sub>f</sub>	Fall Time		–	9.5	17	ns
Q <sub>g</sub>	Total Gate Charge	V <sub>G1S1</sub> = 0 V to 5 V, V <sub>S1S2</sub> = 10 V, I <sub>S1S2</sub> = 8 A, V <sub>G2S2</sub> = 0 V	–	20	28	nC
Q <sub>g</sub>	Total Gate Charge	V <sub>G1S1</sub> = 0 V to 4.5 V, V <sub>S1S2</sub> = 10 V, I <sub>S1S2</sub> = 8 A, V <sub>G2S2</sub> = 0 V	–	18	25	nC
Q <sub>gs</sub>	Gate1 to Source1 Charge	V <sub>S1S2</sub> = 10 V, I <sub>S1S2</sub> = 8 A, V <sub>G2S2</sub> = 0 V	–	2.8	–	nC
Q <sub>gd</sub>	Gate1 to Source2 “Miller” Charge		–	5.3	–	nC

### DRAIN-SOURCE CHARACTERISTICS

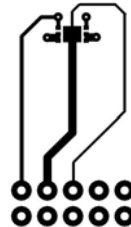
I <sub>fss</sub>	Maximum Continuous Source1–Source2 Diode Forward Current	–	–	8	A	
V <sub>fss</sub>	Source1 to Source2 Diode Forward Voltage	V <sub>G1S1</sub> = 0 V, V <sub>G2S2</sub> = 4.5 V, I <sub>fss</sub> = 8 A (Note 2)	–	0.8	1.2	V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

- R<sub>θJA</sub> is determined with the device mounted on a 1 in<sup>2</sup> pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. R<sub>θJC</sub> is guaranteed by design while R<sub>θCA</sub> is determined by the user's board design.



a. 57°C/W when mounted on a 1 in<sup>2</sup> pad of 2 oz copper



b. 161°C/W when mounted on a minimum pad of 2 oz copper

- Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.
- The diode connected between the gate and source serves only as protection against ESD. No gate overvoltage rating is implied.
- As an N-ch device, the negative V<sub>gs</sub> rating is for low duty cycle pulse occurrence only. No continuous rating is implied.
- R<sub>g</sub> is measured on 100% of the die at wafer level.

TYPICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ , unless otherwise noted)

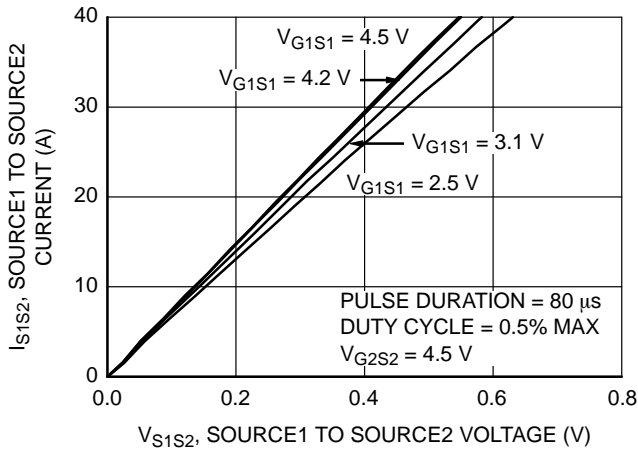


Figure 1. On-Region Characteristics

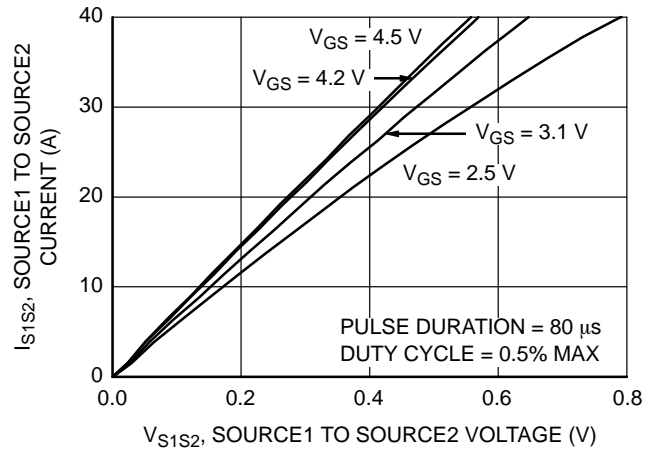


Figure 2. On-Region Characteristics

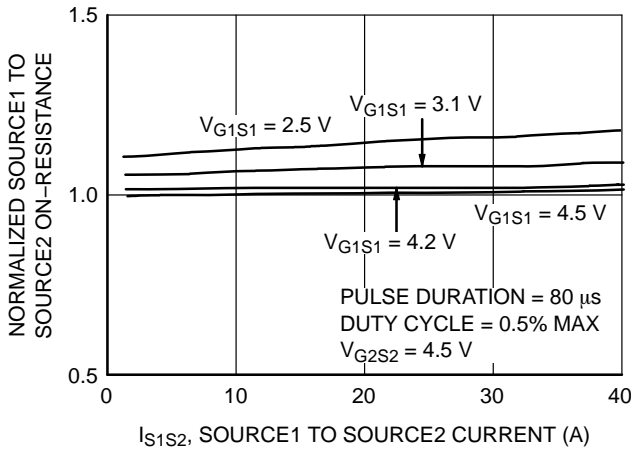


Figure 3. Normalized On-Resistance vs. Source1 to Source2 Current and Gate Voltage

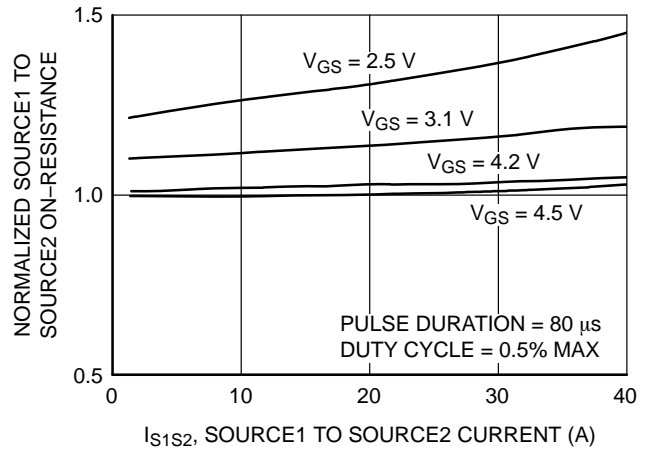


Figure 4. Normalized On-Resistance vs. Source1 to Source2 Current and Gate Voltage

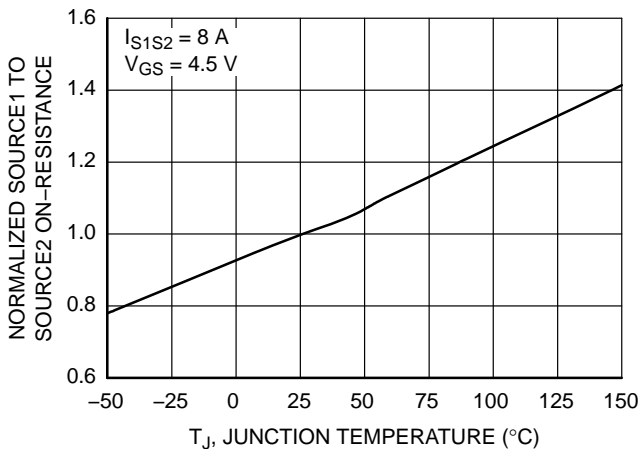


Figure 5. Normalized On Resistance vs. Junction Temperature

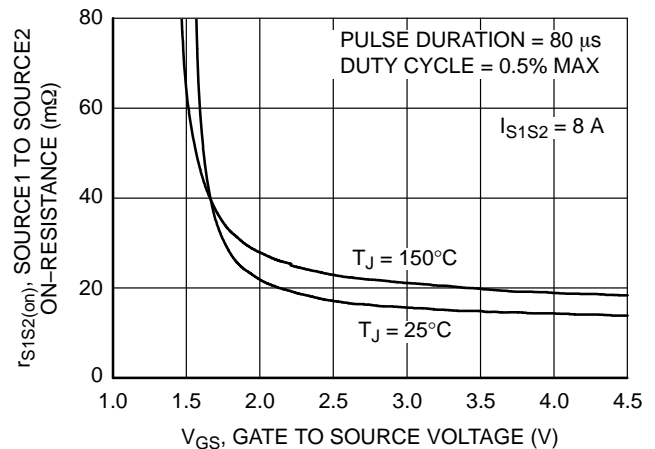


Figure 6. On Resistance vs. Gate to Source Voltage

TYPICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ , unless otherwise noted) (continued)

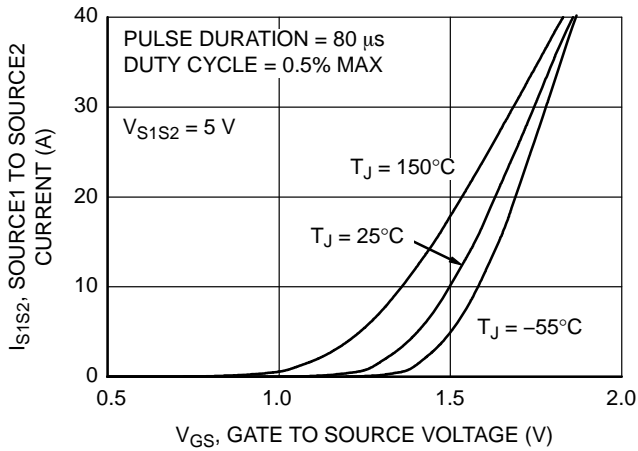


Figure 7. Transfer Characteristics

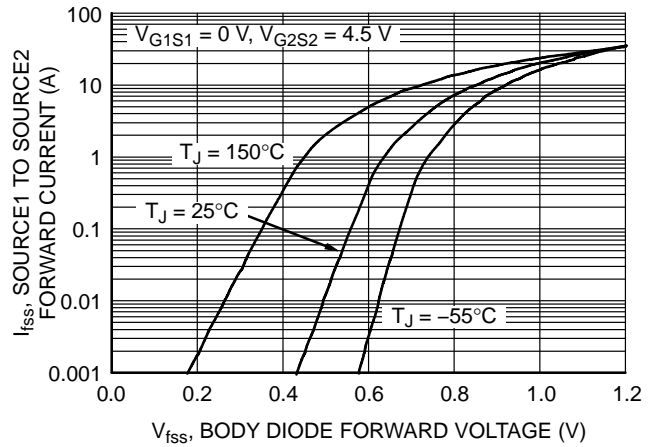


Figure 8. Source1 to Source2 Diode Forward Voltage vs. Source Current

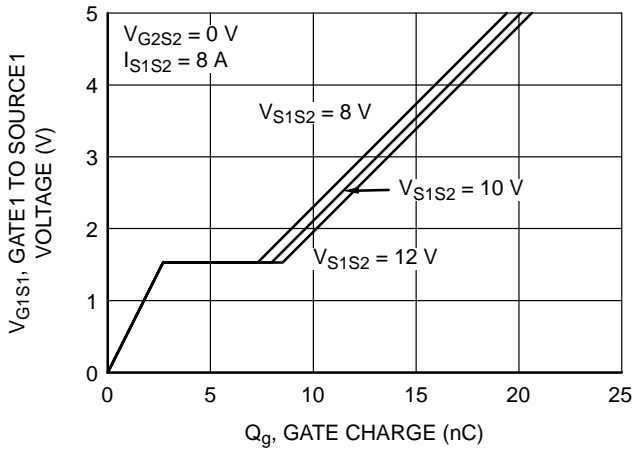


Figure 9. Gate Charge Characteristics

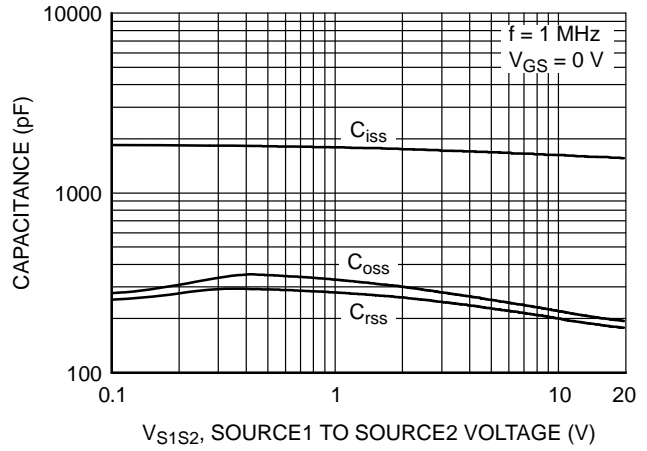


Figure 10. Capacitance vs. Source1 to Source2 Voltage

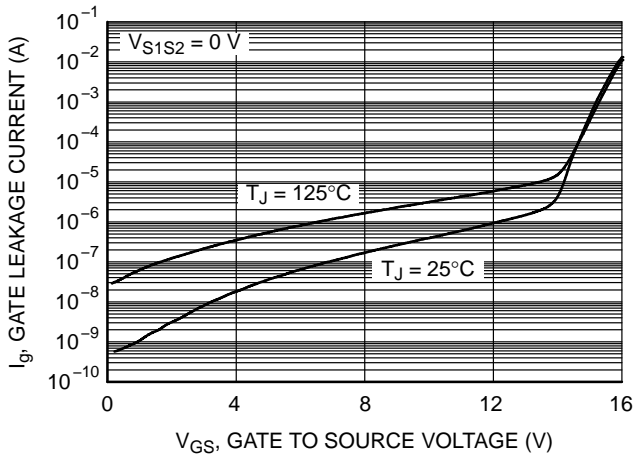


Figure 11. Gate Leakage Current vs. Gate to Source Voltage

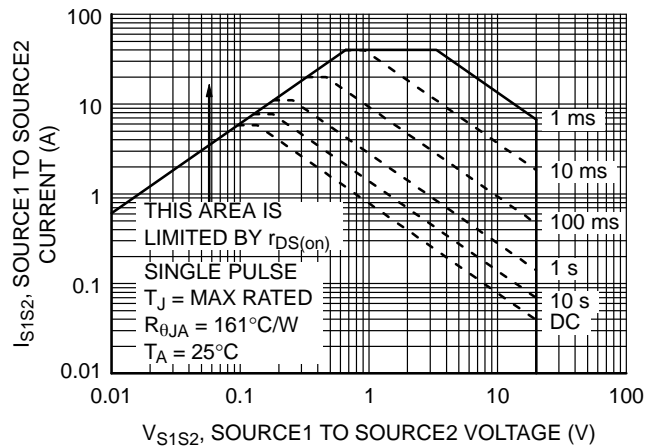


Figure 12. Forward Bias Safe Operating Area

# FDMB2307NZ

## TYPICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ , unless otherwise noted) (continued)

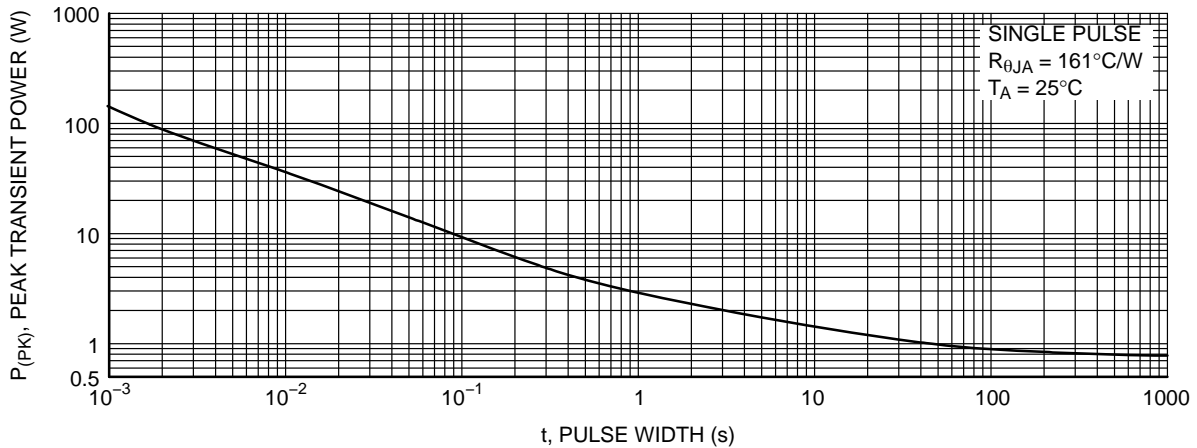


Figure 13. Single Pulse Maximum Power Dissipation

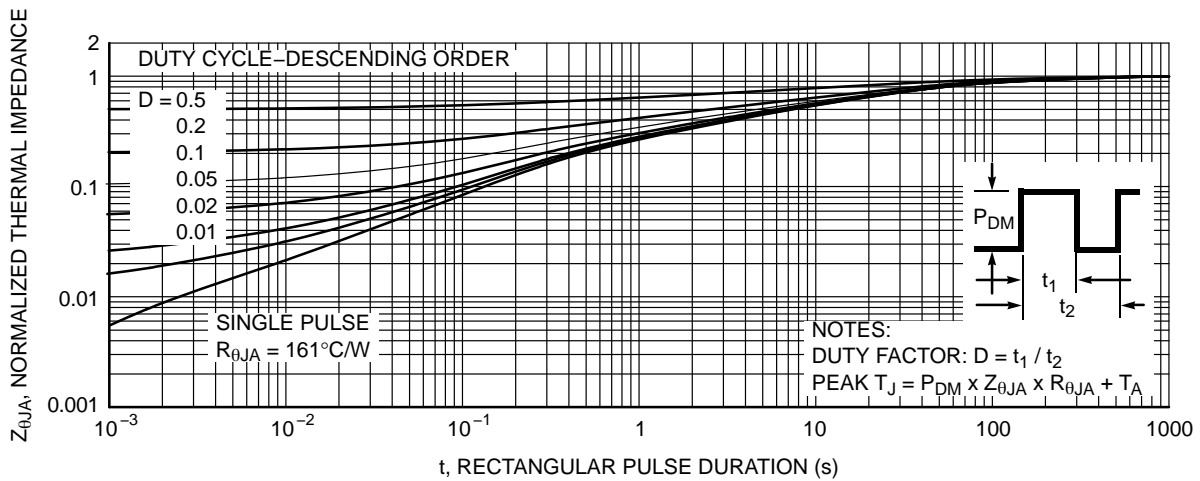


Figure 14. Junction-to-Ambient Transient Thermal Response Curve

### PACKAGE MARKING AND ORDERING INFORMATION

Device	Device Marking	Package	Reel Size	Tape Width	Shipping†
FDMB2307NZ	307	WDFN6 2x3, 0.65P (Pb-Free, Halide Free)	7"	8 mm	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

POWERTRENCH is registered trademark of Semiconductor Components Industries, LLC dba "onsemi" or its affiliates and/or subsidiaries in the United States and/or other countries.

MicroFET is trademark of Semiconductor Components Industries, LLC dba "onsemi" or its affiliates and/or subsidiaries in the United States and/or other countries.

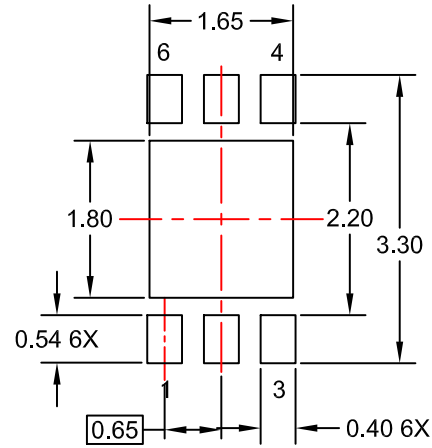
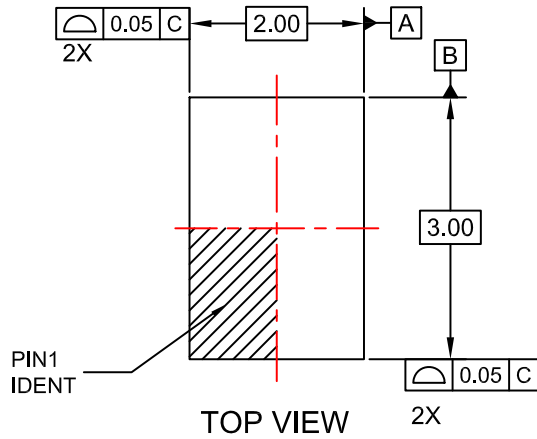
**MECHANICAL CASE OUTLINE**  
**PACKAGE DIMENSIONS**

ON Semiconductor®

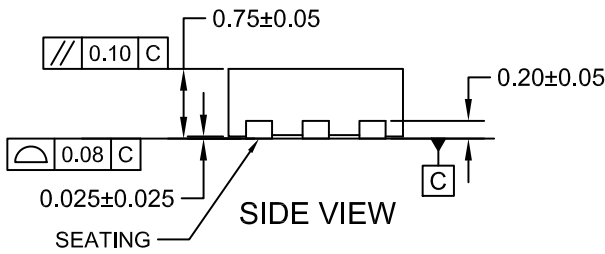


**WDFN6 2x3, 0.65P**  
CASE 511CX  
ISSUE O

DATE 31 JUL 2016

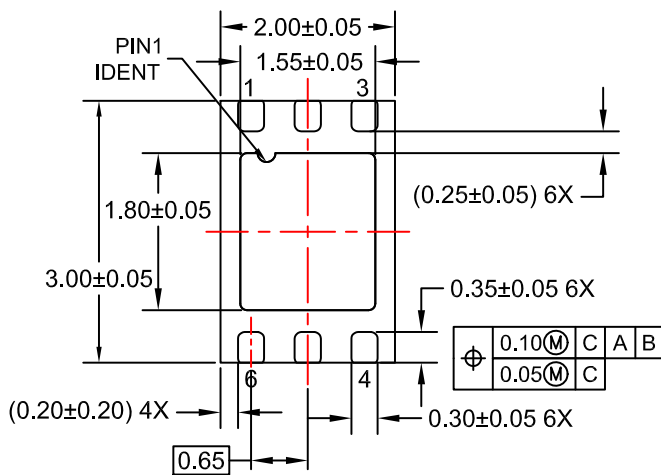


**RECOMMENDED LAND PATTERN**



**NOTES:**

- A. PACKAGE CONFORMS TO JEDEC MO-229 EXCEPT WHERE NOTED.
- B. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.
- C. LAND PATTERN RECOMMENDATION IS EXISTING INDUSTRY LAND PATTERN.
- D. DIMENSIONS ARE IN MILLIMETERS.
- E. REFERENCE DIMENSIONS ARE UNCONTROLLED



**BOTTOM VIEW**

<b>DOCUMENT NUMBER:</b>	<b>98AON13612G</b>	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
<b>DESCRIPTION:</b>	<b>WDFN6 2X3, 0.65P</b>	<b>PAGE 1 OF 1</b>

ON Semiconductor and are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. ON Semiconductor does not convey any license under its patent rights nor the rights of others.

**onsemi**, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at [www.onsemi.com/site/pdf/Patent-Marking.pdf](http://www.onsemi.com/site/pdf/Patent-Marking.pdf). **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

---

## ADDITIONAL INFORMATION

### TECHNICAL PUBLICATIONS:

Technical Library: [www.onsemi.com/design/resources/technical-documentation](http://www.onsemi.com/design/resources/technical-documentation)  
onsemi Website: [www.onsemi.com](http://www.onsemi.com)

### ONLINE SUPPORT: [www.onsemi.com/support](http://www.onsemi.com/support)

For additional information, please contact your local Sales Representative at [www.onsemi.com/support/sales](http://www.onsemi.com/support/sales)