

# MOSFET – N-Channel, POWERTRENCH®

40 V, 49 A, 2.5 mΩ

## FDMC8321L

### General Description

This N-Channel MOSFET has been designed specifically to improve the overall efficiency and to minimize switch mode ringing of DC/DC converters using either synchronous or conventional switching PWM controllers. It has been optimized for low gate charge, low  $R_{DS(on)}$ , fast switching speed body diode reverse recovery performance.

### Features

- Max  $R_{DS(on)}$  = 2.5 mΩ at  $V_{GS} = 10\text{ V}$ ,  $I_D = 22\text{ A}$   
Max  $R_{DS(on)}$  = 4.1 mΩ at  $V_{GS} = 4.5\text{ V}$ ,  $I_D = 18\text{ A}$
- Advanced Package and Silicon Combination for Low  $R_{DS(on)}$  and High Efficiency
- Next Generation Enhanced Body Diode Technology, Engineered for Soft Recovery
- 100% UIL Tested
- Pb-Free, Halide Free and RoHS Compliant

### Applications

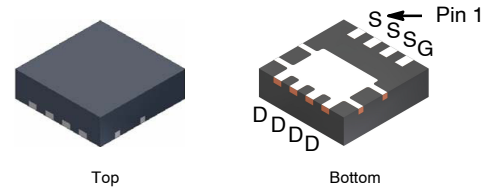
- Synchronous Rectifier
- Load Switch/Orring
- Motor Switch

### MOSFET MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter		Rating	Unit
$V_{DS}$	Drain to Source Voltage		40	V
$V_{GS}$	Gate to Source Voltage		$\pm 20$	V
$I_D$	Drain Current	Continuous $T_C = 25^\circ\text{C}$	49	A
		Continuous (Note 1a) $T_A = 25^\circ\text{C}$	22	
		Pulsed	100	
$E_{AS}$	Single Pulse Avalanche Energy (Note 3)		86	mJ
$P_D$	Power Dissipation	$T_C = 25^\circ\text{C}$	40	W
	Power Dissipation (Note 1a)	$T_A = 25^\circ\text{C}$	2.3	
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range		-55 to +150	$^\circ\text{C}$

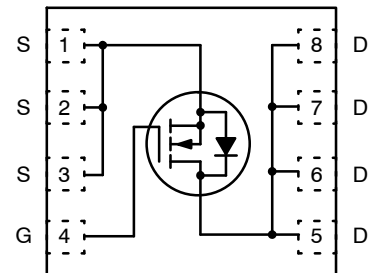
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

$V_{DS}$	$R_{DS(on)}$ MAX	$I_D$ MAX
40 V	2.5 mΩ @ 10 V	49 A
	4.1 mΩ @ 4.5 V	



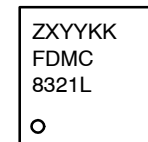
PQFN8 3.3 × 3.3, 0.65P  
(Power 33)  
CASE 483AK

### ELECTRICAL CONNECTION



N-Channel MOSFET

### MARKING DIAGRAM



- Z = Assembly Plant Code
- XYX = 3-Digit Date Code (Year and Week)
- KK = 2-Digits Lot Run Traceability Code
- FDMC8321L = Specific Device Code

### ORDERING INFORMATION

See detailed ordering and shipping information on page 6 of this data sheet.

# FDMC8321L

## THERMAL CHARACTERISTICS (T<sub>A</sub> = 25°C unless otherwise noted)

Symbol	Parameter	Value	Unit
R <sub>θJC</sub>	Thermal Resistance, Junction to Case (Note 1)	3.1	°C/W
R <sub>θJA</sub>	Thermal Resistance, Junction to Ambient (Note 1a)	53	°C/W

## ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

BV <sub>DSS</sub>	Drain to Source Breakdown Voltage	I <sub>D</sub> = 250 μA, V <sub>GS</sub> = 0 V	40	-	-	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I <sub>D</sub> = 250 μA, Referenced to 25°C	-	22	-	mV/°C
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 32 V, V <sub>GS</sub> = 0 V	-	-	1	μA
I <sub>GSS</sub>	Gate to Source Leakage Current	V <sub>GS</sub> = ±20 V, V <sub>DS</sub> = 0 V	-	-	±100	nA

### ON CHARACTERISTICS

V <sub>GS(th)</sub>	Gate to Source Threshold Voltage	V <sub>GS</sub> = V <sub>DS</sub> , I <sub>D</sub> = 250 μA	1.0	1.7	3.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I <sub>D</sub> = 250 μA, Referenced to 25°C	-	-5	-	mV/°C
R <sub>DS(on)</sub>	Static Drain to Source On-Resistance	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 22 A V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 18 A V <sub>GS</sub> = 10 V, I <sub>D</sub> = 22 A, T <sub>J</sub> = 125°C	-	1.9 2.7 2.8	2.5 4.1 3.7	mΩ
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> = 5 V, I <sub>D</sub> = 22 A	-	114	-	S

### DYNAMIC CHARACTERISTICS

C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> = 20 V, V <sub>GS</sub> = 0 V, f = 1 MHz	-	2930	3900	pF
C <sub>oss</sub>	Output Capacitance		-	1000	1330	pF
C <sub>rss</sub>	Reverse Transfer Capacitance		-	60	90	pF
R <sub>g</sub>	Gate Resistance		0.1	0.7	2.5	Ω

### SWITCHING CHARACTERISTICS

t <sub>d(on)</sub>	Turn-On Delay Time	V <sub>DD</sub> = 20 V, I <sub>D</sub> = 22 A, V <sub>GS</sub> = 10 V, R <sub>GEN</sub> = 6 Ω	-	12	22	ns
t <sub>r</sub>	Rise Time		-	6.1	12	ns
t <sub>d(off)</sub>	Turn-Off Delay Time		-	32	51	ns
t <sub>f</sub>	Fall Time		-	4.9	10	ns
Q <sub>g(TOT)</sub>	Total Gate Charge at 10 V	V <sub>DD</sub> = 20 V, I <sub>D</sub> = 22 A	-	44	61	nC
Q <sub>g(TOT)</sub>	Total Gate Charge at 5 V		-	21	32	nC
Q <sub>gs</sub>	Gate to Source Charge		-	7.7	-	nC
Q <sub>gd</sub>	Gate to Drain "Miller" Charge		-	5.8	-	nC

### DRAIN-SOURCE DIODE CHARACTERISTICS

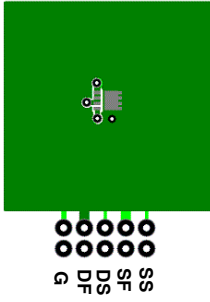
V <sub>SD</sub>	Source to Drain Diode Forward Voltage	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 2 A (Note 2)	-	0.69	1.2	V
		V <sub>GS</sub> = 0 V, I <sub>S</sub> = 22 A (Note 2)	-	0.77	1.3	
t <sub>rr</sub>	Reverse Recovery Time	I <sub>F</sub> = 22 A, di/dt = 100 A/μs	-	41	65	ns
Q <sub>rr</sub>	Reverse Recovery Charge		-	20	33	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

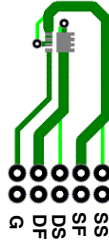
# FDMC8321L

## NOTES:

1.  $R_{\theta JA}$  is determined with the device mounted on a 1 in<sup>2</sup> pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.



a) 53°C/W when mounted on a 1 in<sup>2</sup> pad of 2 oz copper



b) 125°C/W when mounted on a minimum pad of 2 oz copper

2. Pulse Test: Pulse Width < 300  $\mu$ s, Duty Cycle < 2.0%.
3. Starting  $T_J = 25^\circ\text{C}$ ; N-ch:  $L = 0.3$  mH,  $I_{AS} = 24$  A,  $V_{DD} = 36$  V,  $V_{GS} = 10$  V.

TYPICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$  unless otherwise noted)

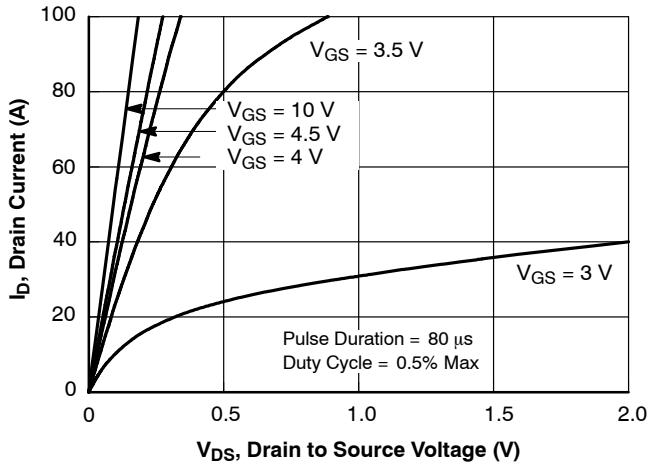


Figure 1. On Region Characteristics

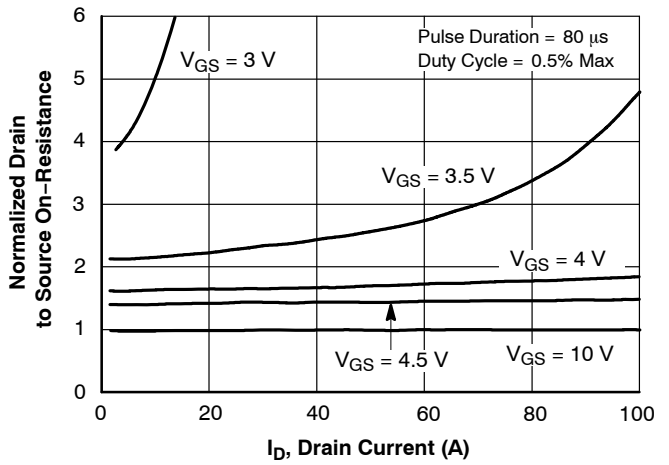


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

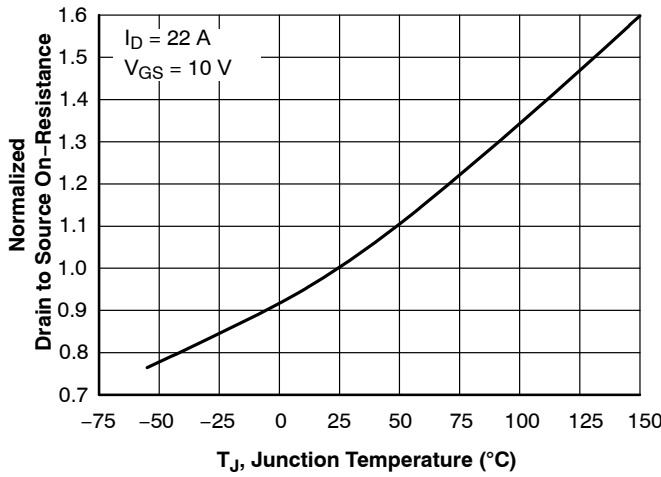


Figure 3. Normalized On Resistance vs. Junction Temperature

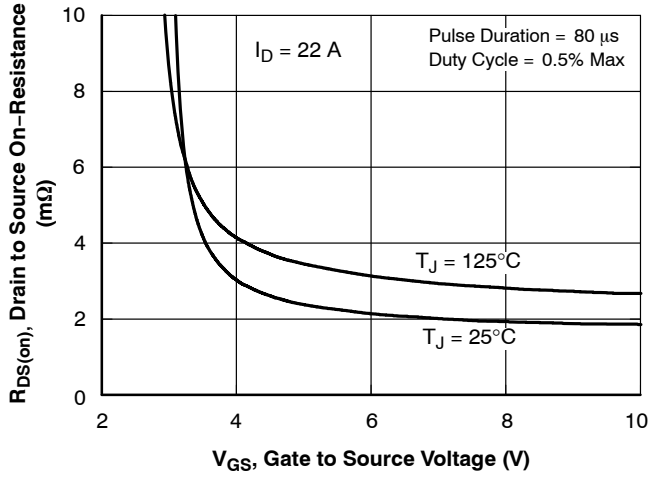


Figure 4. On-Resistance vs. Gate to Source Voltage

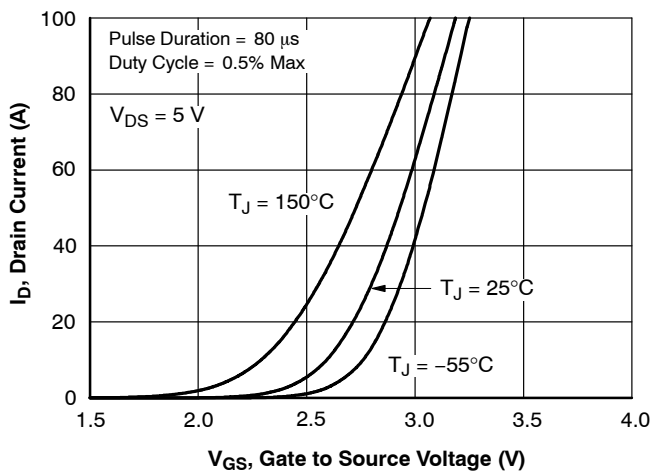


Figure 5. Transfer Characteristics

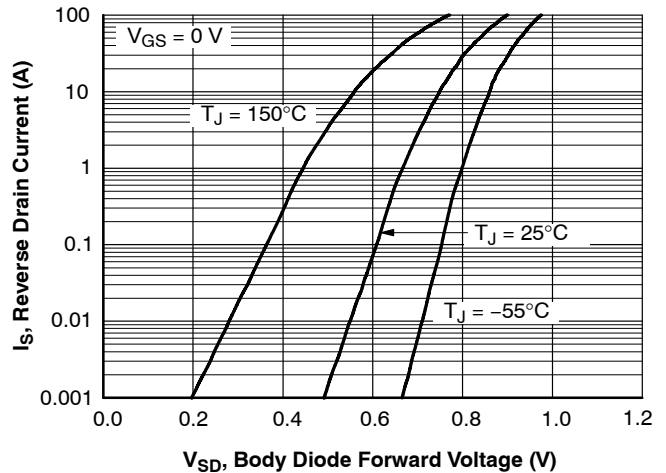


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

TYPICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$  unless otherwise noted) (continued)

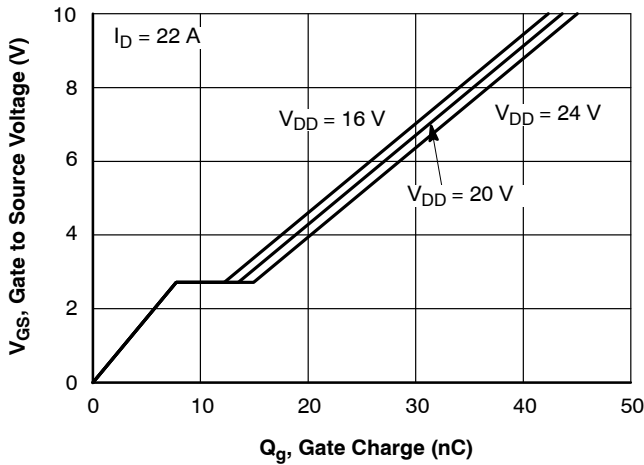


Figure 7. Gate Charge Characteristics

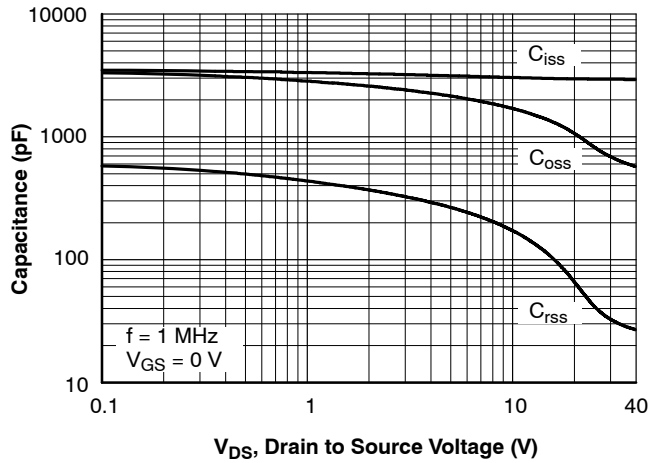


Figure 8. Capacitance vs. Drain to Source Voltage

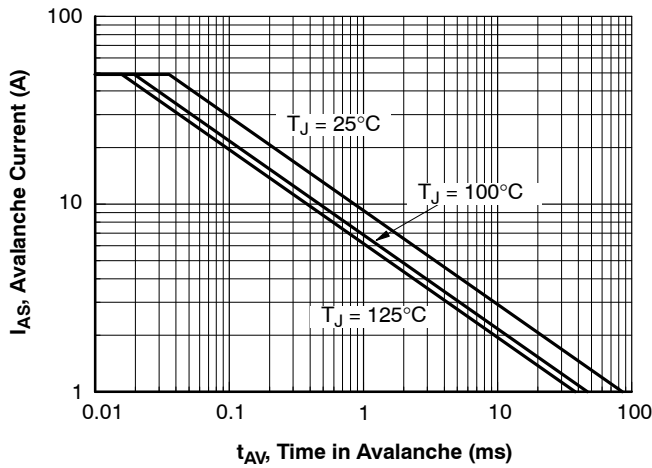


Figure 9. Unclamped Inductive Switching Capability

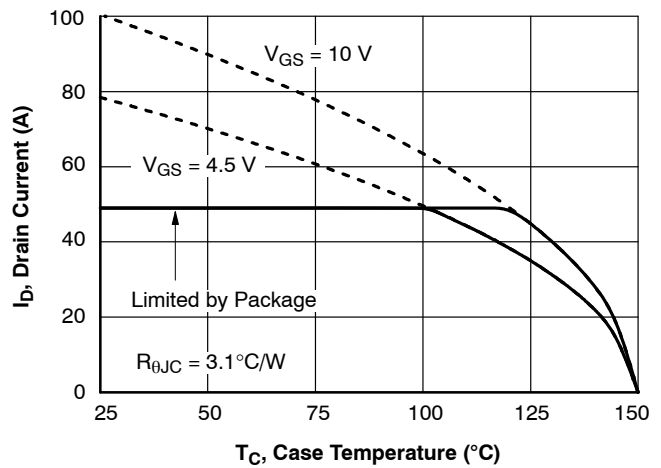


Figure 10. Maximum Continuous Drain Current vs. Case Temperature

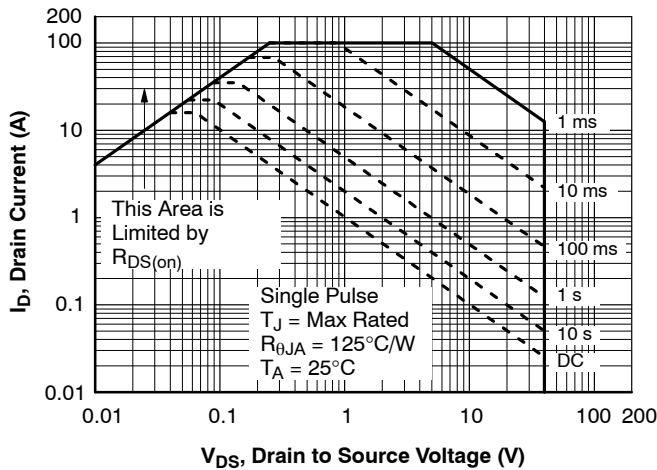


Figure 11. Forward Bias Safe Operating Area

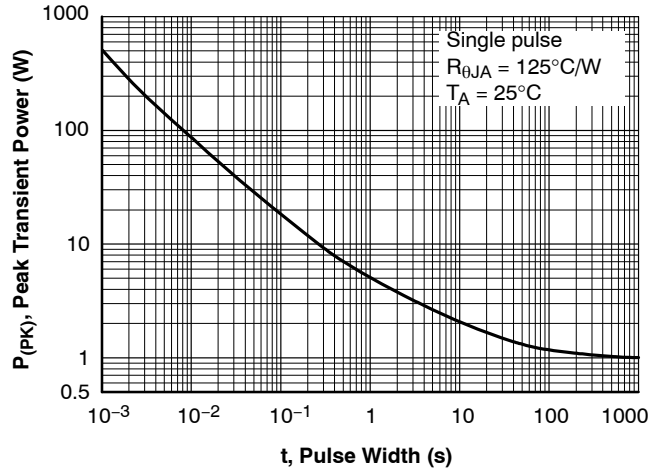


Figure 12. Single Pulse Maximum Power Dissipation

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## TYPICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ unless otherwise noted) (continued)

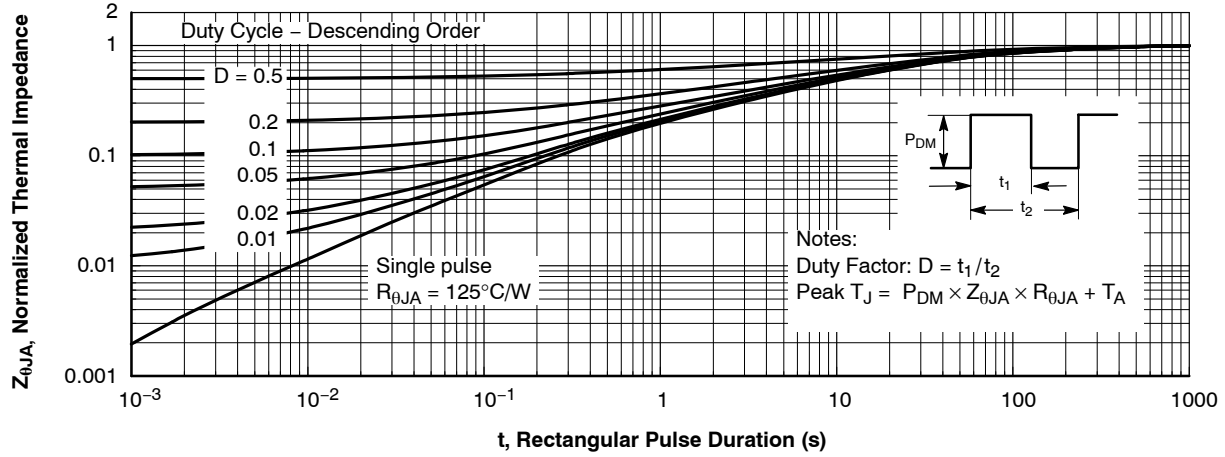


Figure 13. Junction-to-Ambient Transient Thermal Response Curve

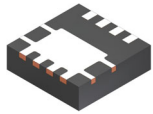
### PACKAGE MARKING AND ORDERING INFORMATION

Device	Device Marking	Package Type	Reel Size	Tape Width	Shipping <sup>†</sup>
FDMC8321L	FDMC8321L	PQFN8 3.3 x 3.3, 0.65P (Power 33) (Pb-Free/Halide Free)	13"	12 mm	3000 / Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

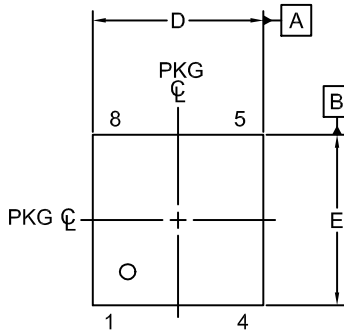
# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

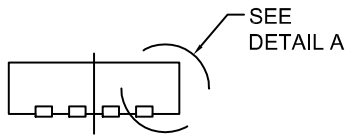


**PQFN8 3.3X3.3, 0.65P**  
**CASE 483AK**  
**ISSUE B**

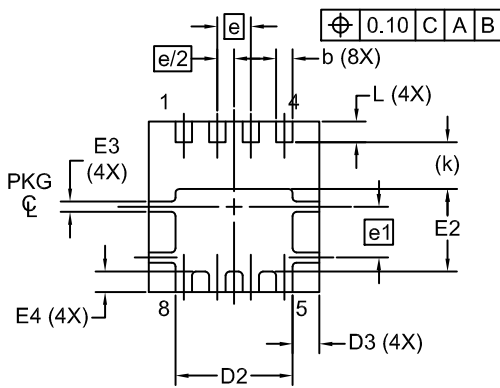
DATE 12 OCT 2021



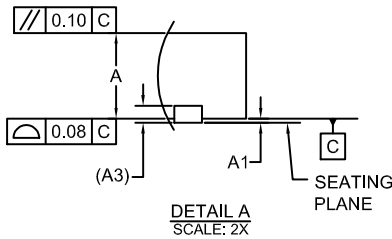
TOP VIEW



FRONT VIEW



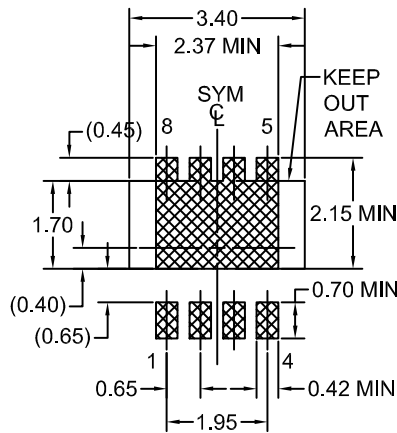
BOTTOM VIEW



DETAIL A  
SCALE: 2X

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.
4. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
5. SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.
6. IT IS RECOMMENDED TO HAVE NO TRACES OR VIAS WITHIN THE KEEP OUT AREA.



LAND PATTERN  
RECOMMENDATION

\*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERM/D.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.90	1.00	1.10
A1	0.00	-	0.05
A3	0.20 REF		
b	0.27	0.32	0.37
D	3.20	3.30	3.40
D2	2.17	2.27	2.37
D3	0.42	0.52	0.62
E	3.20	3.30	3.40
E2	1.50	1.60	1.70
E3	0.10	0.20	0.30
E4	0.29	0.39	0.49
e	0.65 BSC		
e/2	0.325 BSC		
e1	0.98 BSC		
k	0.91 REF		
L	0.30	0.40	0.50

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