

MOSFET – P-Channel, POWER TRENCH®

-150 V, -2 A, 307 mΩ

FDMC86262P

General Description

This P-Channel MOSFET is produced using onsemi's advanced POWER TRENCH technology. This very high density process is especially tailored to minimize on-state resistance and optimized for superior switching performance.

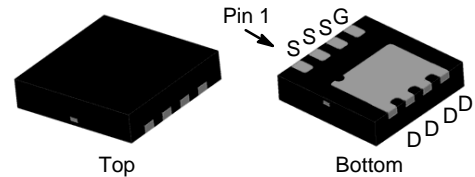
Features

- Max $r_{DS(on)}$ = 307 mΩ at $V_{GS} = -10$ V, $I_D = -2$ A
- Max $r_{DS(on)}$ = 356 mΩ at $V_{GS} = -6$ V, $I_D = -1.8$ A
- Very Low $r_{DS(on)}$ Mid Voltage P-Channel Silicon Technology Optimised for Low Q_g
- Optimised for Fast Switching Applications as Well as Load Switch Applications
- 100% UIL Tested
- This Device is Pb-Free, Halide Free and is ROHS Compliant

Applications

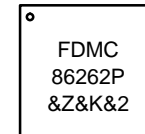
- Active Clamp Switch
- Load Switch

V_{DS}	$r_{DS(on)}$ MAX	I_D MAX
-150 V	307 mΩ @ -10 V	-2 A
	356 mΩ @ -6 V	



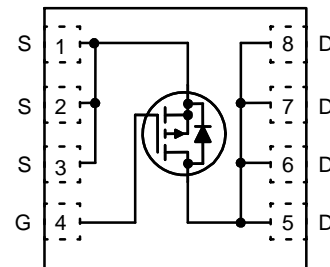
WDFN8 3.3x3.3, 0.65P
(MLP 3.3x3.3)
CASE 511DH

MARKING DIAGRAM



FDMC86262P = Device Code
&Z = Assembly Plant Code
&K = 2-Digits Lot Run Traceability Code
&2 = 2-Digit Date Code Format

PIN ASSIGNMENT



ORDERING INFORMATION

See detailed ordering and shipping information on page 6 of this data sheet.

MOSFET MAXIMUM RATINGS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter			Ratings	Unit
V _{DS}	Drain to Source Voltage			−150	V
V _{GS}	Gate to Source Voltage			±25	V
I _D	Drain Current	Continuous (Note 3)	T _C = 25°C	−8.4	A
		Continuous (Note 3)	T _C = 100°C	−5.3	A
		Continuous (Note 4a)	T _A = 25°C	−2	A
		Pulsed (Note 2)		−35	
E _{AS}	Single Pulse Avalanche Energy (Note 1)			37	mJ
P _D	Power Dissipation		T _C = 25°C	40	W
	Power Dissipation (Note 4a)		T _A = 25°C	2.3	
T _J , T _{STG}	Operating and Storage Junction Temperature Range			−55 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Starting $T_J = 25^\circ\text{C}$, $L = 3\text{ mH}$, $I_{AS} = -5\text{ A}$, $V_{DD} = -150\text{ V}$, $V_{GS} = -10\text{ V}$.

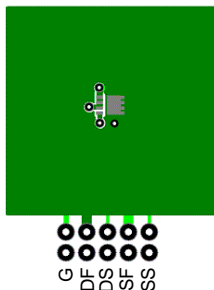
2. Pulsed I_D please refer to Figure 11 SOA graph for more details.

3. Computed continuous current limited to Max Junction Temperature only, actual continuous current will be limited by thermal & electro-mechanical application board design.

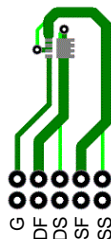
THERMAL CHARACTERISTICS

Symbol	Parameter	Ratings	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	3.1	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 4a)	53	

4. $R_{\theta JA}$ is determined with the device mounted on a 1 in² pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a. 53°C/W when mounted on a 1 in² pad of 2 oz copper



b. 125°C/W when mounted on a minimum pad of 2 oz copper

FDMC86262P

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

BV _{DSS}	Drain to Source Breakdown Voltage	I _D = -250 μA, V _{GS} = 0 V	-150	-	-	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I _D = -250 μA, referenced to 25°C	-	-86	-	mV/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = -120 V, V _{GS} = 0 V	-	-	-1	μA
I _{GSS}	Gate to Source Leakage Current	V _{GS} = ±25 V, V _{DS} = 0 V	-	-	±100	nA

ON CHARACTERISTICS

V _{GS(th)}	Gate to Source Threshold Voltage	V _{GS} = V _{DS} , I _D = 250 μA	-2	-2.9	-4	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I _D = -250 μA, referenced to 25°C	-	5	-	mV/°C
r _{DS(on)}	Static Drain to Source On Resistance	V _{GS} = -10 V, I _D = -2 A	-	241	307	mΩ
		V _{GS} = -6 V, I _D = -1.8 A	-	266	356	
		V _{GS} = -10 V, I _D = -2 A, T _J = 125°C	-	425	541	
g _{FS}	Forward Transconductance	V _{DS} = -10 V, I _D = -2 A	-	5.4	-	S

DYNAMIC CHARACTERISTICS

C _{iss}	Input Capacitance	V _{DS} = -75 V, V _{GS} = 0 V, f = 1 MHz	-	632	885	pF
C _{oss}	Output Capacitance		-	45	65	pF
C _{rss}	Reverse Transfer Capacitance		-	1.3	2.0	pF
R _g	Gate Resistance		0.1	3	6	Ω

SWITCHING CHARACTERISTICS

t _{d(on)}	Turn-On Delay Time	V _{DD} = -75 V, I _D = -2 A, V _{GS} = -10 V, R _{GEN} = 6 Ω	-	8.5	17	ns
t _r	Rise Time		-	2.2	10	ns
t _{d(off)}	Turn-Off Delay Time		-	15	26	ns
t _f	Fall Time		-	5.6	11	ns
Q _g	Total Gate Charge	V _{GS} = 0 V to -10 V, V _{DD} = -75 V, I _D = -2 A	-	9.1	13	nC
Q _g	Total Gate Charge	V _{GS} = 0 V to -6 V, V _{DD} = -75 V, I _D = -2 A	-	5.6	7.9	nC
Q _{gs}	Gate to Source Charge	V _{DD} = -75 V, I _D = -2 A	-	2.5	-	nC
Q _{gd}	Gate to Drain "Miller" Charge		-	1.6	-	nC

DRAIN-SOURCE DIODE CHARACTERISTICS

V _{SD}	Source-Drain Diode Forward Voltage	V _{GS} = 0 V, I _S = -2 A (Note 5)	-	-0.8	-1.3	V
t _{rr}	Reverse Recovery Time	I _F = -2 A, di/dt = 100 A/μs	-	72	116	ns
Q _{rr}	Reverse Recovery Charge		-	166	266	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.

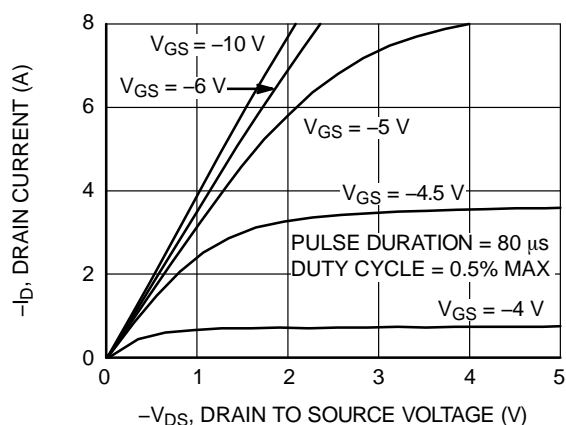
TYPICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)

Figure 1. On Region Characteristics

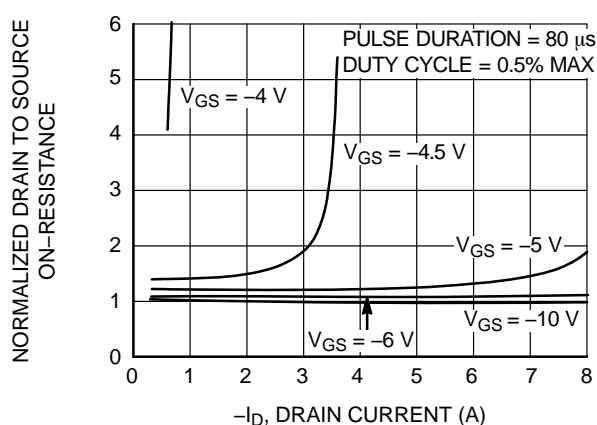


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

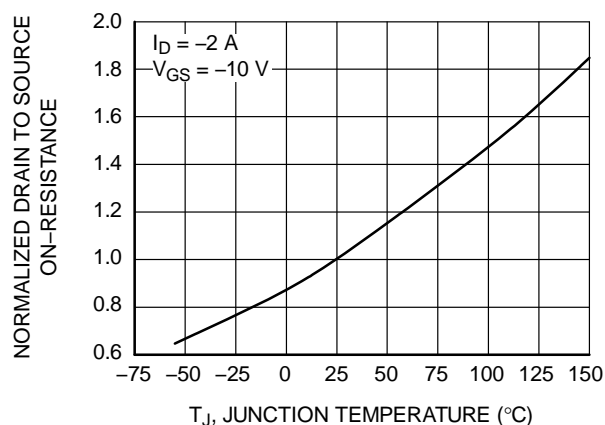


Figure 3. Normalized On-Resistance vs. Junction Temperature

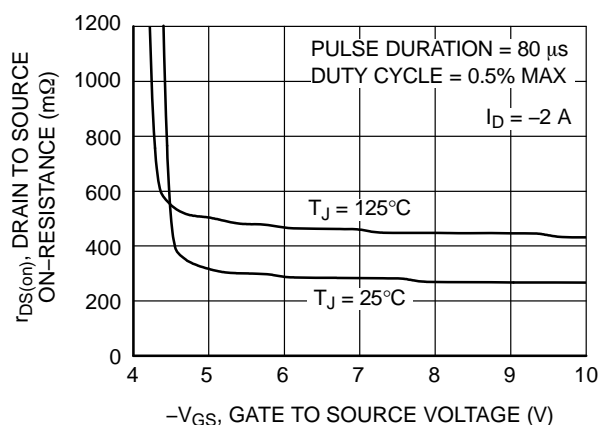


Figure 4. On Resistance vs. Gate to Source Voltage

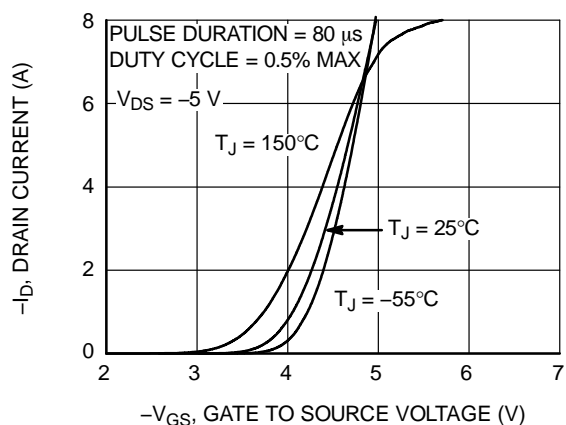


Figure 5. Transfer Characteristics

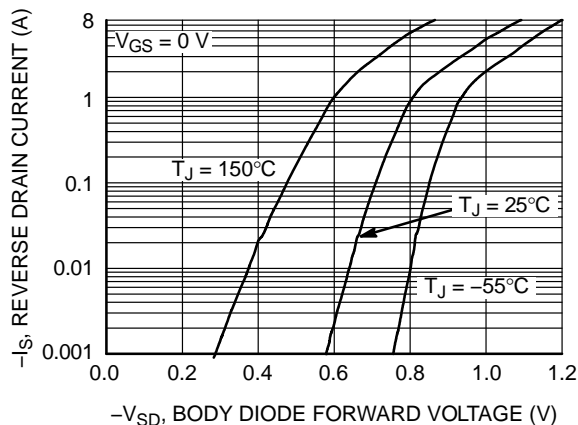


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

TYPICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED) (CONTINUED)

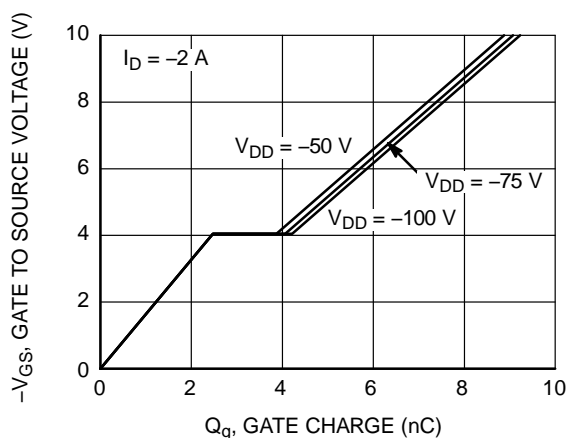


Figure 7. Gate Charge Characteristics

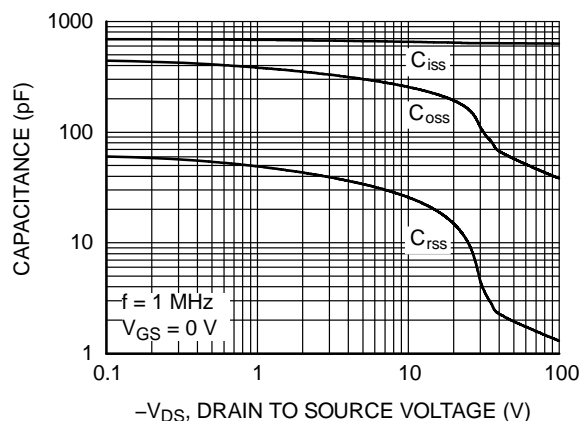


Figure 8. Capacitance vs. Drain to Source Voltage

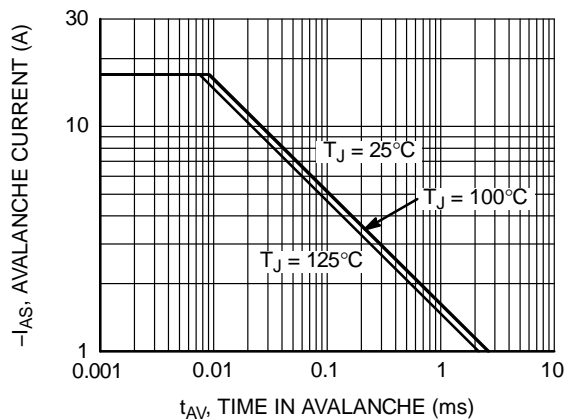


Figure 9. Unclamped Inductive Switching Capability

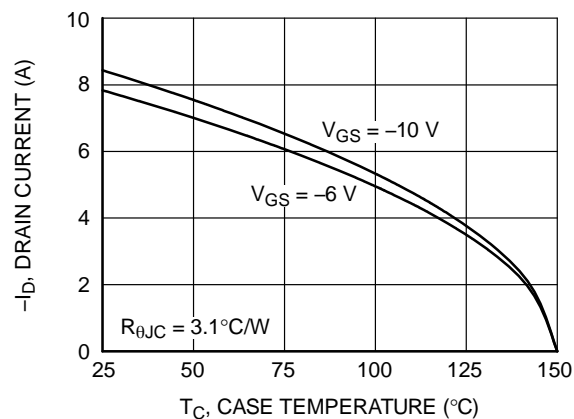


Figure 10. Maximum Continuous Drain Current vs. Case Temperature

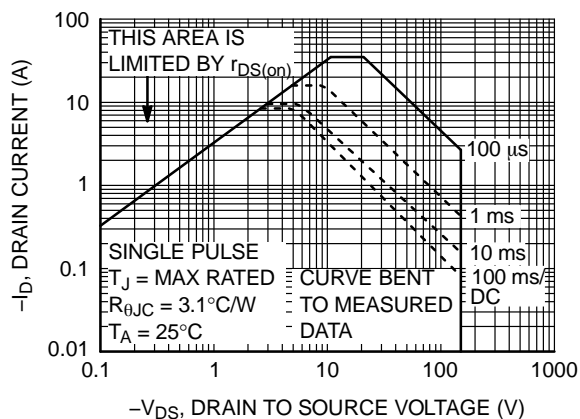


Figure 11. Forward Bias Safe Operating Area

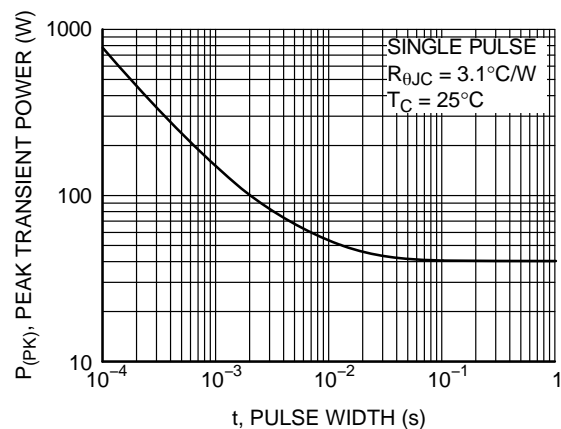


Figure 12. Single Pulse Maximum Power Dissipation

TYPICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED) (CONTINUED)

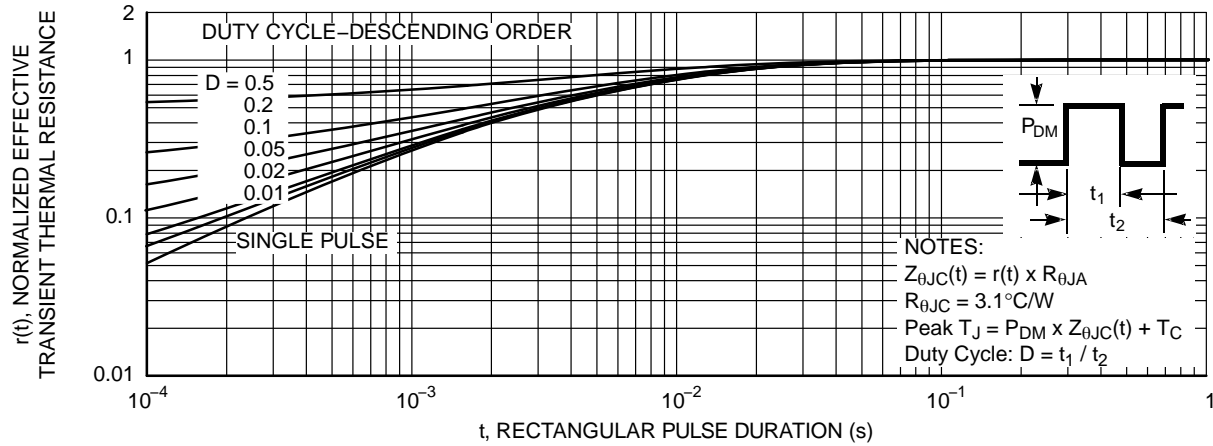


Figure 13. Junction-to-Ambient Transient Thermal Response Curve

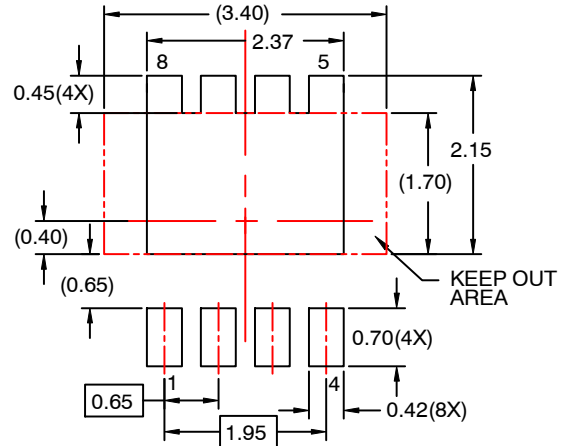
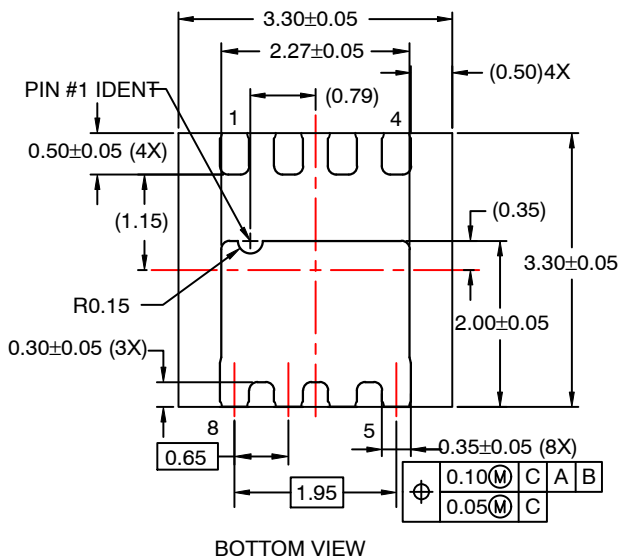
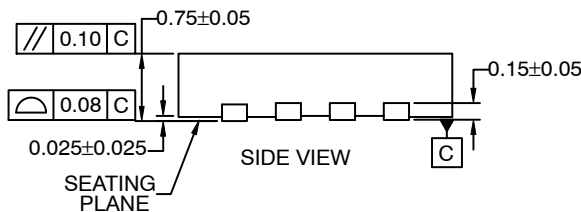
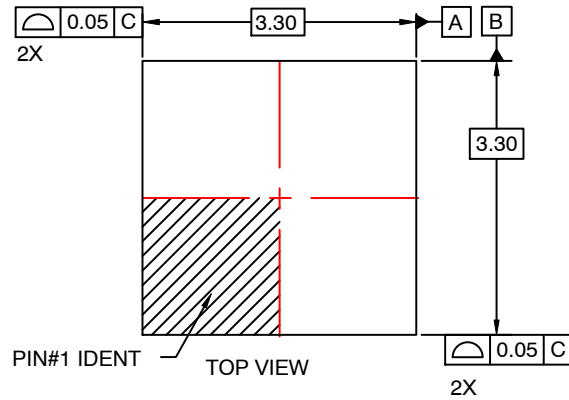
PACKAGE MARKING AND ORDERING INFORMATION

Device	Device Marking	Package Type	Reel Size	Tape Width	Shipping [†]
FDMC86262P	FDMC86262P	WDFN8 3.3x3.3, 0.65P Power 33 (Pb-Free, Halide Free)	13"	12 mm	3000 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

WDFN8 3.3x3.3, 0.65P
CASE 511DH
ISSUE O

DATE 31 JUL 2016


RECOMMENDED LAND PATTERN
NOTES:

- A. DOES NOT CONFORM TO JEDEC REGISTRATION MO-229
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.
- D. LAND PATTERN RECOMMENDATION IS EXISTING INDUSTRY LAND PATTERN.

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DESCRIPTION:	WDFN8 3.3X3.3, 0.65P	PAGE 1 OF 1

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