

# FDMD8430

## Dual N-Channel PowerTrench<sup>®</sup> MOSFET

30 V, 28 A, 2.12 mΩ

### General Description

This package integrates two N-Channel devices connected internally in common-source configuration. This enables very low package parasitics and optimized thermal path to the common source pad on the bottom. Provides a very small footprint (3.3 x 5 mm) for higher power density.

### Features

- Max  $r_{DS(on)}$  = 2.12 mΩ at  $V_{GS} = 10\text{ V}$ ,  $I_D = 28\text{ A}$
- Max  $r_{DS(on)}$  = 2.95 mΩ at  $V_{GS} = 4.5\text{ V}$ ,  $I_D = 24\text{ A}$
- Ideal for Flexible Layout in Secondary Side Synchronous Rectification
- 100% UIL Tested
- Termination is Lead-free and RoHS Compliant

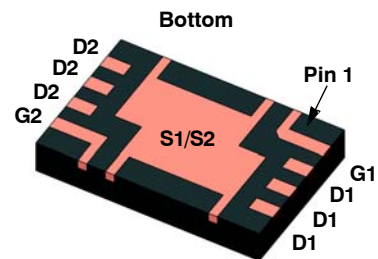
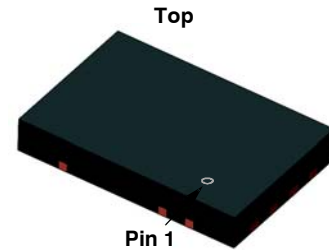
### Applications

- Isolated DC-DC Synchronous Rectifiers
- Common Ground Load Switches

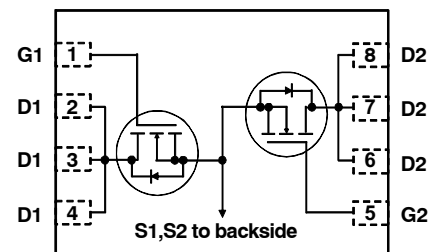


ON Semiconductor<sup>®</sup>

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PQFN8  
PowerTrench  
CASE 483AU



### ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

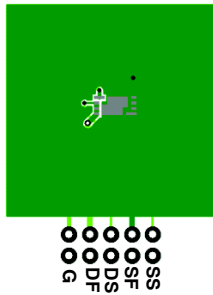
# FDMD8430

**Table 1. MOSFET MAXIMUM RATINGS**  $T_A = 25^\circ\text{C}$  unless otherwise noted.

Symbol	Parameter	Rating	Units
$V_{DS}$	Drain to Source Voltage	30	V
$V_{GS}$	Gate to Source Voltage	$\pm 20$	V
$I_D$	Drain Current – Continuous	$T_C = 25^\circ\text{C}$ (Note 1)	95
	– Continuous	$T_C = 100^\circ\text{C}$ (Note 1)	60
	– Continuous	$T_A = 25^\circ\text{C}$ (Figure 1)	28
	– Pulsed	(Note 2)	562
$E_{AS}$	Single Pulse Avalanche Energy	(Note 3)	96
$P_D$	Power Dissipation	$T_C = 25^\circ\text{C}$	29
	Power Dissipation	$T_A = 25^\circ\text{C}$ (Figure 1)	2.1
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	$-55$ to $+150$	$^\circ\text{C}$

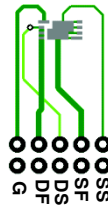
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Computed continuous current limited to Max Junction Temperature only, actual continuous current will be limited by thermal & electro-mechanical application board design.
2. Pulse  $I_D$  refers to Figure 13 Forward Bias Safe Operating Area.
3.  $E_{AS}$  of 96 mJ is based on starting  $T_J = 25^\circ\text{C}$ ;  $L = 0.3$  mH,  $I_{AS} = 31.7$  A,  $V_{DD} = 27$  V.



a.  $60^\circ\text{C/W}$  when mounted on a  $1\text{in}^2$  pad of 2 oz copper

**Figure 1.**



b.  $160^\circ\text{C/W}$  when mounted on a minimum pad of 2 oz copper

**Figure 2.**

**Table 2. THERMAL CHARACTERISTICS**

$R_{\theta JC}$	Thermal Resistance, Junction to Case	4.7	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Figure 1)	60	

4.  $R_{\theta JA}$  is determined with the device mounted on a  $1\text{in}^2$  pad 2 oz copper pad on a  $1.5 \times 1.5$  in. board of FR-4 material,  $R_{\theta CA}$  is determined by the user's board design.

**Table 3. PACKAGE MARKING AND ORDERING INFORMATION**

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMD8430	FDMD8430	Power 3.3 x 5	13"	12 mm	3000 units

# FDMD8430

**Table 4. ELECTRICAL CHARACTERISTICS**  $T_J = 25^\circ\text{C}$  unless otherwise noted.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
<b>OFF CHARACTERISTICS</b>						
$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = 250 \mu\text{A}$ , $V_{GS} = 0 \text{ V}$	30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250 \mu\text{A}$ , referenced to $25^\circ\text{C}$		17		mV/ $^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 24 \text{ V}$ , $V_{GS} = 0 \text{ V}$			1	$\mu\text{A}$
$I_{GSS}$	Gate to Source Leakage Current	$V_{GS} = \pm 20 \text{ V}$ , $V_{DS} = 0 \text{ V}$			$\pm 100$	nA

**ON CHARACTERISTICS**

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$ , $I_D = 250 \mu\text{A}$	1.0	1.6	3.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250 \mu\text{A}$ , referenced to $25^\circ\text{C}$		-5		mV/ $^\circ\text{C}$
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10 \text{ V}$ , $I_D = 28 \text{ A}$		1.5	2.12	m $\Omega$
		$V_{GS} = 4.5 \text{ V}$ , $I_D = 24 \text{ A}$		2.0	2.95	
		$V_{GS} = 10 \text{ V}$ , $I_D = 28 \text{ A}$ , $T_J = 125^\circ\text{C}$		1.7	2.4	
$g_{FS}$	Forward Transconductance	$V_{DD} = 5 \text{ V}$ , $I_D = 28 \text{ A}$			250	S

**DYNAMIC CHARACTERISTICS**

$C_{iss}$	Input Capacitance	$V_{DS} = 15 \text{ V}$ , $V_{GS} = 0 \text{ V}$ , $f = 1 \text{ MHz}$		3595	5035	pF
$C_{oss}$	Output Capacitance			1150	1610	pF
$C_{rss}$	Reverse Transfer Capacitance			112	160	pF
$R_g$	Gate Resistance			2.3	4.5	$\Omega$

**SWITCHING CHARACTERISTICS**

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 15 \text{ V}$ , $I_D = 28 \text{ A}$ , $V_{GS} = 10 \text{ V}$ , $R_{GEN} = 6 \Omega$		11	20	ns
$t_r$	Rise Time			8	16	ns
$t_{d(off)}$	Turn-Off Delay Time			71	114	ns
$t_f$	Fall Time			20	36	ns
$Q_{g(tot)}$	Total Gate Charge	$V_{GS} = 0 \text{ V to } 10 \text{ V}$	$V_{DD} = 15 \text{ V}$ , $I_D = 28 \text{ A}$	52	90	nC
	Total Gate Charge	$V_{GS} = 0 \text{ V to } 4.5 \text{ V}$		25	45	nC
$Q_{gs}$	Gate to Source Charge			10		nC
$Q_{gd}$	Gate to Drain "Miller" Charge			7		nC

**DRAIN-SOURCE DIODE CHARACTERISTICS**

$V_{SD}$	Source to Drain Diode Forward Voltage	$V_{GS} = 0 \text{ V}$ , $I_S = 28 \text{ A}$ (Note 5)		0.8	1.2	V
$t_{rr}$	Reverse Recovery Time	$I_F = 28 \text{ A}$ , $di/dt = 100 \text{ A}/\mu\text{s}$		40	64	ns
$Q_{rr}$	Reverse Recovery Charge			22	36	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. Pulse Test: Pulse Width < 300  $\mu\text{s}$ , Duty Cycle < 2.0%.

TYPICAL CHARACTERISTICS  $T_J = 25^\circ\text{C}$  unless otherwise noted.

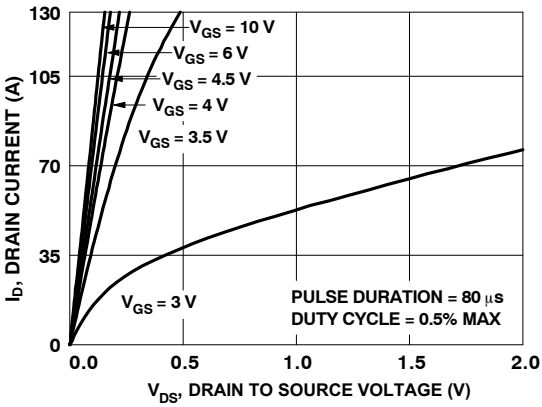


Figure 3. On Region Characteristics

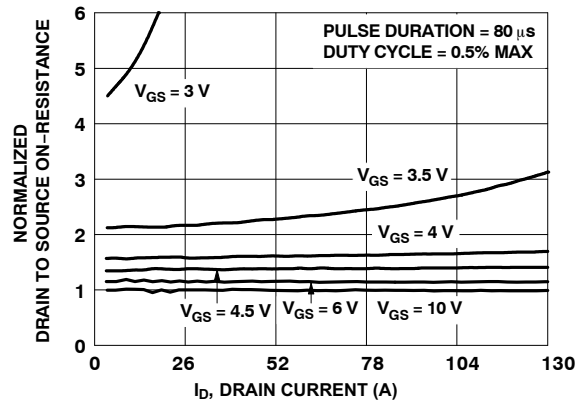


Figure 4. Normalized On-Resistance vs. Drain Current and Gate Voltage

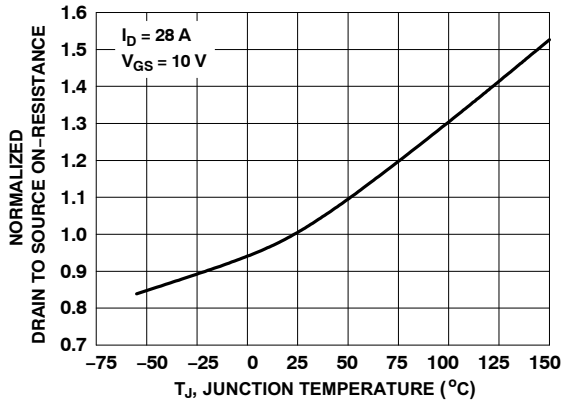


Figure 5. Normalized On-Resistance vs. Junction Temperature

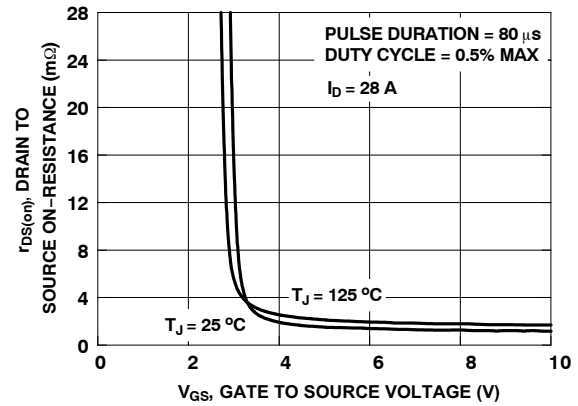


Figure 6. On-Resistance vs. Gate to Source Voltage

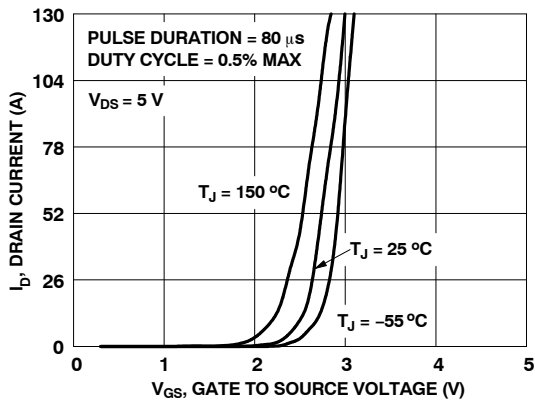


Figure 7. Transfer Characteristics

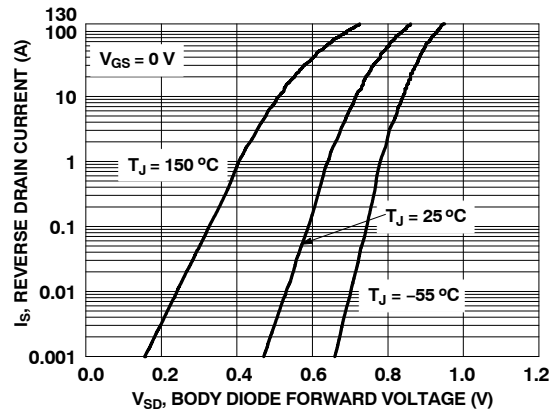


Figure 8. Source to Drain Diode Forward Voltage vs. Source Current

TYPICAL CHARACTERISTICS  $T_J = 25^\circ\text{C}$  unless otherwise noted.

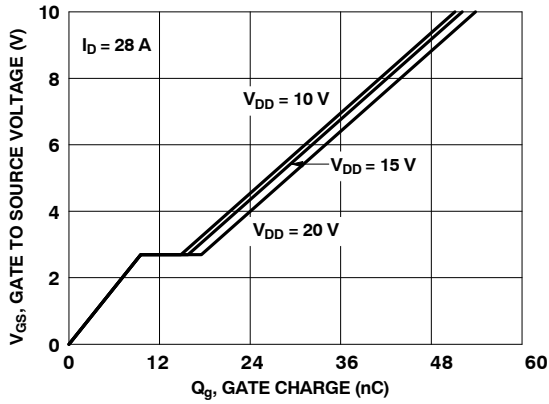


Figure 9. Gate Charge Characteristics

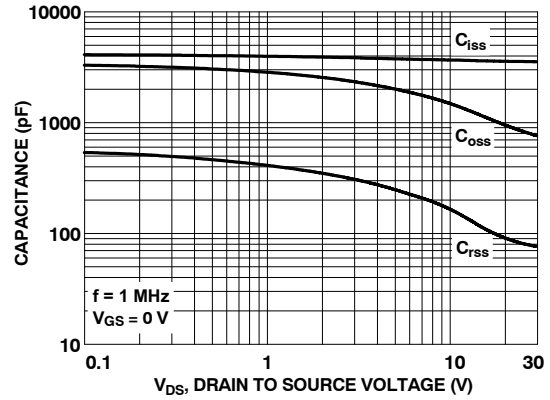


Figure 10. Capacitance vs. Drain to Source Voltage

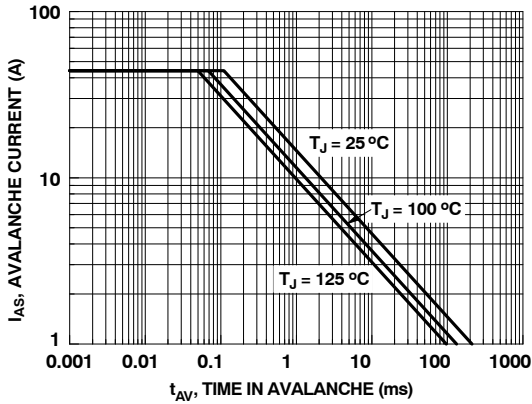


Figure 11. Unclamped Inductive Switching Capability

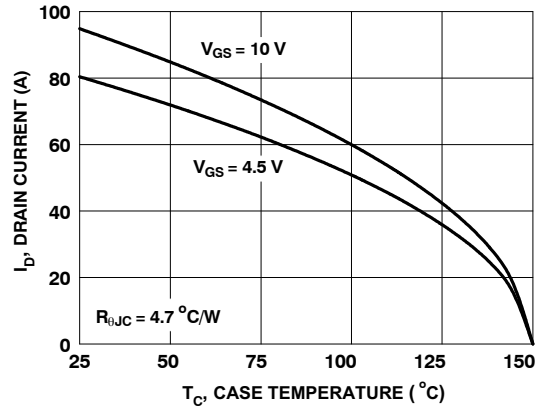


Figure 12. Maximum Continuous Drain Current vs. Case Temperature

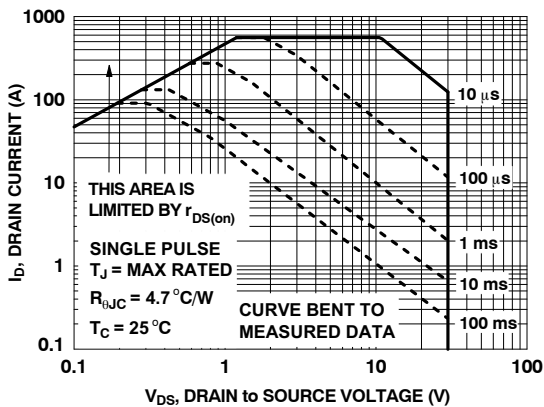


Figure 13. Forward Bias Safe Operating Area

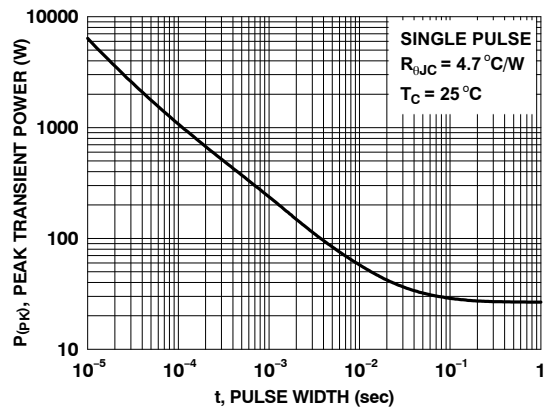


Figure 14. Single Pulse Maximum Power Dissipation

# FDMD8430

TYPICAL CHARACTERISTICS  $T_J = 25^\circ\text{C}$  unless otherwise noted.

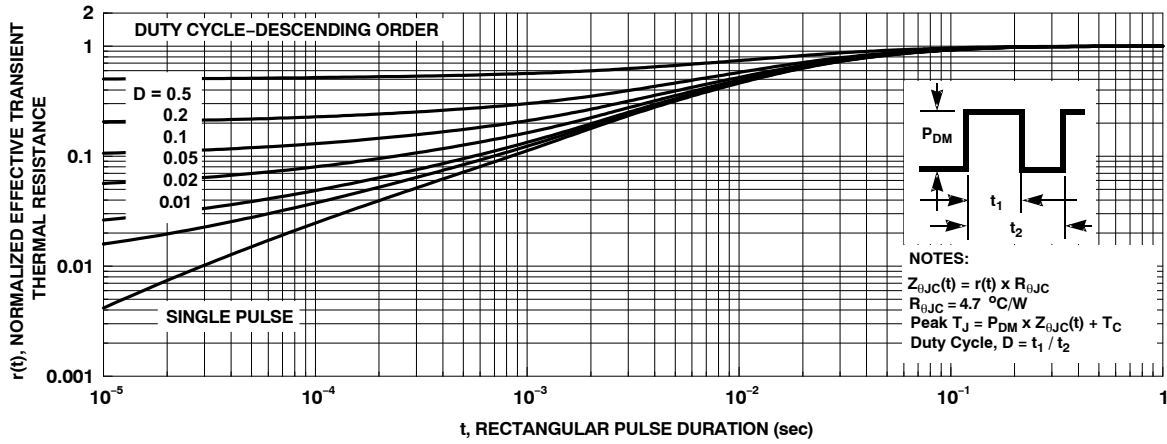
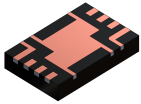


Figure 15. Junction-to-Case Transient Thermal Response Curve

# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

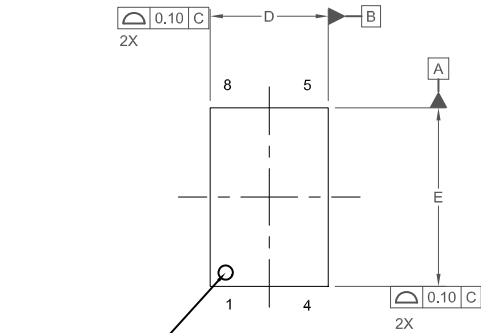


### PQFN8 3.30x5.00x0.75, 0.65P

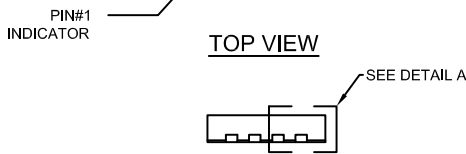
#### CASE 483AU

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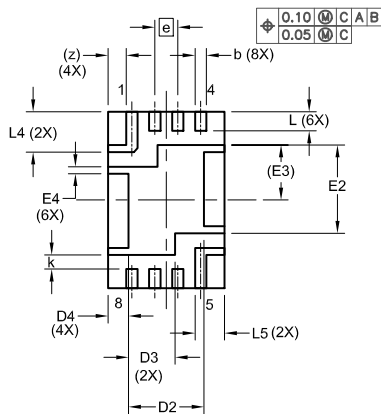
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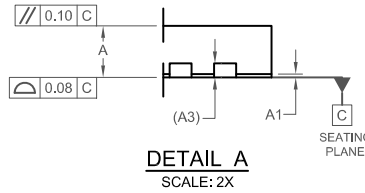
TOP VIEW



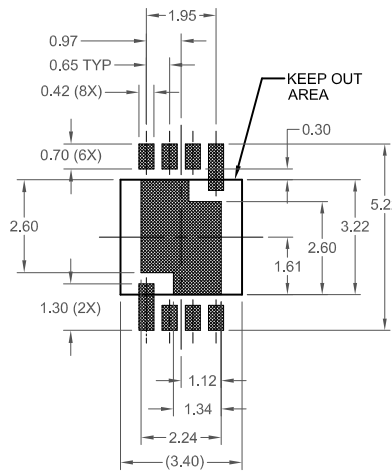
FRONT VIEW



BOTTOM VIEW



DETAIL A  
SCALE: 2X



RECOMMENDED LAND PAD

NOTES: UNLESS OTHERWISE SPECIFIED  
 A) DOES NOT FULLY CONFORM TO JEDEC REGISTRATION, MO229 DATED 8/2012.  
 B) ALL DIMENSIONS ARE IN MILLIMETERS.  
 C) DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.  
 D) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.  
 E) IT IS RECOMMENDED TO HAVE NO TRACES OR VIAS WITHIN THE KEEP OUT AREA.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.00	-	0.05
A3	0.20 REF		
b	0.27	0.32	0.37
D	3.20	3.30	3.40
D2	2.04	2.14	2.24
D3	1.22	1.32	1.42
D4	0.48	0.58	0.68
E	4.90	5.00	5.10
E2	2.40	2.50	2.60
E3	1.56 REF		
E4	0.10	0.20	0.30
e	0.65 BSC		
k	0.30	0.40	0.50
L	0.44	0.54	0.64
L4	1.04	1.14	1.24
L5	0.75	0.85	0.95
z	0.51 REF		

\*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ONSEMI SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

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