

MOSFET – P-Channel POWERTRENCH®

-20 V, -8 A, 24 mΩ

FDME910PZT, FDME910PZT-P, FDME910PZT-P-Q

General Description

This device is designed specifically for battery charging or load switching in cellular handset and other ultraportable applications. It features a MOSFET with low on-state resistance and zener diode protection against ESD. The MicroFET™ 1.6x1.6 Thin package offers exceptional thermal performance for its physical size and is well suited to switching and linear mode applications.

Features

- Max $R_{DS(on)}$ = 24 mΩ at $V_{GS} = -4.5$ V, $I_D = -8$ A
- Max $R_{DS(on)}$ = 31 mΩ at $V_{GS} = -2.5$ V, $I_D = -7$ A
- Max $R_{DS(on)}$ = 45 mΩ at $V_{GS} = -1.8$ V, $I_D = -6$ A
- Low Profile: 0.55 mm Maximum in the New Package MicroFET 1.6x1.6 Thin
- HBM ESD Protection Level > 2 kV typical (Note 3)
- Free from Halogenated Compounds and Antimony Oxides
- These Devices are Pb-Free and are RoHS Compliant

MOSFET MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$, Unless otherwise specified)

Symbol	Parameter	Ratings	Unit
V_{DS}	Drain to Source Voltage	-20	V
V_{GS}	Gate to Source Voltage	± 8	V
I_D	Drain Current Continuous ($T_A = 25^\circ\text{C}$) (Note 1a) Pulsed	-8 -32	A
P_D	Power Dissipation ($T_A = 25^\circ\text{C}$) (Note 1a) ($T_A = 25^\circ\text{C}$) (Note 1b)	2.1 0.7	W
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +150	$^\circ\text{C}$

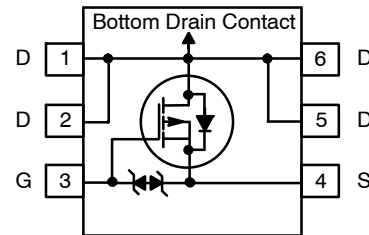
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

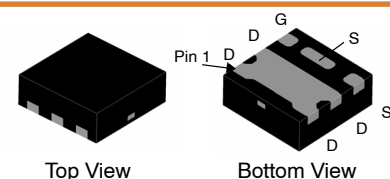
Symbol	Parameter	Ratings	Unit
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	60	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1b)	175	$^\circ\text{C}/\text{W}$

V_{DS}	I_D MAX	$R_{DS(on)}$ MAX
-20 V	-8 A	24 mΩ

ELECTRICAL CONNECTION

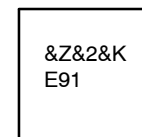


P-Channel MOSFET



MicroFET
(UDFN6)
CASE 517DV

MARKING DIAGRAM



- &Z = Assembly Plant Code
- &2 = 2-Digit Date Code (YW)
- &K = 2-Digit Lot Traceability Code
- E91 = Specific Device Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

FDME910PZT, FDME910PZT-P, FDME910PZT-P-Q

PACKAGE MARKING AND ORDERING INFORMATION

Device	Device Marking	Package	Quantity [†]
FDME910PZT	E91	MicroFET 1.6x1.6 Thin (Pb-Free / Halide Free)	5,000 Units / Tape & Reel
FDME910PZT-P	E91	MicroFET 1.6x1.6 Thin (Pb-Free / Halide Free)	5,000 Units / Tape & Reel
FDME910PZT-P-Q	E91	MicroFET 1.6x1.6 Thin (Pb-Free / Halide Free)	5,000 Units / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

B _V DSS	Drain to Source Breakdown Voltage	I _D = -250 μA, V _{GS} = 0 V	-20	-	-	V
ΔB _V DSS/ΔT _J	Breakdown Voltage Temperature Coefficient	I _D = -250 μA, referenced to 25°C	-	-16	-	mV/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = -16 V, V _{GS} = 0 V	-	-	-1	μA
I _{GSS}	Gate to Source Leakage Current, Forward	V _{GS} = ±8 V, V _{DS} = 0 V	-	-	±10	μA

ON CHARACTERISTICS

V _{GS(th)}	Gate to Source Threshold Voltage	V _{GS} = V _{DS} , I _D = -250 μA	-0.4	-0.6	-1.5	V
ΔV _{GS(th)} /ΔT _J	Gate to Source Threshold Voltage Temperature Coefficient	I _D = -250 μA, referenced to 25°C	-	2.7	-	mV/°C
R _{DS(on)}	Static Drain to Source On Resistance	V _{GS} = -4.5 V, I _D = -8 A V _{GS} = -2.5 V, I _D = -7 A V _{GS} = -1.8 V, I _D = -6 A, V _{GS} = -4.5 V, I _D = -8 A, T _J = 125°C	-	20 25 32 26	24 31 45 36	mΩ
g _{FS}	Forward Transconductance	V _{DD} = -5 V, I _D = -8 A	-	38	-	S

DYNAMIC CHARACTERISTICS

C _{iss}	Input Capacitance	V _{DS} = -10 V, V _{GS} = 0 V, f = 1 MHz	-	1586	2110	pF
C _{oss}	Output Capacitance		-	236	355	pF
C _{rss}	Reverse Transfer Capacitance		-	218	330	pF

SWITCHING CHARACTERISTICS

t _{d(on)}	Turn-On Delay Time	V _{DD} = -10 V, I _D = -8 A, V _{GS} = -4.5 V, R _{GEN} = 6 Ω	-	9	18	ns
t _r	Rise Time		-	11	20	ns
t _{d(off)}	Turn-Off Delay Time		-	87	139	ns
t _f	Fall Time		-	46	74	ns
Q _g	Total Gate Charge	V _{GS} = -4.5 V, V _{DD} = -10 V, I _D = -8 A	-	15	21	nC
Q _{gs}	Gate to Source Gate Charge		-	2.2	-	nC
Q _{gd}	Gate to Drain "Miller" Charge		-	3.6	-	nC

DRAIN-SOURCE DIODE CHARACTERISTICS

V _{SD}	Source to Drain Diode Forward Voltage	V _{GS} = 0 V, I _S = -8 A (Note 2)	-0.57	-0.8	-1.2	V
		V _{GS} = 0 V, I _S = -1.8 A (Note 2)	-	-0.7	-1.2	V
t _{rr}	Reverse Recovery Time	I _F = -8 A, di/dt = 100 A/μs	-	17	31	ns
Q _{rr}	Reverse Recovery Charge		-	4.1	10	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

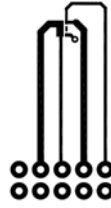
FDME910PZT, FDME910PZT-P, FDME910PZT-P-Q

NOTES:

1. $R_{\theta JA}$ is determined with the device mounted on a 1 in² pad 2 oz copper pad on a 1.5 × 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



- a) 60°C/W when mounted on a 1 in² pad of 2 oz copper.



- b) 175°C/W when mounted on a minimum pad of 2 oz copper.

2. Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.
3. The diode connected between the gate and source serves only as protection ESD. No gate overvoltage rating is implied.

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TYPICAL CHARACTERISTICS

($T_J = 25^\circ\text{C}$ unless otherwise noted)

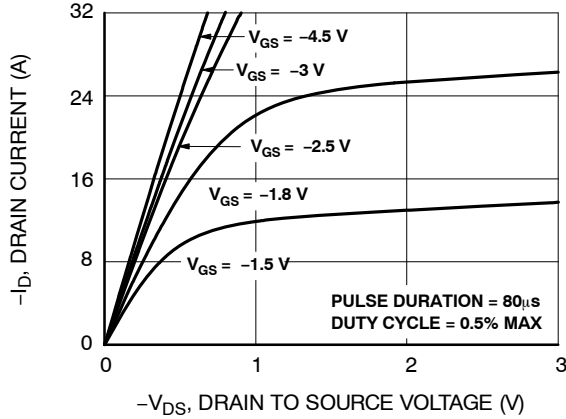


Figure 1. On-Region Characteristics

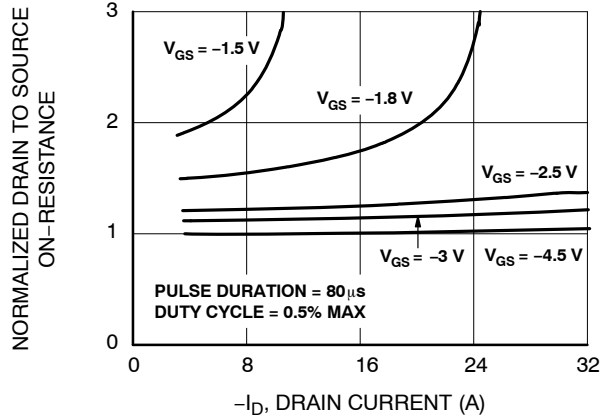


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

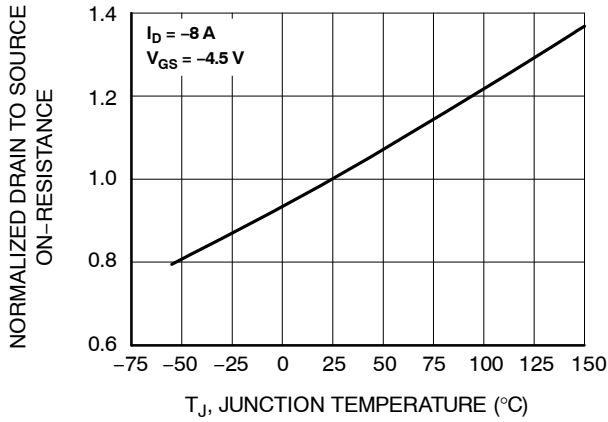


Figure 3. Normalized On Resistance vs. Junction Temperature

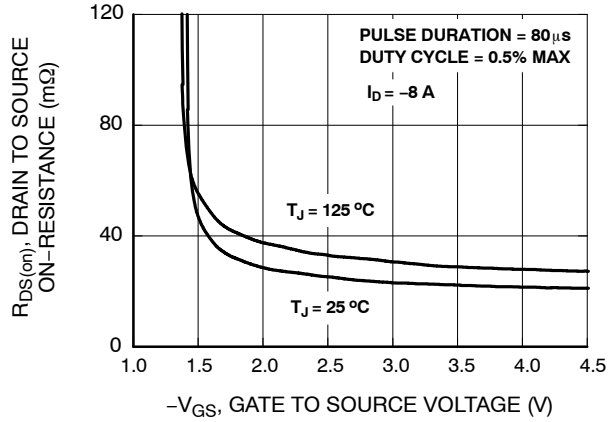


Figure 4. On-Resistance vs. Gate to Source Voltage

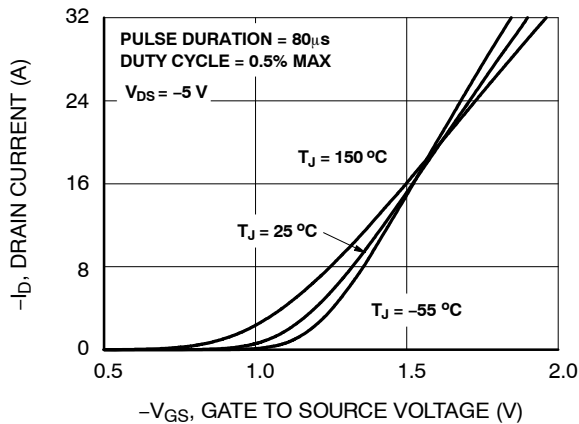


Figure 5. Transfer Characteristics

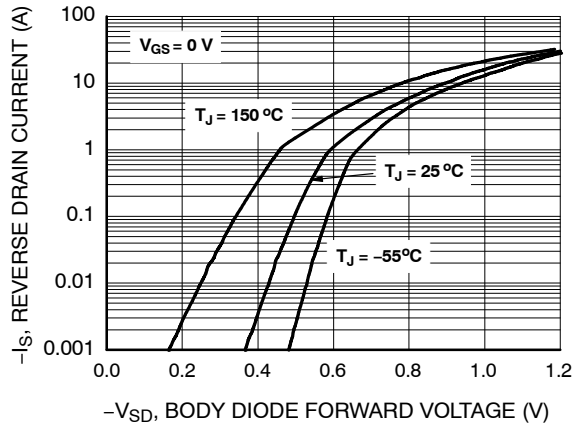


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

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TYPICAL CHARACTERISTICS

($T_J = 25^\circ\text{C}$ unless otherwise noted)

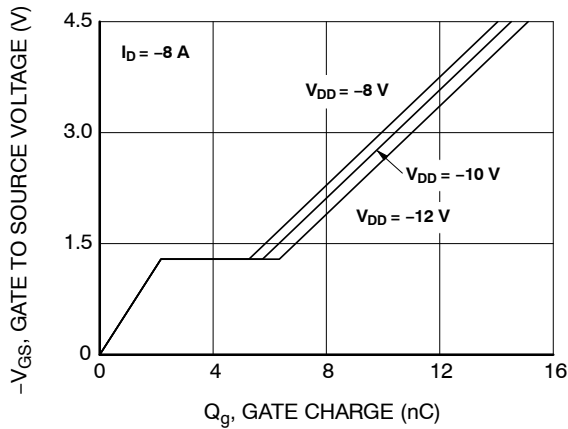


Figure 7. Gate Charge Characteristics

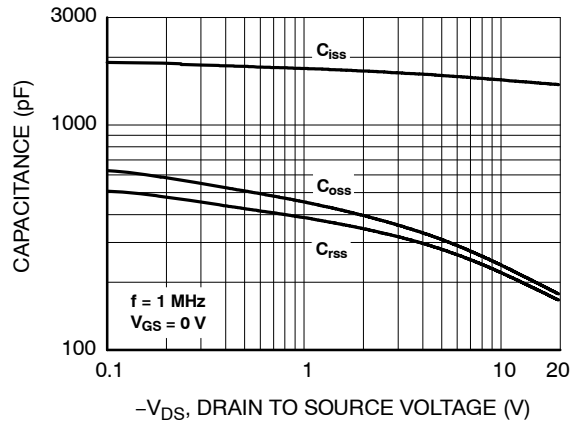


Figure 8. Capacitance vs. Drain to Source Voltage

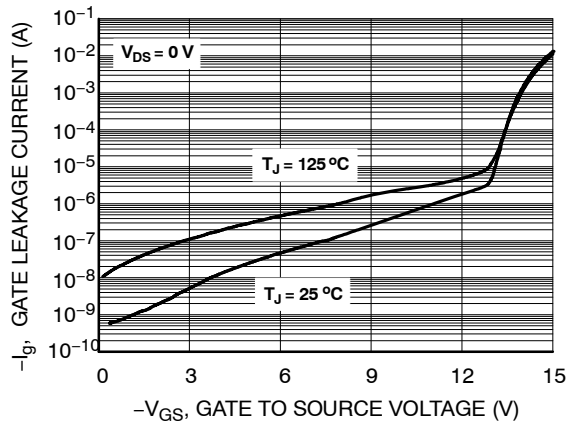


Figure 9. Gate Leakage Current vs. Gate to Source Voltage

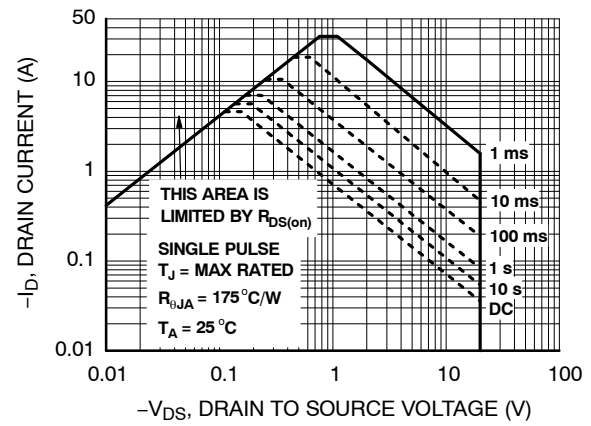


Figure 10. Forward Bias Safe Operating Area

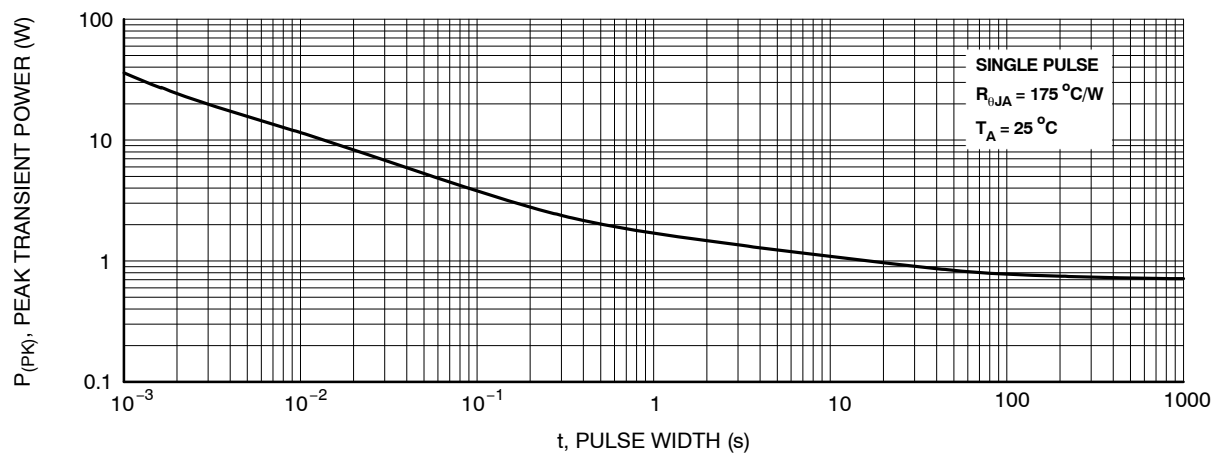


Figure 11. Single Pulse Maximum Power Dissipation

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TYPICAL CHARACTERISTICS

($T_J = 25^\circ\text{C}$ unless otherwise noted)

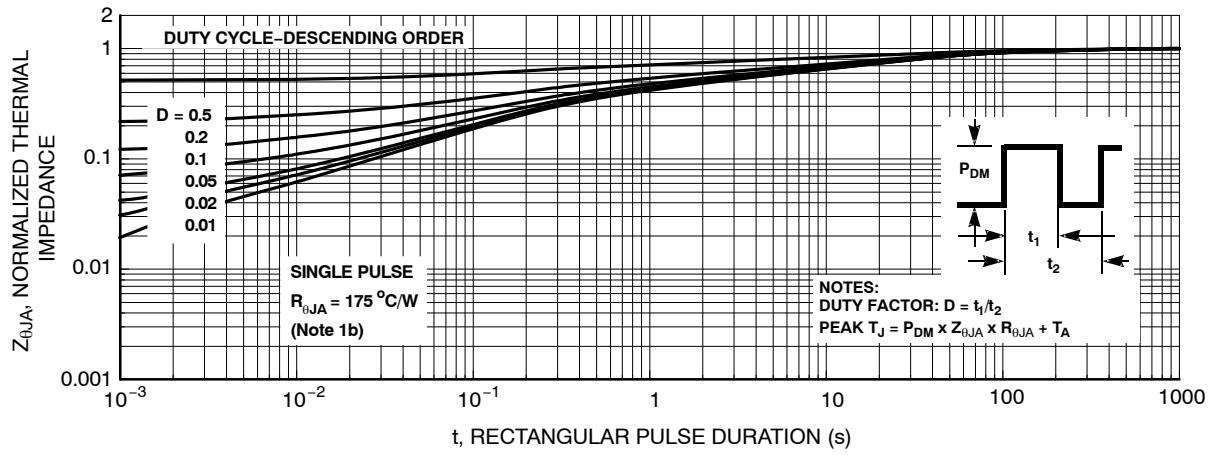


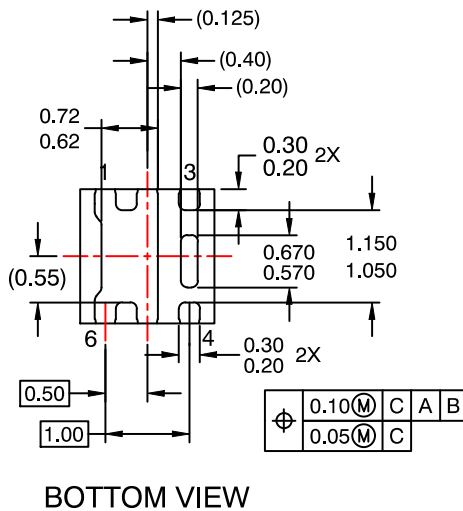
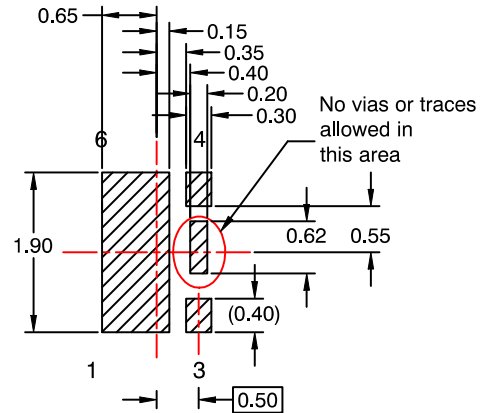
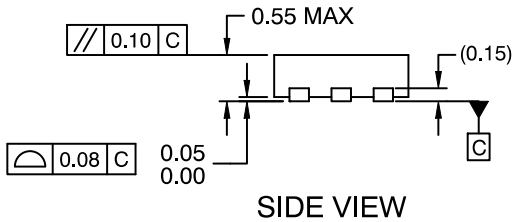
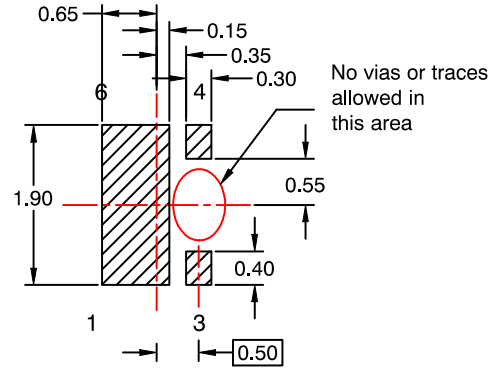
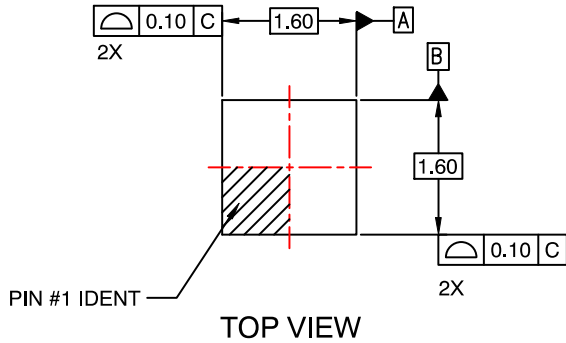
Figure 12. Junction-to-Ambient Transient Thermal Response Curve

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UDFN6 1.6x1.6, 0.5P
CASE 517DV
ISSUE O

DATE 31 OCT 2016



RECOMMENDED LAND PATTERN OPT 2

- NOTES:**
- A. DOES NOT FULLY CONFORM TO JEDEC REGISTRATION
 - B. DIMENSIONS ARE IN MILLIMETERS.
 - C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.

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