MOSFET – N-Channel, POWERTRENCH®

75 V, 49 A, 14.5 mΩ

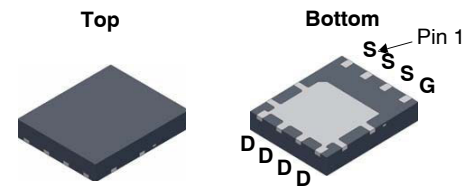## FDMS3500

General Description

This N−Channel MOSFET is produced using **onsemi**'s advanced POWERTRENCH process that has been especially tailored to minimize the on−state resistance and yet maintain superior switching performance.
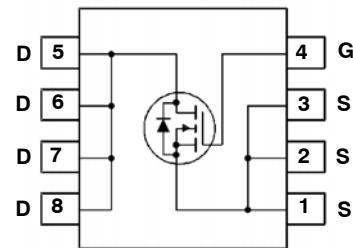
Features

- Max $R_{DS(on)}$ = 14.5 mΩ at V_{GS} = 10 V, I_D = 11.5 A
- Max $R_{DS(on)}$ = 16.3 mΩ at V_{GS} = 4.5 V, I_D = 10 A
- Advanced Package and Silicon Combination for Low $R_{DS(on)}$
- MSL1 Robust Package Design
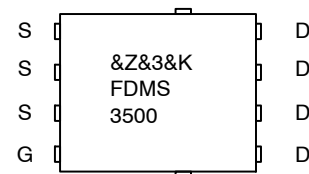- 100% UIL Tested
- RoHS Compliant

Applications

- DC−DC Conversion

Top **Bottom** Pin 1

**Power 56
(PQFN8)
CASE 483AE**

D	5	4	G
D	6	3	S
D	7	2	S
D	8	1	S

MARKING DIAGRAM

S			D
S	&Z&3&K		D
S	FDMS 3500		D
G			D

&Z	= Assembly Plant Code
&3	= Data Code (Year & Week)
&K	= Lot
FDMS3500	= Specific Device Code

ORDERING INFORMATION

Device	Package	Shipping†
FDMS3500	Power 56 (PQFN8) (Pb-Free / Halogen Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Value	Unit
V_{DS}	Drain to Source Voltage	75	V
V_{GS}	Gate to Source Voltage	±20	V
I_D	Drain Current: – Continuous (Package Limit) T_C = 25°C – Continuous (Silicon Limited) T_C = 25C – Continuous T_A = 25°C (Note 1a) – Pulsed	 49 57 9.2 100	A
E_{AS}	Single Pulse Avalanche Energy (Note 3)	384	mJ

P_D	Power Dissipation:
	   T_C = 25°C
	   T_A = 25°C (Note 1a)
		
		96
		2.5
			W

T_J, T_{STG}	Operating and Storage Junction Temperature Range	−55 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case	1.3	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	50	

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 250 μA, V_{GS} = 0 V	75	–	–	V
ΔBV_{DSS} /ΔT_J	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, referenced to 25°C	–	71	–	mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{GS} = 0 V, V_{DS} = 60 V	–	–	1	μA
I_{GSS}	Gate to Source Leakage Current, Forward	V_{GS} = ±20 V, V_{DS} = 0 V	–	–	±100	nA
ON CHARACTERISTICS						
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 250 μA	1.0	1.8	3.0	V
$\Delta V_{GS(th)}$ /ΔT_J	Gate to Source Threshold Voltage Temperature Coefficient	I_D = 250 μA, referenced to 25°C	–	−6.8	–	mV/°C
$R_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = 10 V, I_D = 11.5 A	–	11.1	14.5	mΩ
		V_{GS} = 4.5 V, I_D = 10 A	–	12.8	16.3	
		V_{GS} = 10 V, I_D = 11.5 A, T_J = 125°C	–	17.6	23.0	
g_{FS}	Forward Transconductance	V_{DD} = 5 V, I_D = 11.5 A	–	56	–	S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = 40 V, V_{GS} = 0 V, f = 1 MHz	–	3580	4765	pF
C_{oss}	Output Capacitance		–	225	300	pF
C_{rss}	Reverse Transfer Capacitance		–	120	175	pF
R_g	Gate Resistance	f = 1 MHz	0.1	1.2	–	Ω

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted) (continued)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
SWITCHING CHARACTERISTICS						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 40 V, I_D = 11.5 A, V_{GS} = 10 V, R_{GEN} = 6 Ω	–	16	29	ns
t_r	Rise Time		–	9	18	ns
$t_{d(off)}$	Turn-Off Delay Time		–	48	77	ns
t_f	Fall Time		–	6	11	ns
Q_g	Total Gate Charge	V_{GS} = 0 V to 10 V, V_{DD} = 40 V, I_D = 11.5 A	–	65	91	nC
		V_{GS} = 0 V to 5 V, V_{DD} = 40 V, I_D = 11.5 A	–	34	48	nC
Q_{gs}	Gate to Source Charge	V_{DD} = 50 V, I_D = 44 A	–	9.9	–	nC
Q_{gd}	Gate to Drain "Miller" Charge		–	11.6	–	nC
DRAIN-SOURCE DIODE CHARACTERISTICS						
V_{SD}	Source to Drain Diode Forward Voltage	V_{GS} = 0 V, I_S = 11.5 A (Note 2)	–	0.8	1.3	V
		V_{GS} = 0 V, I_S = 2.1 A (Note 2)	–	0.7	1.2	
t_{rr}	Reverse Recovery Time	I_F = 11.5 A, di/dt = 100 A/μs	–	38	60	ns
Q_{rr}	Reverse Recovery Charge		–	45	72	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTES:
1. $R_{θJA}$ is determined with the device mounted on a 1 in^2 pad 2 oz copper pad on a 1.5 × 1.5 in. board of FR−4 material. $R_{θJC}$ is guaranteed by design while $R_{θCA}$ is determined by the user's board design.
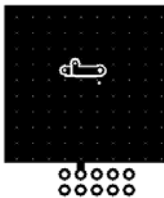
a. 50 °C/W when mounted on a 1 in^2 pad of 2 oz copper.

b. 125 °C/W when mounted on a minimum pad of 2 oz copper.

2. Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.
3. Starting T_J = 25°C, L = 3 mH, I_{AS} = 16 A, V_{DD} = 75 V, V_{GS} = 10 V.

TYPICAL CHARACTERISTICS

(T_J = 25°C unless otherwise noted)
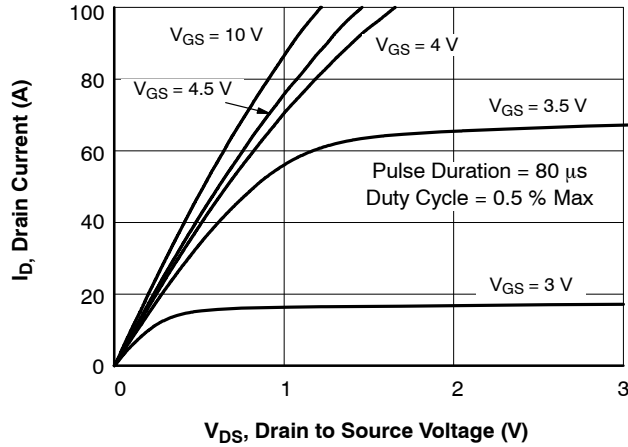
Figure 1. On Region Characteristics
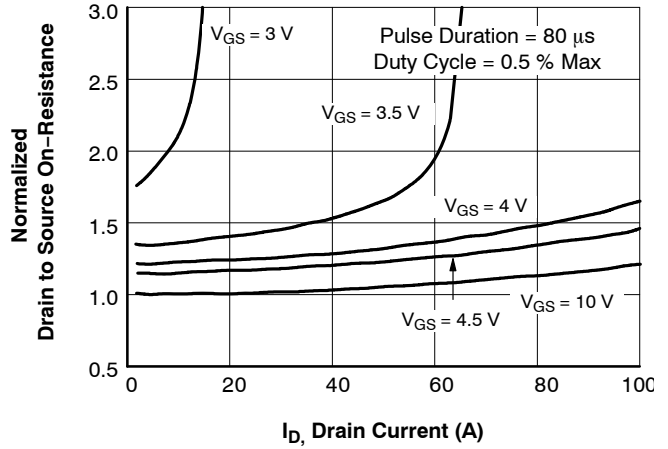
Figure 2. Normalized On−Resistance
vs. Drain Current and Gate Voltage
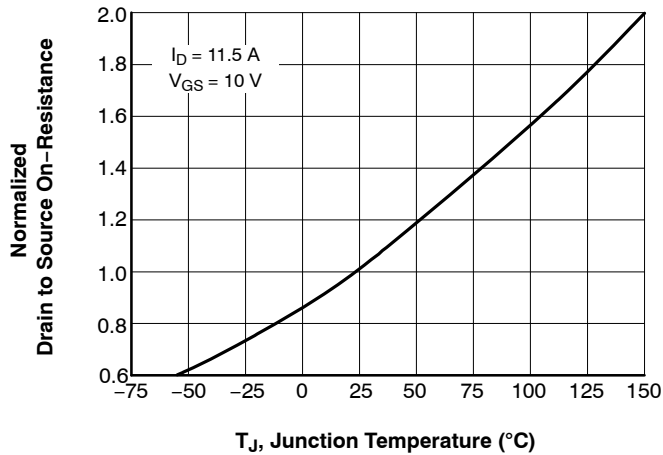
Figure 3. Normalized On Resistance
vs. Junction Temperature
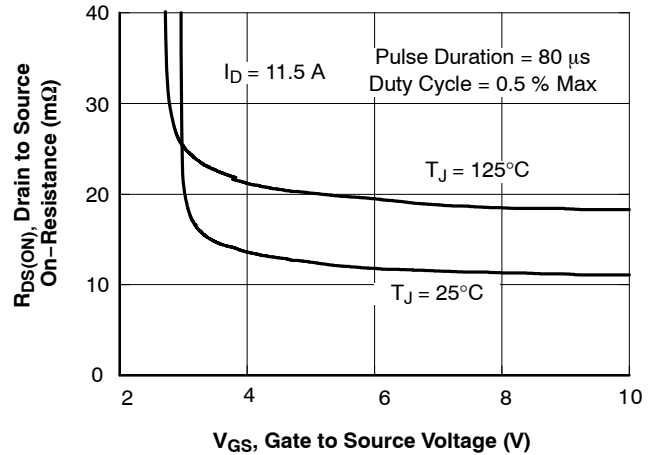
Figure 4. On−Resistance vs. Gate to Source
Voltage
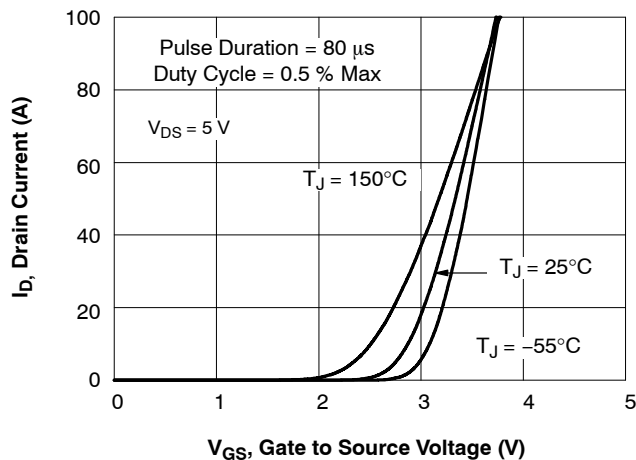
Figure 5. Transfer Characteristics
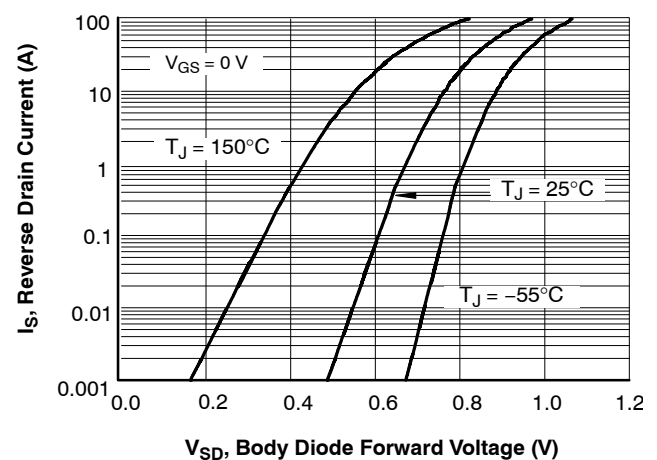
Figure 6. Source to Drain Diode
Forward Voltage vs. Source Current
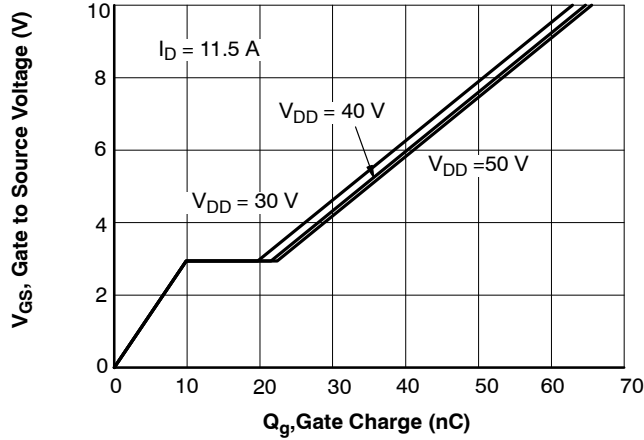
Figure 7. Gate Charge Characteristics
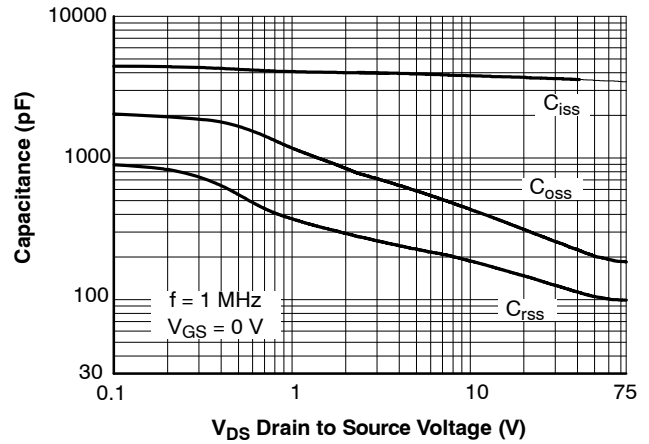
Figure 8. Capacitance vs. Drain
to Source Voltage
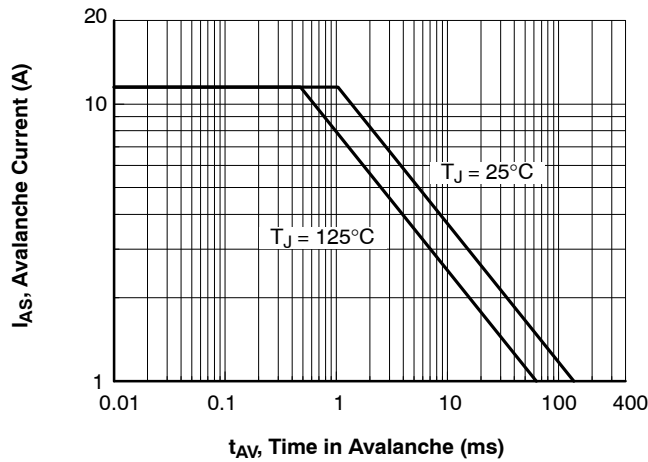
Figure 9. Unclamped Inductive
Switching Capability
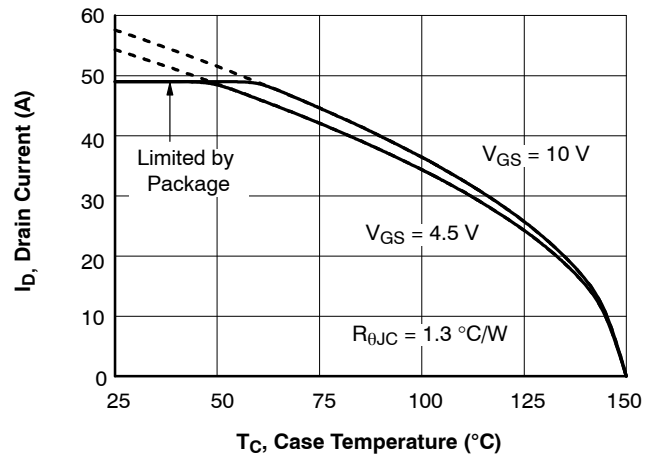
Figure 10. Maximum Continuous Drain
Current vs. Case Temperature
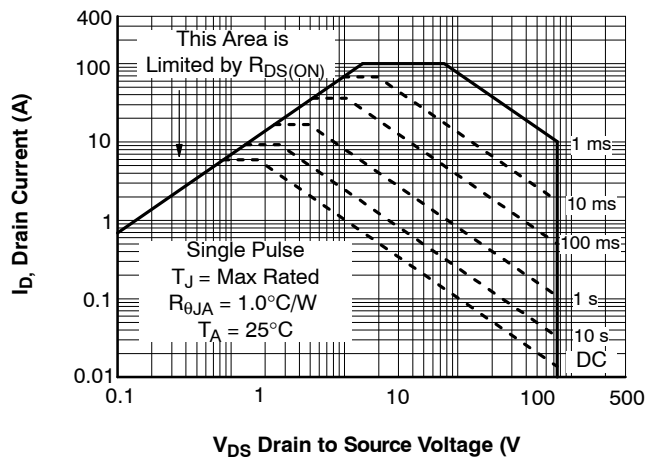
Figure 11. Forward Bias Safe
Operating Area
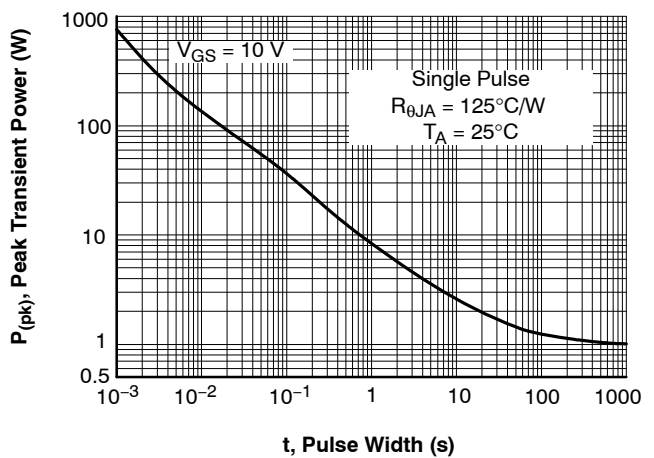
Figure 12. Single Pulse Maximum
Power Dissipation

Figure 13. Transient Thermal Response Curve
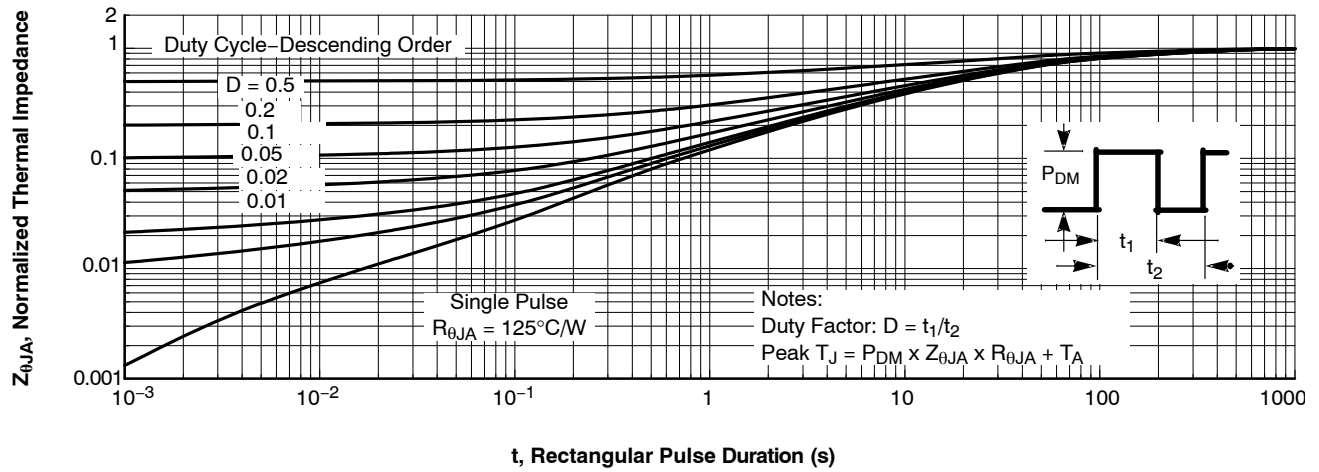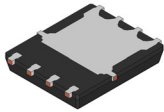
PQFN8 5X6, 1.27P
CASE 483AE
ISSUE C

DATE 21 JAN 2022

TOP VIEW

PIN 1 AREA

SEE DETAIL B

OPTIONAL DRAFT ANGLE MAY APPEAR ON FOUR SIDES OF THE PACKAGE

SIDE VIEW

SEE DETAIL C

DETAIL C
SCALE: 2:1

SEATING PLANE

DETAIL B
SCALE: 2:1

BOTTOM VIEW
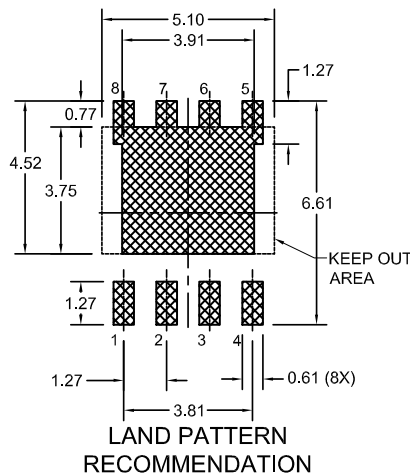
LAND PATTERN RECOMMENDATION

KEEP OUT AREA

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.
4. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
5. SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.
6. IT IS RECOMMENDED TO HAVE NO TRACES OR VIAS WITHIN THE KEEP OUT AREA.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.90	1.00	1.10
A1	0.00	-	0.05
b	0.21	0.31	0.41
b1	0.31	0.41	0.51
A3	0.15	0.25	0.35
D	4.90	5.00	5.20
D1	4.80	4.90	5.00
D2	3.61	3.82	3.96
E	5.90	6.15	6.25
E1	5.70	5.80	5.90
E2	3.38	3.48	3.78
E3	0.30 REF		
E4	0.52 REF		
e	1.27 BSC		
e/2	0.635 BSC		
e1	3.81 BSC		
e2	0.50 REF		
L	0.51	0.66	0.76
L2	0.05	0.18	0.30
L4	0.34	0.44	0.54
z	0.34 REF		
Θ	0°	-	12°

DOCUMENT NUMBER:	98AON13655G		
DESCRIPTION:	**PQFN8 5X6, 1.27P**		**PAGE 1 OF 1**

ADDITIONAL INFORMATION

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