

MOSFET – N-Channel, UltraFET Trench

100 V, 22 A, 23 mΩ

FDMS3672

General Description

UltraFET devices combine characteristics that enable benchmark efficiency in power conversion applications. Optimized for $R_{DS(on)}$, low ESR, low total and Miller gate charge, these devices are ideal for high frequency DC to DC converters.

Features

- Max $R_{DS(on)}$ = 23 mΩ at $V_{GS} = 10$ V, $I_D = 7.4$ A
- Max $R_{DS(on)}$ = 29 mΩ at $V_{GS} = 6$ V, $I_D = 6.6$ A
- Typ Qg = 31 nC at $V_{GS} = 10$ V
- Low Miller Charge
- Optimized Efficiency at High Frequencies
- This Device is Pb-Free, Halide Free and RoHS Compliant

Applications

- DC-DC Conversion

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted.)

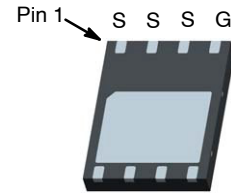
Symbol	Parameter	Value	Unit
V_{DS}	Drain-Source Voltage	100	V
V_{GS}	Gate-Source Voltage	±20	V
I_D	Drain Current – Continuous (Package Limited) $T_C = 25^\circ\text{C}$ – Continuous (Silicon Limited) $T_C = 25^\circ\text{C}$ – Continuous (Note 1a) $T_A = 25^\circ\text{C}$ – Pulsed	22 41 7.4 30	A
P_D	Power Dissipation Power Dissipation (Note 1a)	78 2.5	W
T_J, T_{STG}	Operating and Storage Junction Temperature Range	–55 to +150	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise noted.)

Symbol	Parameter	Value	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case	1.6	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	53	$^\circ\text{C/W}$

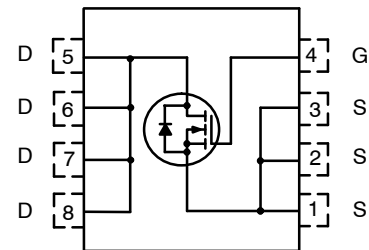
V_{DS}	$R_{DS(on)}$ MAX	I_D MAX
100 V	23 mΩ @ 10 V	22 A
	29 mΩ @ 6 V	



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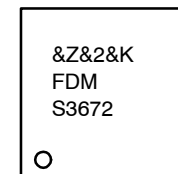
Bottom

WDFN8 5x6, 1.27P
Power 56
CASE 506DP



N-CHANNEL MOSFET

MARKING DIAGRAM



&Z = Assembly Location
 &2 = Date Code
 &K = Lot Run Traceability Code
 FDMS3672 = Specific Device Code

ORDERING INFORMATION

Device	Package	Shipping [†]
FDMS3672	WDFN8 (Pb-Free, Halide Free)	3000 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 250\ \mu\text{A}$, $V_{GS} = 0\ \text{V}$	100	–	–	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$, referenced to 25°C	–	104	–	$\text{mV}/^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 80\ \text{V}$, $V_{GS} = 0\ \text{V}$	–	–	1	μA
		$V_{DS} = 80\ \text{V}$, $V_{GS} = 0\ \text{V}$, $T_J = 55^\circ\text{C}$	–	–	10	
I_{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 20\ \text{V}$, $V_{DS} = 0\ \text{V}$	–	–	± 100	nA

ON CHARACTERISTICS

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = 250\ \mu\text{A}$	2.0	3.1	4.0	V
$\Delta V_{GS(th)} / \Delta T_J$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$, referenced to 25°C	–	–11	–	$\text{mV}/^\circ\text{C}$
$R_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\ \text{V}$, $I_D = 7.4\ \text{A}$	–	19	23	$\text{m}\Omega$
		$V_{GS} = 6\ \text{V}$, $I_D = 6.6\ \text{A}$	–	24	29	
		$V_{GS} = 10\ \text{V}$, $I_D = 7.4\ \text{A}$, $T_J = 125^\circ\text{C}$	–	33	40	
g_{FS}	Forward Transconductance	$V_{DS} = 10\ \text{V}$, $I_D = 7.4\ \text{A}$	–	20	–	S

DYNAMIC CHARACTERISTICS

C_{iss}	Input Capacitance	$V_{DS} = 50\ \text{V}$, $V_{GS} = 0\ \text{V}$, $f = 1\ \text{MHz}$	–	2015	2680	pF
C_{oss}	Output Capacitance		–	210	280	pF
C_{rss}	Reverse Transfer Capacitance		–	90	135	pF
R_g	Gate Resistance	$f = 1\ \text{MHz}$	–	1.3	–	Ω

SWITCHING CHARACTERISTICS

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 50\ \text{V}$, $I_D = 7.4\ \text{A}$, $V_{GS} = 10\ \text{V}$, $R_{GEN} = 6\ \Omega$	–	23	37	ns
t_r	Rise Time		–	11	20	ns
$t_{d(off)}$	Turn-Off Delay Time		–	36	58	ns
t_f	Fall Time		–	8	16	ns
Q_g	Total Gate Charge at 10 V	$V_{GS} = 0\ \text{V}$ to $10\ \text{V}$, $V_{DD} = 50\ \text{V}$, $I_D = 7.4\ \text{A}$	–	31	44	nC
Q_g	Total Gate Charge at 4.5 V	$V_{GS} = 0\ \text{V}$ to $4.5\ \text{V}$, $V_{DD} = 50\ \text{V}$, $I_D = 7\ \text{A}$	–	–	–	nC
Q_{gs}	Gate to Source Charge	$V_{DD} = 50\ \text{V}$, $I_D = 7.4\ \text{A}$	–	9.5	–	nC
Q_{gd}	Gate to Drain "Miller" Charge	$V_{DD} = 50\ \text{V}$, $I_D = 7.4\ \text{A}$	–	8	–	nC

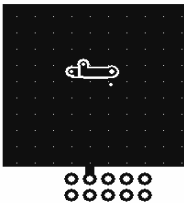
DRAIN-SOURCE DIODE CHARACTERISTICS

V_{SD}	Source to Drain Diode Forward Voltage	$V_{GS} = 0\ \text{V}$, $I_S = 7.4\ \text{A}$ (Note 2)	–	0.8	1.2	V
t_{rr}	Reverse Recovery Time	$I_F = 7.4\ \text{A}$, $di/dt = 100\ \text{A}/\mu\text{s}$	–	52	78	ns
Q_{rr}	Reverse Recovery Charge		–	101	152	nC

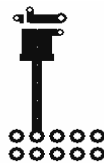
Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTES:

- $R_{\theta JA}$ is determined with the device mounted on a 1 in² pad 2 oz copper pad on a 1.5 × 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a) $50^\circ\text{C}/\text{W}$ when mounted on a 1 in² pad of 2 oz copper.



b) $125^\circ\text{C}/\text{W}$ when mounted on a minimum pad of 2 oz copper.

- Pulse Test: Pulse Width < 300 μs , Duty cycle < 2.0%.

TYPICAL CHARACTERISTICS

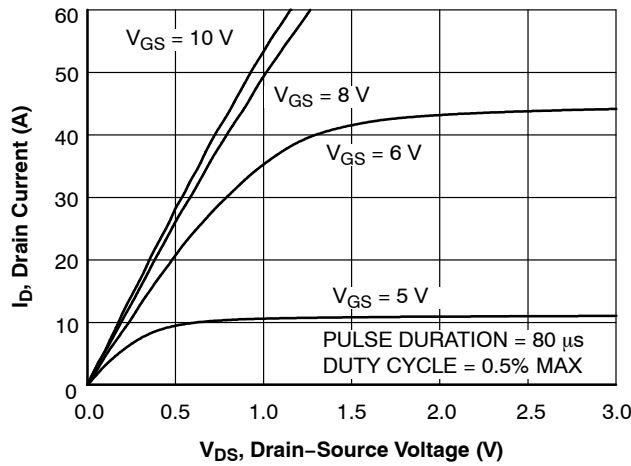
(T_J = 25°C unless otherwise noted)

Figure 1. On-Region Characteristics

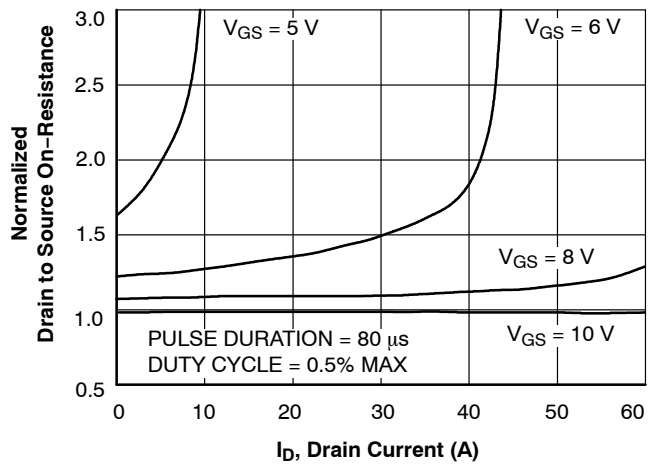


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

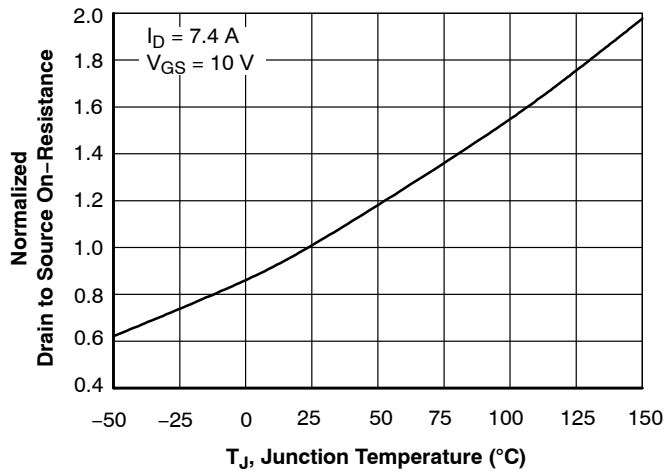


Figure 3. Normalized On-Resistance vs. Junction Temperature

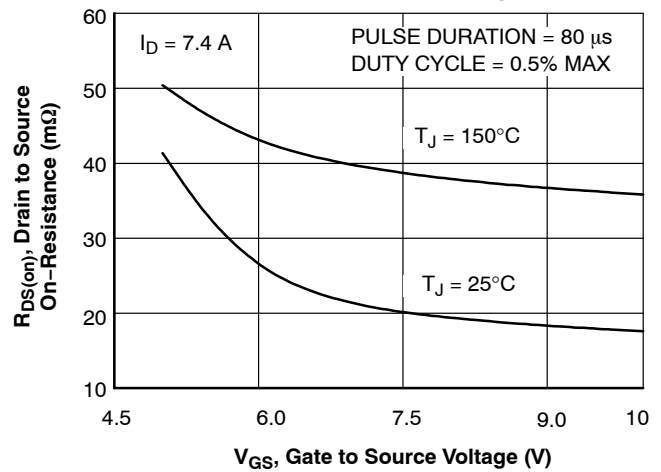


Figure 4. On-Resistance vs. Gate to Source Voltage

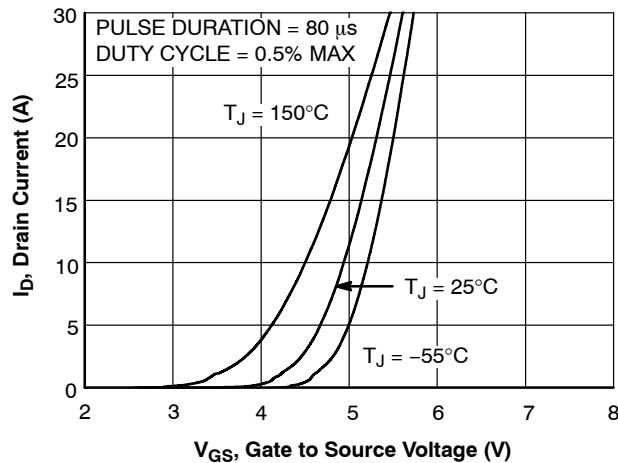


Figure 5. Transfer Characteristics

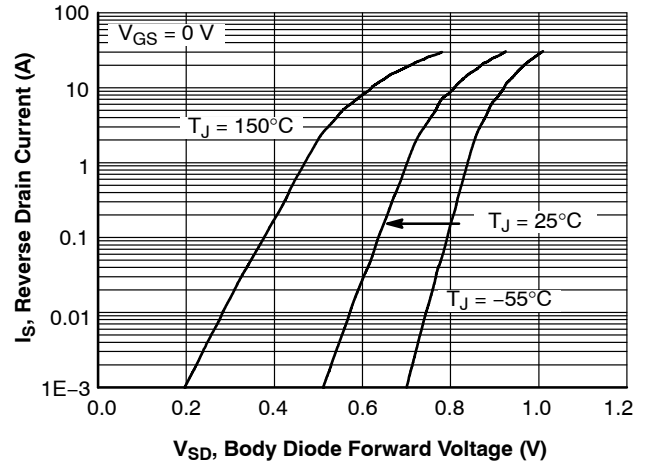


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

TYPICAL CHARACTERISTICS (CONTINUED)

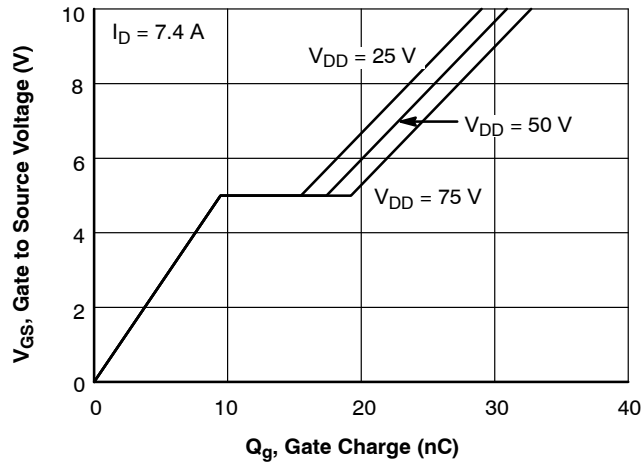
(T_J = 25°C unless otherwise noted)

Figure 7. Gate Charge Characteristics

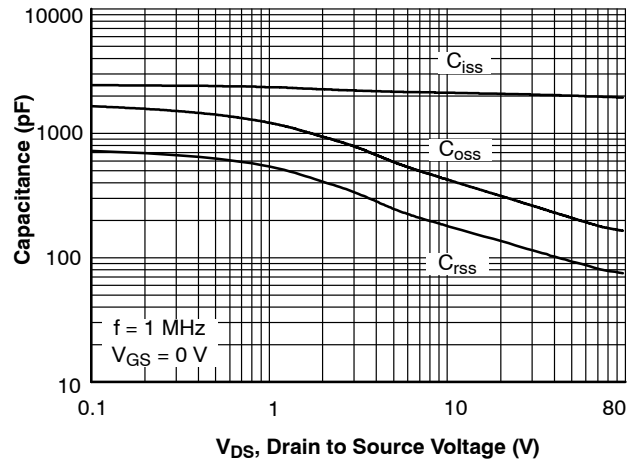


Figure 8. Capacitance vs. Drain to Source Voltage

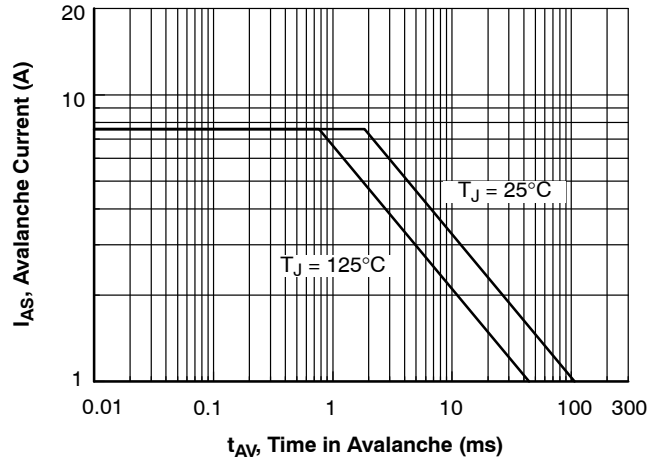


Figure 9. Unclamped Inductive Switching Capability

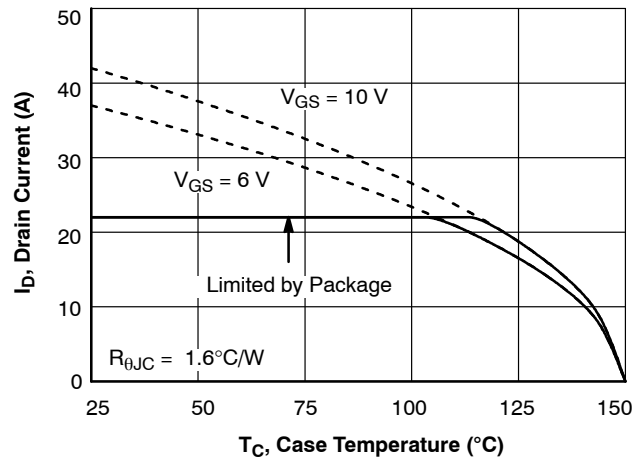


Figure 10. Maximum Continuous Drain Current vs. Case Temperature

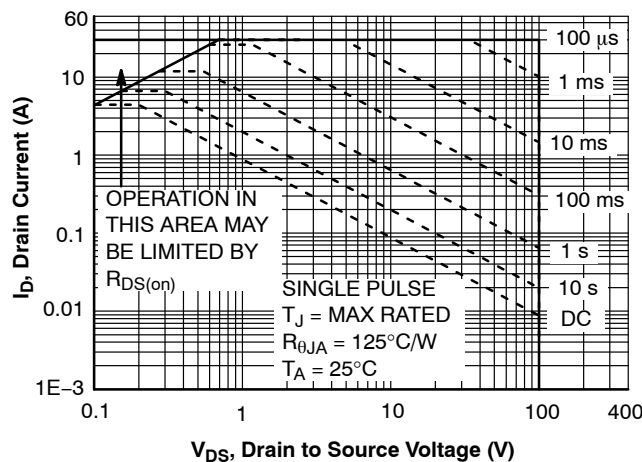


Figure 11. Forward Bias Safe Operating Area

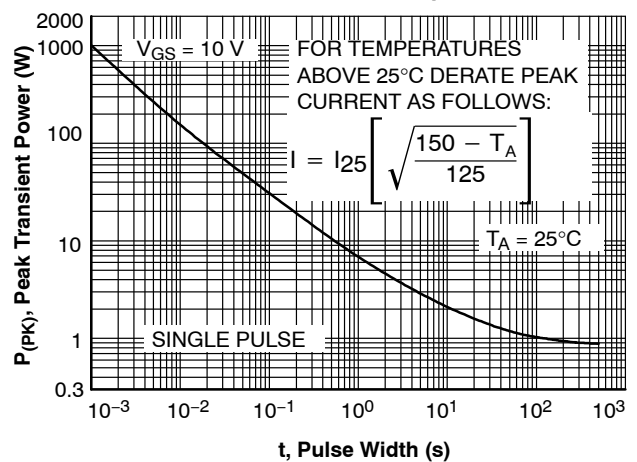


Figure 12. Single Pulse Maximum Power Dissipation

TYPICAL CHARACTERISTICS (CONTINUED)

($T_J = 25^\circ\text{C}$ unless otherwise noted)

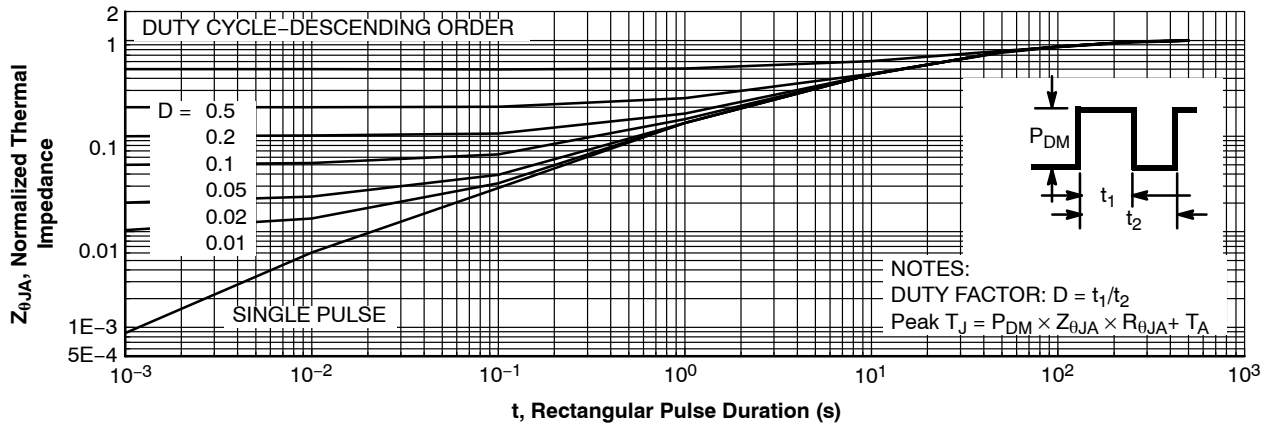
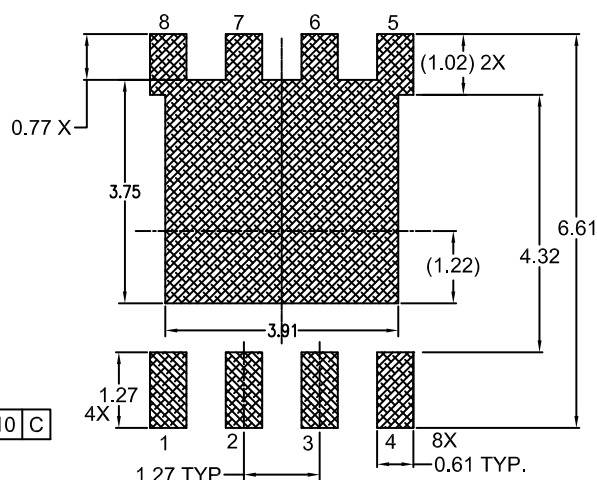
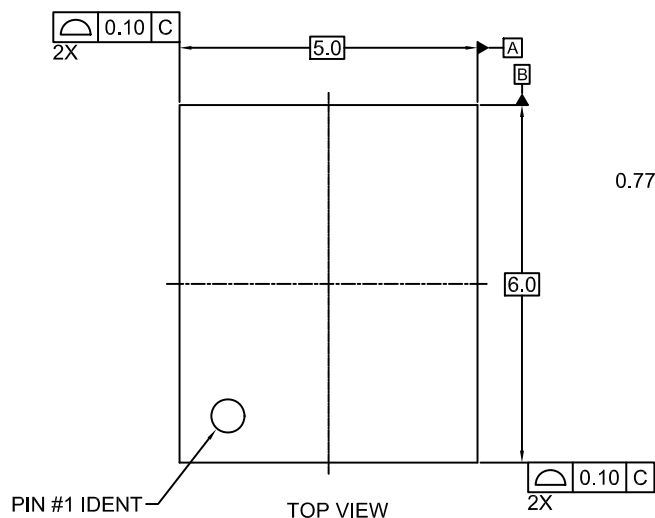


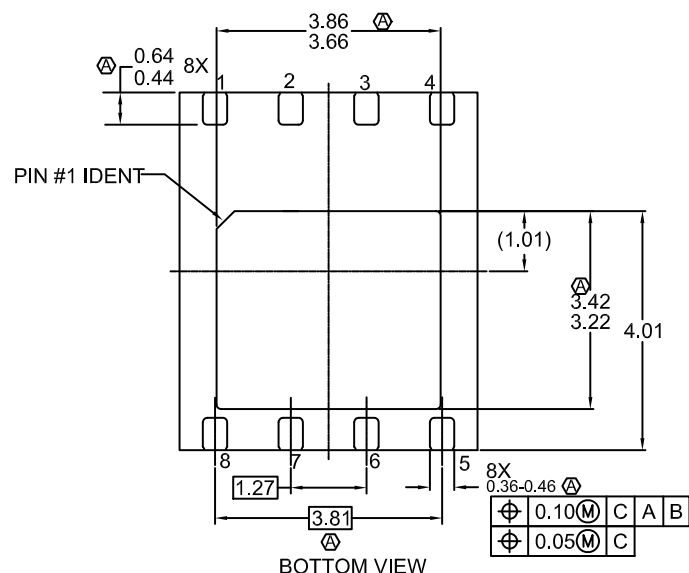
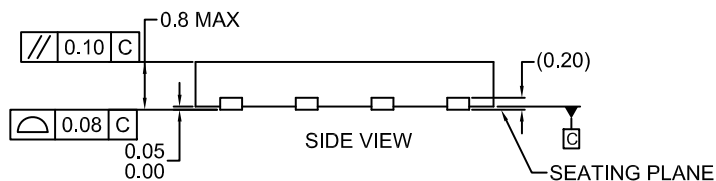
Figure 13. Transient Thermal Response Curve

WDFN8 5x6, 1.27P
CASE 506DP
ISSUE O

DATE 31 AUG 2016



RECOMMENDED LAND PATTERN



NOTES:

- A. DOES NOT FULLY CONFORM TO JEDEC REGISTRATION, MO-229.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994
- D. TERMINALS 5,6,7 AND 8 ARE TIED TO THE EXPOSED PADDLE

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