

MOSFET – Dual N-Channel, POWERTRENCH®

Q1: 30 V, 13 A, 20 mΩ

Q2: 30 V, 22 A, 11.2 mΩ

FDMS7620S

General Description

This device includes two specialized MOSFETs in a unique dual Power 56 package. It is designed to provide an optimal synchronous buck power stage in terms of efficiency and PCB utilization. The low switching loss “High Side” MOSFET is complementary by a low conduction loss “Low Side” SyncFET™.

Features

Q1: N-Channel

- Max $R_{DS(on)}$ = 20.0 mΩ at V_{GS} = 10 V, I_D = 10.1 A
- Max $R_{DS(on)}$ = 30.0 mΩ at V_{GS} = 4.5 V, I_D = 7.5 A

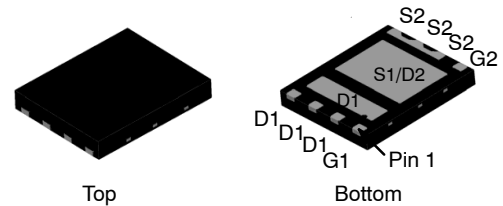
Q2: N-Channel

- Max $R_{DS(on)}$ = 11.2 mΩ at V_{GS} = 10 V, I_D = 12.4 A
- Max $R_{DS(on)}$ = 14.2 mΩ at V_{GS} = 4.5 V, I_D = 10.9 A
- Pinout Optimized for Simple PCB Design
- Thermally Efficient Dual Power 56 Package
- Pb-Free, Halogen Free/BFR Free and RoHS Compliant

Applications

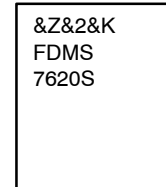
Synchronous Buck Converter for:

- Notebook System Power
- General Purpose Point of Load

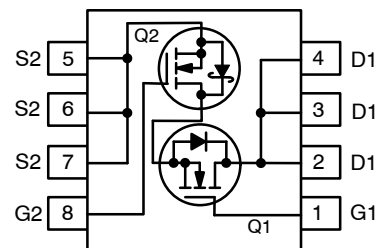


DFN8 5x6, 1.27P,
Power 56
CASE 506DR

MARKING DIAGRAM



&Z = Assembly Plant Code
&2 = 2-Digit Date Code (Year & Week)
&K = 2-Digit Lot Run Traceability Code
FDMS7620S = Specific Device Code



Dual N-Channel MOSFET

ORDERING INFORMATION

See detailed ordering and shipping information on page 11 of this data sheet.

FDMS7620S

MOSFET MAXIMUM RATINGS ($T_A = 25\text{ }^{\circ}\text{C}$ unless otherwise specified)

Symbol	Parameter	Q1	Q2	Unit
V_{DS}	Drain to Source Voltage	30	30	V
V_{GS}	Gate to Source Voltage (Note 3)	± 20	± 20	V
I_D	Drain Current – Continuous $T_C = 25\text{ }^{\circ}\text{C}$	13	22	A
	– Continuous $T_A = 25\text{ }^{\circ}\text{C}$	10.1	12.4	
	– Pulsed	27	45	
E_{AS}	Single Pulse Avalanche Energy (Note 4)	9	21	mJ
P_D	Power Dissipation for Single Operation	$T_A = 25\text{ }^{\circ}\text{C}$ (Note 1a)	2.2	W
		$T_A = 25\text{ }^{\circ}\text{C}$ (Note 1b)	–	
		$T_A = 25\text{ }^{\circ}\text{C}$ (Note 1c)	1.0	
		$T_A = 25\text{ }^{\circ}\text{C}$ (Note 1d)	–	
T_J, T_{STG}	Operating and Storage Junction Temperature Range	–55 to +150		$^{\circ}\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

Symbol	Parameter	Q1	Q2	Unit
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	57	–	$^{\circ}\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1b)	–	50	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1c)	125	–	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1d)	–	120	

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ELECTRICAL CHARACTERISTICS (T_J = 25 °C unless otherwise noted)

Symbol	Parameter	Test Condition	Type	Min.	Typ.	Max.	Unit
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OFF CHARACTERISTICS

BV _{DSS}	Drain to Source Breakdown Voltage	I _D = 250 μA, V _{GS} = 0 V I _D = 1 mA, V _{GS} = 0 V	Q1 Q2	30 30	– –	– –	V
$\frac{\Delta BV_{DSS}}{\Delta T_j}$	Breakdown Voltage Temperature Coefficient	I _D = 250 μA, referenced to 25 °C I _D = 10 mA, referenced to 25 °C	Q1 Q2	– –	19 19	– –	mV/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 24 V, V _{GS} = 0 V	Q1 Q2	– –	– –	1 500	μA
I _{GSS}	Gate to Source Leakage Current, Forward	V _{GS} = 20 V, V _{DS} = 0 V	Q1 Q2	– –	– –	100 100	nA

ON CHARACTERISTICS

V _{GS(th)}	Gate to Source Threshold Voltage	V _{GS} = V _{DS} , I _D = 250 μA V _{GS} = V _{DS} , I _D = 1 mA	Q1 Q2	1.0 1.0	2.2 2.0	3.0 3.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_j}$	Gate to Source Threshold Voltage Temperature Coefficient	I _D = 250 μA, referenced to 25 °C I _D = 10 mA, referenced to 25 °C	Q1 Q2	– –	–6 –5	– –	mV/°C
R _{DS(on)}	Static Drain to Source On Resistance	V _{GS} = 10 V, I _D = 10.1 A V _{GS} = 14.5 V, I _D = 7.5 A V _{GS} = 10 V, I _D = 10 A, T _J = 125 °C	Q1	– – –	15.2 22.7 18.7	20.0 30.0 22.5	mΩ
		V _{GS} = 10 V, I _D = 12.4 A V _{GS} = 4.5 V, I _D = 10.9 A V _{GS} = 10 V, I _D = 12.4 A, T _J = 125 °C	Q2	– – –	8.3 10.5 8.9	11.2 14.2 15.1	
g _{FS}	Forward Transconductance	V _{DD} = 5 V, I _D = 10.1 A V _{DD} = 5 V, I _D = 12.4 A	Q1 Q2	– –	22 53	– –	S

DYNAMIC CHARACTERISTICS

C _{iss}	Input Capacitance	V _{DS} = 15 V, V _{GS} = 0 V, f = 1 MHz	Q1 Q2	– –	457 1050	608 1400	pF
C _{oss}	Output Capacitance		Q1 Q2	– –	167 358	222 477	pF
C _{rss}	Reverse Transfer Capacitance		Q1 Q2	– –	22 35	31 49	pF
R _g	Gate Resistance		Q1 Q2	0.2 0.2	1.6 1.2	4.4 3.5	Ω

SWITCHING CHARACTERISTICS

t _{d(on)}	Turn-On Delay Time	Q1 V _{DD} = 15 V, I _D = 10.1 A, R _{GEN} = 6 Ω Q2 V _{DD} = 15 V, I _D = 12.4 A, R _{GEN} = 6 Ω	Q1 Q2	– –	5.2 6.6	10 14	ns
t _r	Rise Time		Q1 Q2	– –	1.2 1.8	10 10	ns
t _{d(off)}	Turn-Off Delay Time		Q1 Q2	– –	11.9 17.4	22 32	ns
t _f	Fall Time		Q1 Q2	– –	1.4 1.5	10 10	ns
Q _{g(TOT)}	Total Gate Charge	V _{GS} = 0 V to 10 V	Q1 Q2	– –	7.2 15.6	11 23	nC
Q _{g(TOT)}	Total Gate Charge	V _{GS} = 0 V to 5 V	Q1 Q2	– –	3.8 7.9	6 12	nC
Q _{gs}	Gate to Source Charge	Q1 V _{DD} = 15 V, I _D = 10.1 A	Q1 Q2	– –	1.6 3.2	– –	nC
Q _{gd}	Gate to Drain "Miller" Charge	Q2 V _{DD} = 15 V, I _D = 12.4 A	Q1 Q2	– –	1.1 1.6	– –	nC

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ELECTRICAL CHARACTERISTICS ($T_J = 25\text{ }^{\circ}\text{C}$ unless otherwise noted) (continued)

Symbol	Parameter	Test Condition	Type	Min.	Typ.	Max.	Unit
DRAIN-SOURCE DIODE CHARACTERISTICS							
V_{SD}	Source-Drain Diode Forward Voltage	$V_{GS} = 0\text{ V}$, $I_S = 10.1\text{ A}$ (Note 2) $V_{GS} = 0\text{ V}$, $I_S = 12.4\text{ A}$ (Note 2)	Q1 Q2	– –	0.90 0.83	1.2 1.2	V
t_{rr}	Reverse Recovery Time	Q1 $I_F = 10.1\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$	Q1 Q2	– –	16 18	28 32	ns
Q_{rr}	Reverse Recovery Charge	Q2 $I_F = 12.4\text{ A}$, $di/dt = 300\text{ A}/\mu\text{s}$	Q1 Q2	– –	4 13	10 23	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTES:

- $R_{\theta JA}$ is determined with the device mounted on a 1 in² pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



d 57 °C/W when mounted on
a 1 in² pad of 2 oz copper



d 50 °C/W when mounted on
a 1 in² pad of 2 oz copper



d 125 °C/W when mounted on
a minimum pad of 2 oz copper



d 120 °C/W when mounted on
a minimum pad of 2 oz copper

- Pulse Test: Pulse Width < 300 μs , Duty cycle < 2.0%.
- As an N-ch device, the negative Vgs rating is for low duty cycle pulse occurrence only. No continuous rating is implied.
- Q1: E_{AS} of 9 mJ is based on starting $T_J = 25\text{ }^{\circ}\text{C}$, $L = 0.3\text{ mH}$, $I_{AS} = 8\text{ A}$, $V_{DD} = 27\text{ V}$, $V_{GS} = 10\text{ V}$. 100% test at $L = 0.1\text{ mH}$, $I_{AS} = 12\text{ A}$.
- Q2: E_{AS} of 21 mJ is based on starting $T_J = 25\text{ }^{\circ}\text{C}$, $L = 0.3\text{ mH}$, $I_{AS} = 12\text{ A}$, $V_{DD} = 27\text{ V}$, $V_{GS} = 10\text{ V}$. 100% test at $L = 0.1\text{ mH}$, $I_{AS} = 18\text{ A}$.

TYPICAL CHARACTERISTICS (Q1-Channel) ($T_J = 25^\circ\text{C}$ unless otherwise noted)

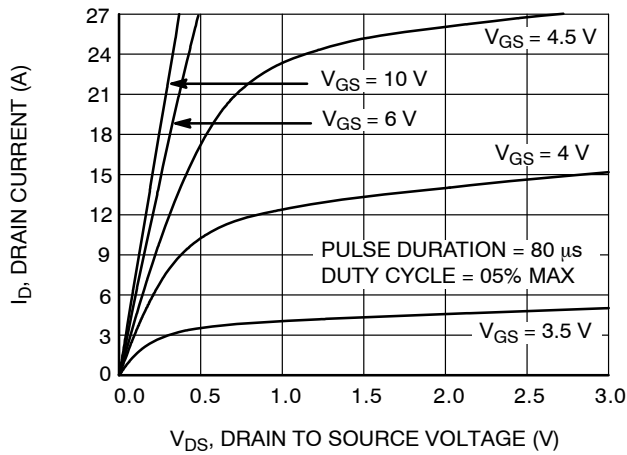


Figure 1. On Region Characteristics

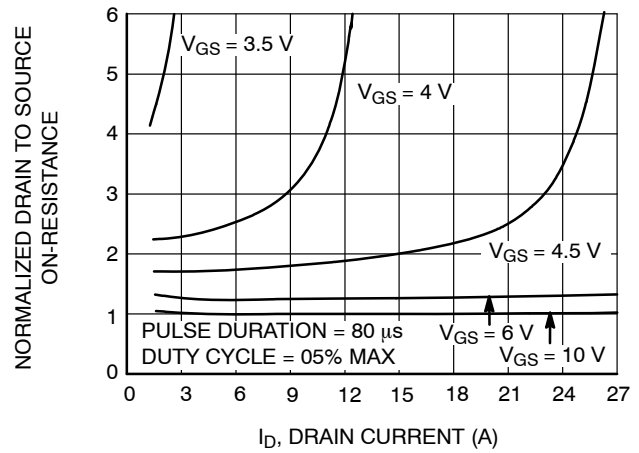


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

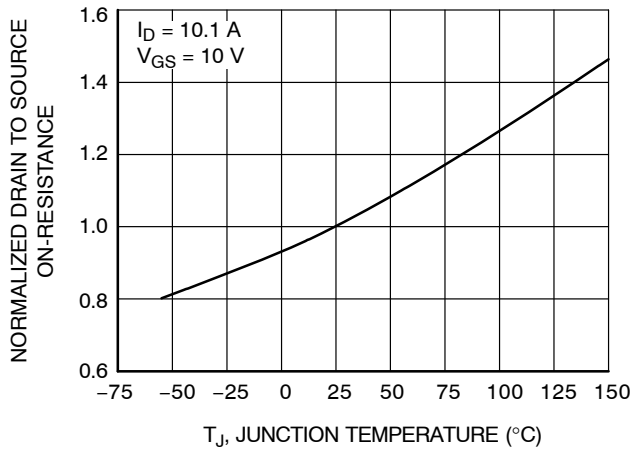


Figure 3. Normalized On Resistance vs. Junction Temperature

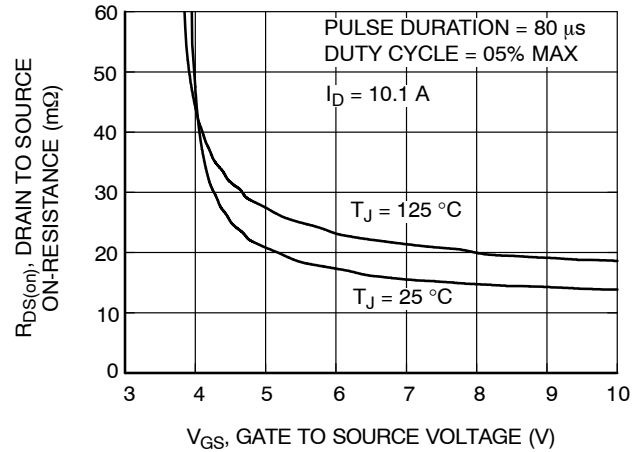


Figure 4. On-Resistance vs. Gate to Source Voltage

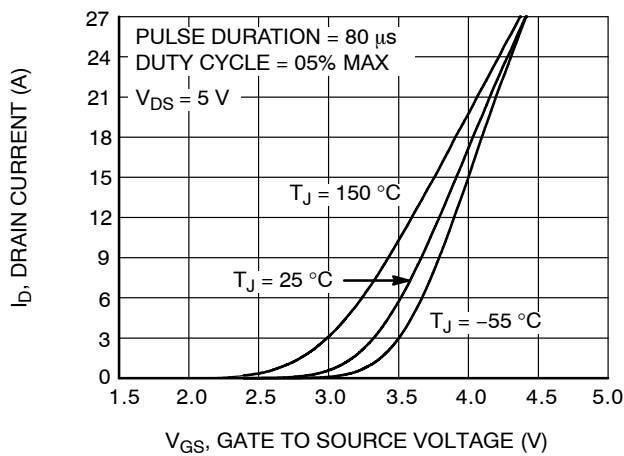


Figure 5. Transfer Characteristics

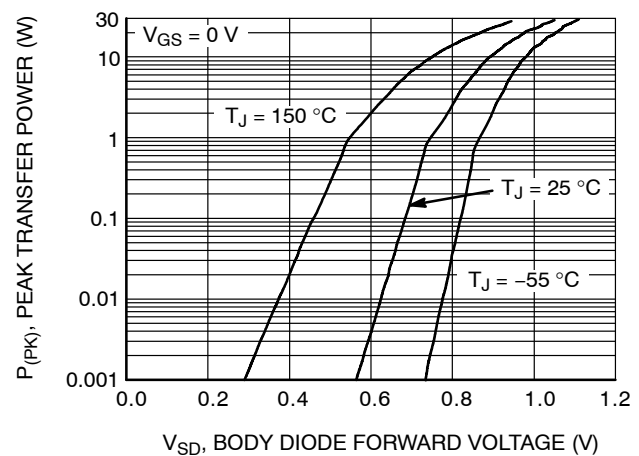


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

TYPICAL CHARACTERISTICS (Q1-Channel) ($T_J = 25^\circ\text{C}$ unless otherwise noted) (continued)

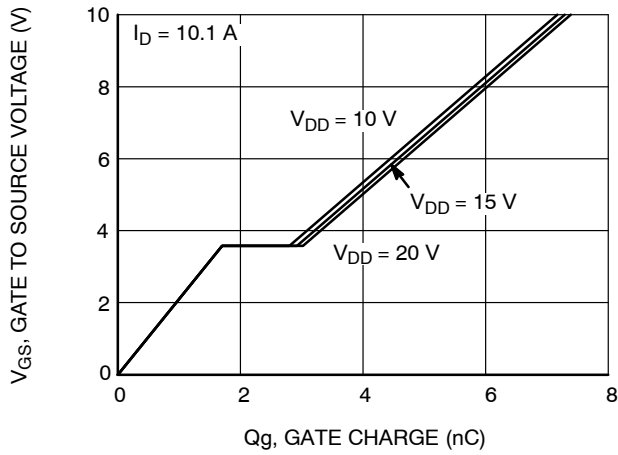


Figure 7. Gate Charge Characteristics

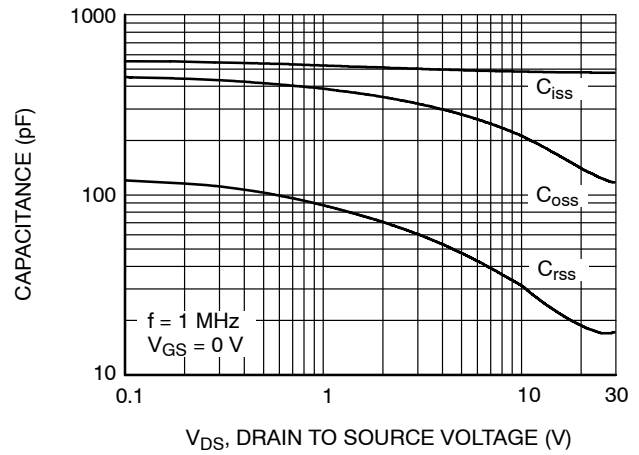


Figure 8. Capacitance vs. Drain to Source Voltage

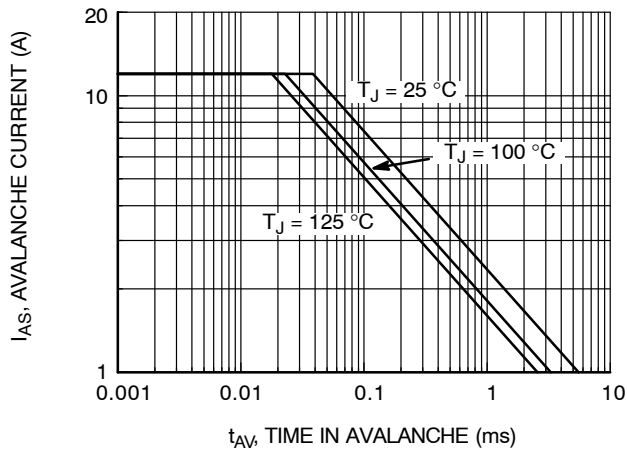


Figure 9. Unclamped Inductive Switching Capability

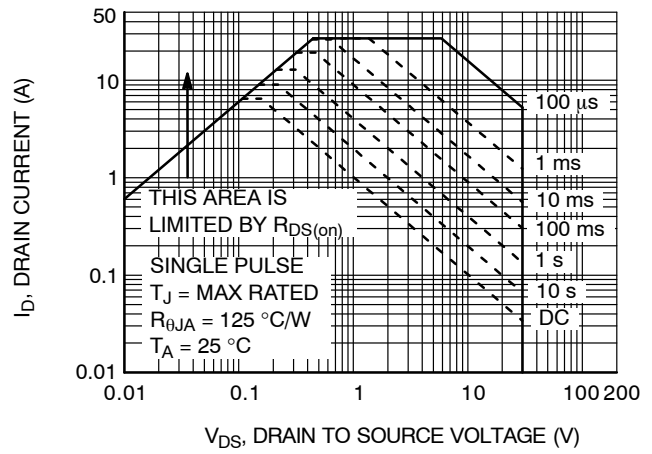


Figure 10. Forward Bias Safe Operating Area

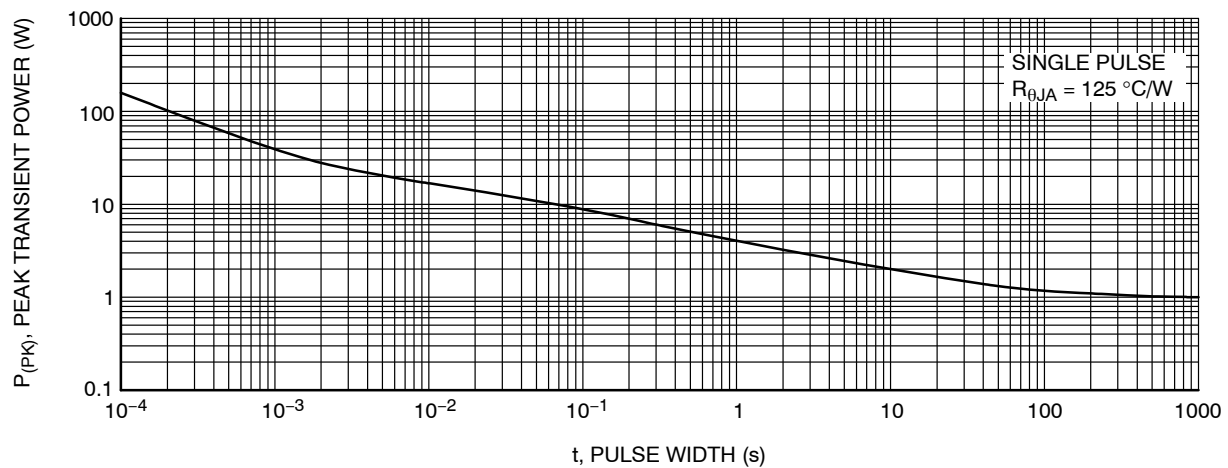


Figure 11. Single Pulse Maximum Power Dissipation

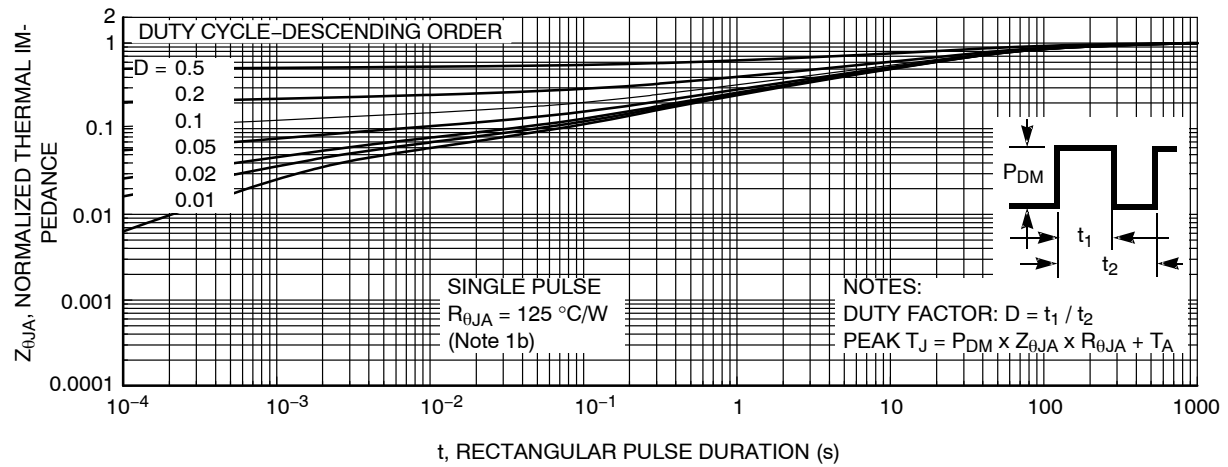
TYPICAL CHARACTERISTICS (Q1-Channel) ($T_J = 25\text{ }^{\circ}\text{C}$ unless otherwise noted) (continued)

Figure 12. Junction-to-Ambient Transient Thermal Response Curve

TYPICAL CHARACTERISTICS (Q2-Channel) ($T_J = 25^\circ\text{C}$ unless otherwise noted)

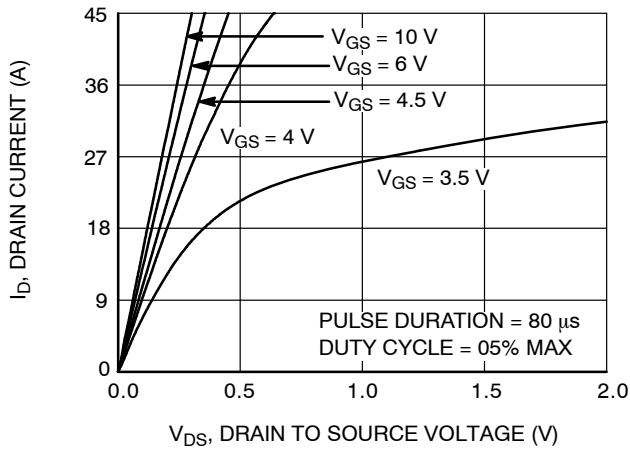


Figure 13. On Region Characteristics

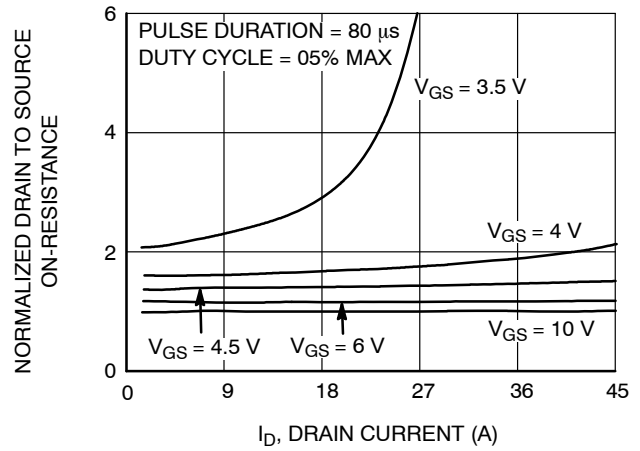


Figure 14. Normalized On-Resistance vs. Drain Current and Gate Voltage

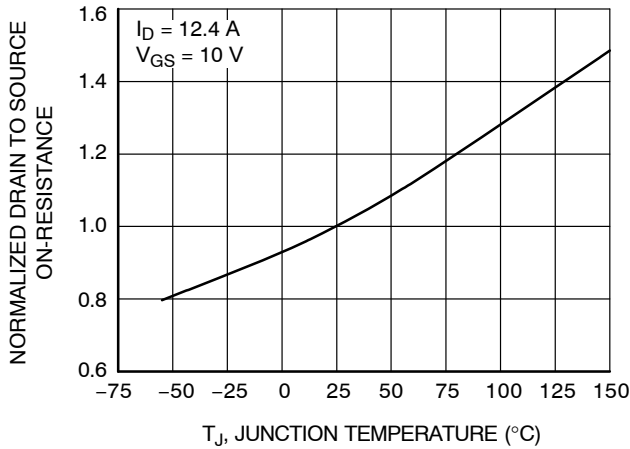


Figure 15. Normalized On-Resistance vs. Junction Temperature

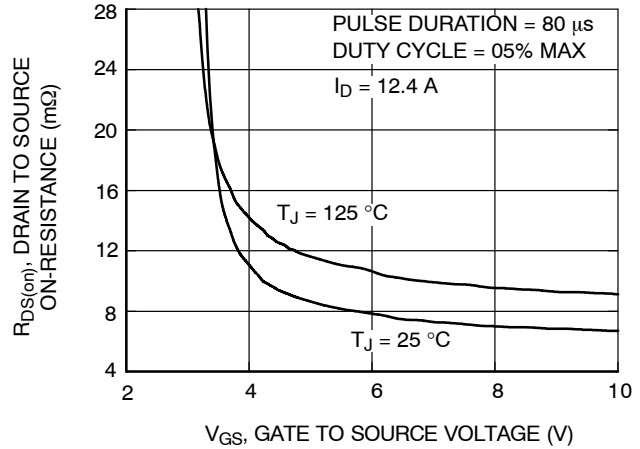


Figure 16. On-Resistance vs. Gate to Source Voltage

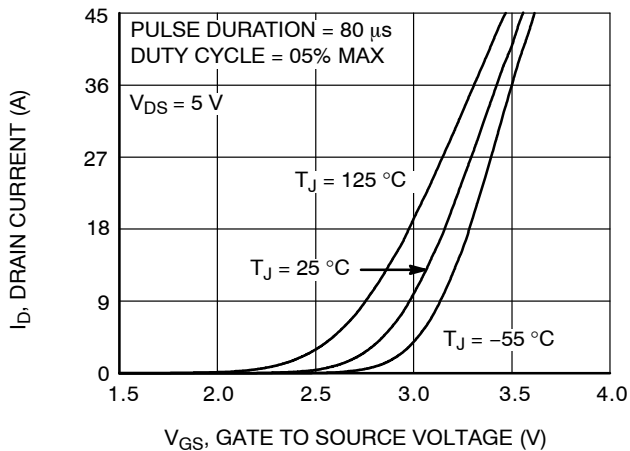


Figure 17. Transfer Characteristics

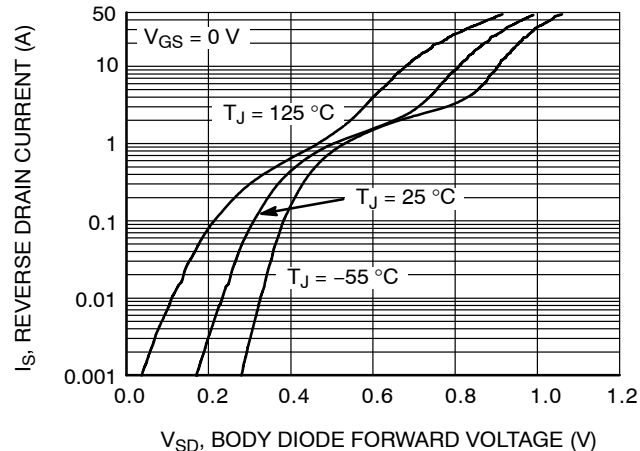


Figure 18. Source to Drain Diode Forward Voltage vs. Source Current

TYPICAL CHARACTERISTICS (Q2-Channel) ($T_J = 25^\circ\text{C}$ unless otherwise noted) (continued)

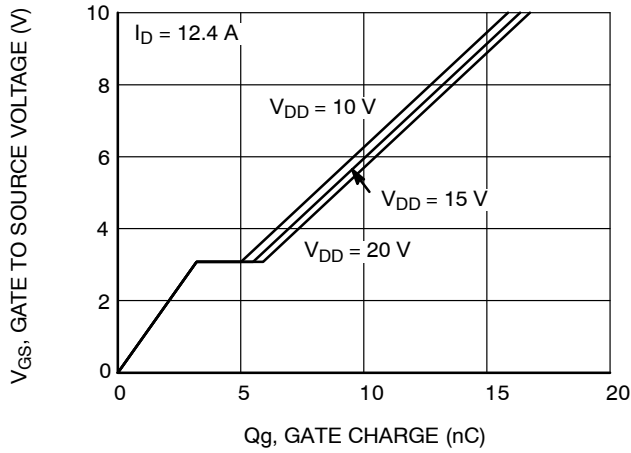


Figure 19. Gate Charge Characteristics

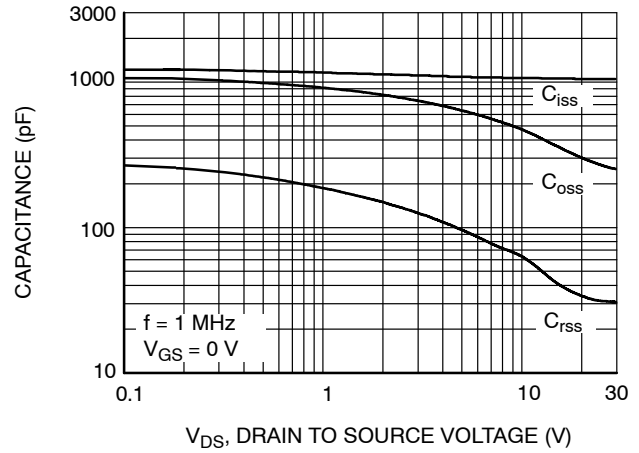


Figure 20. Capacitance vs. Drain to Source Voltage

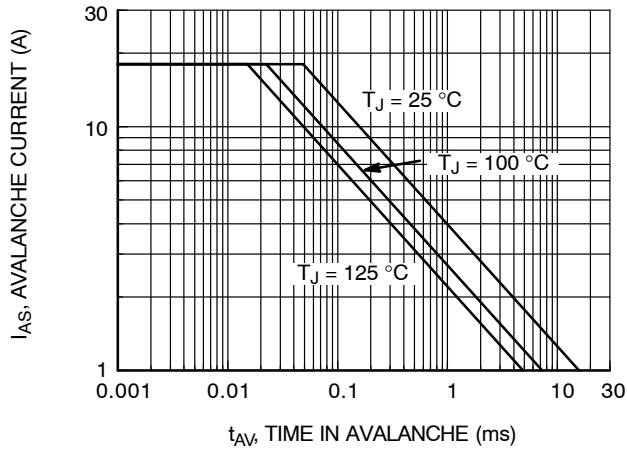


Figure 21. Unclamped Inductive Switching Capability

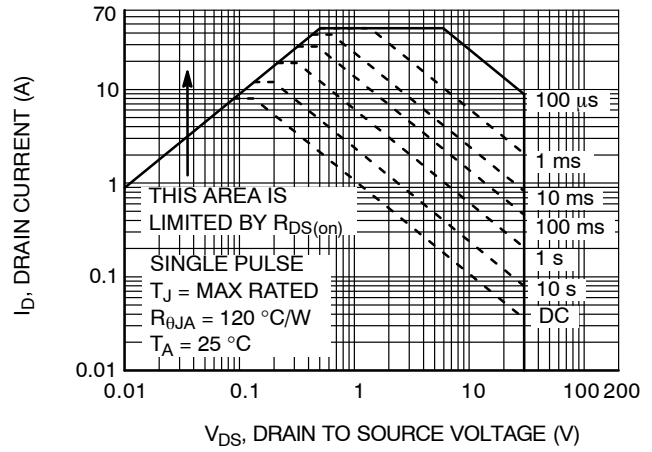


Figure 22. Forward Bias Safe Operating Area

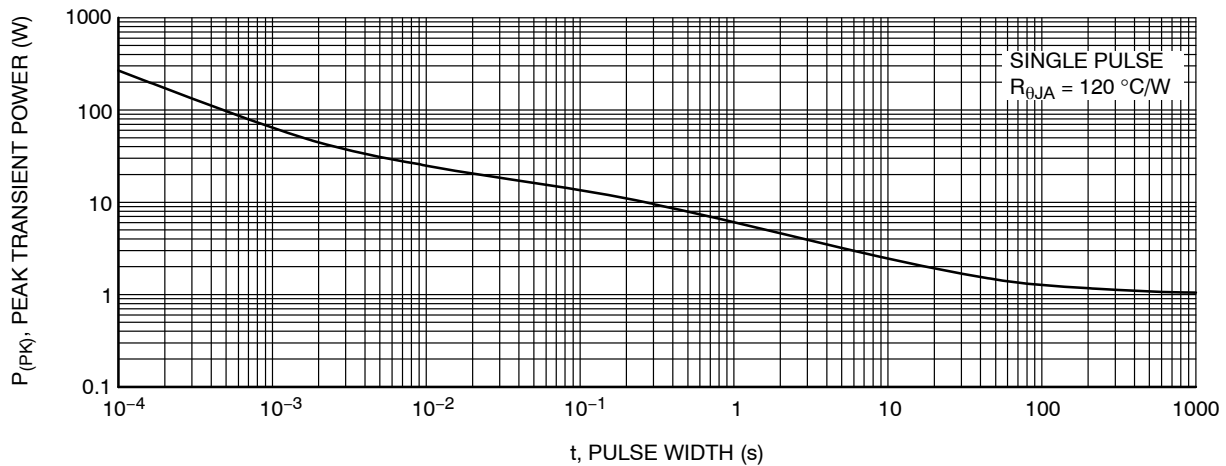


Figure 23. Single Pulse Maximum Power Dissipation

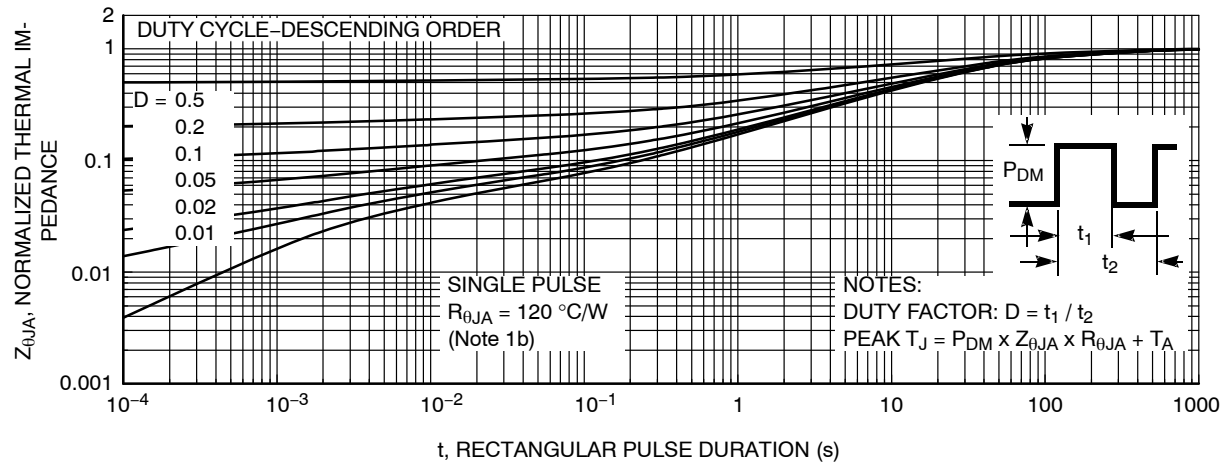
TYPICAL CHARACTERISTICS (Q2-Channel) ($T_J = 25\text{ }^{\circ}\text{C}$ unless otherwise noted) (continued)

Figure 24. Junction-to-Ambient Transient Thermal Response Curve

FDMS7620S

TYPICAL CHARACTERISTICS (continued)

SyncFET Schottky Body Diode Characteristics

onsemi's SyncFET™ process embeds a Schottky diode in parallel with PowerTrench™ MOSFET. This diode exhibits similar characteristics to a discrete external Schottky diode in parallel with a MOSFET. Figure 26 shows the reverse recovery characteristic of the FDMS7620S.

Schottky barrier diodes exhibit significant leakage at high temperature and high reverse voltage. This will increase the power in the device.

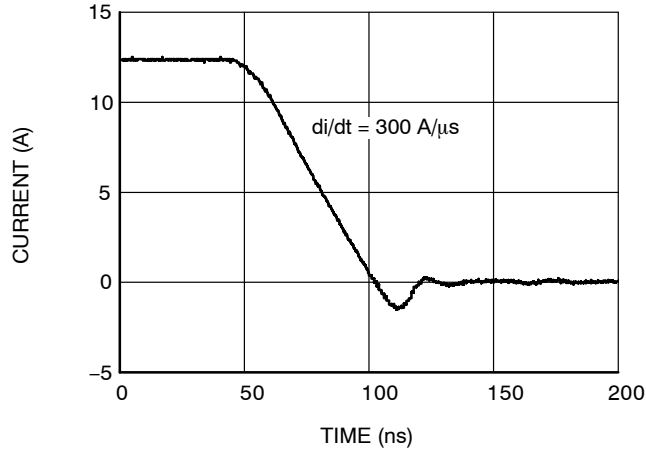


Figure 25. FDMS7620S SyncFET Body Diode Reverse Recovery Characteristic

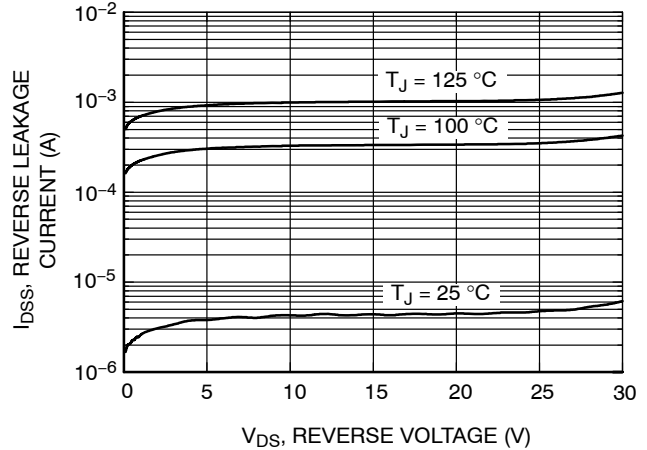


Figure 26. SyncFET Body Diode Reverse Leakage vs. Drain-Source Voltage

ORDERING INFORMATION

Device	Device Marking	Package	Reel Size	Tape Width	Shipping†
FDMS7620S	FDMS7620S	DFN8 5x6, 1.27P, Power 56 (Pb-Free)	13"	12 mm	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

FDMS7620S

REVISION HISTORY

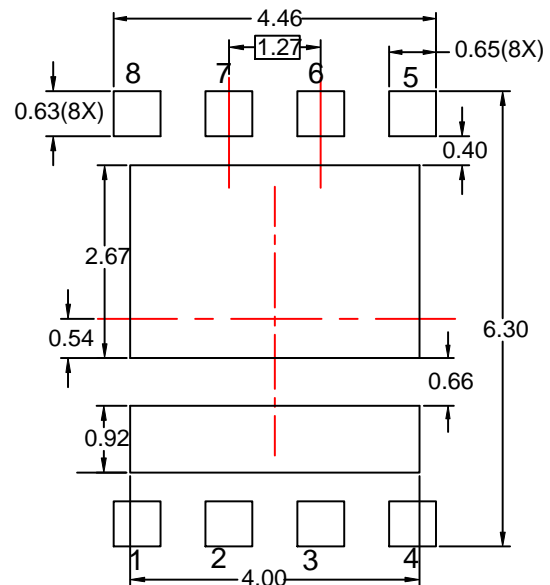
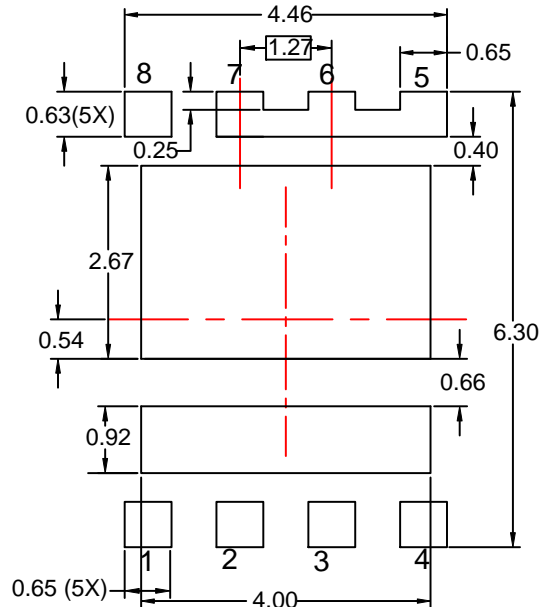
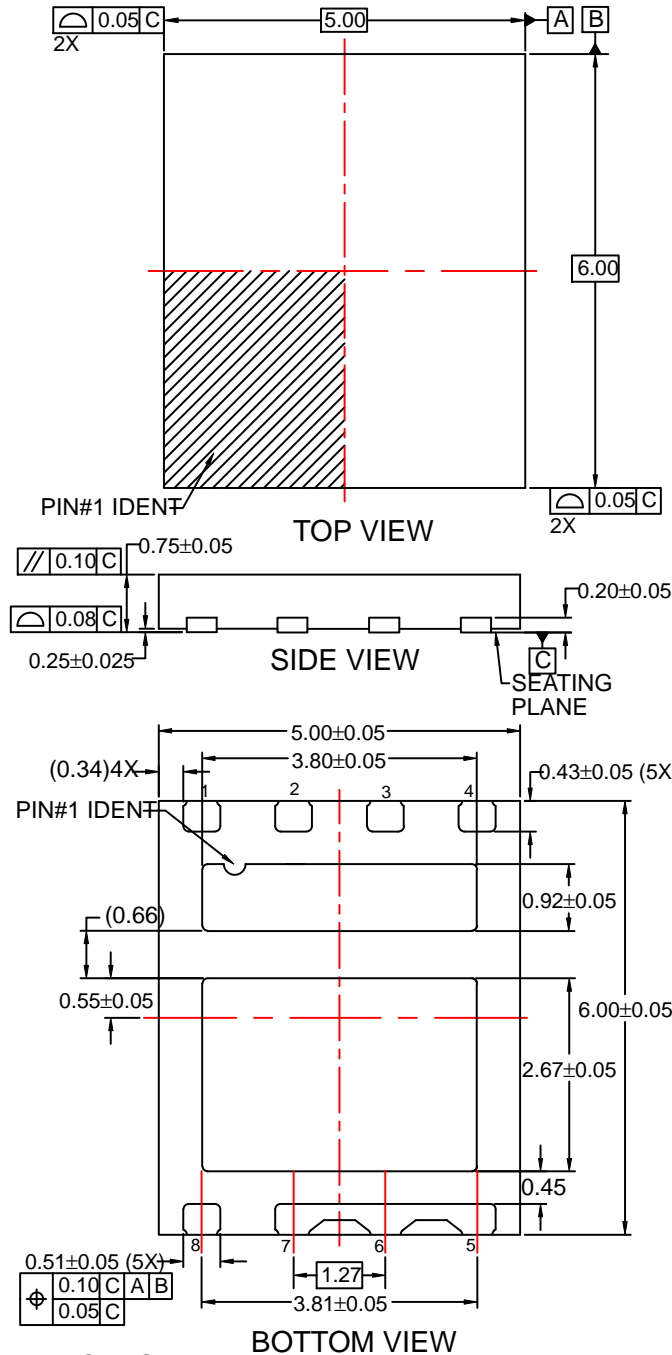
Revision	Description of Changes	Date
4	Data Sheet converted to onsemi format.	8/11/2025

This document has undergone updates prior to the inclusion of this revision history table. The changes tracked here only reflect updates made on the noted approval dates.

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DFN8 5x6, 1.27P
CASE 506DR
ISSUE O

DATE 31 JUL 2016



NOTES:

- A. PACKAGE DOES NOT FULLY CONFORM TO JEDEC STANDARD.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.

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