

FDMS7660AS

N-Channel PowerTrench® SyncFET™ 30 V, 42 A, 2.4 mΩ

Features

- Max $r_{DS(on)}$ = 2.4 mΩ at $V_{GS} = 10\text{ V}$, $I_D = 25\text{ A}$
- Max $r_{DS(on)}$ = 2.6 mΩ at $V_{GS} = 7\text{ V}$, $I_D = 23\text{ A}$
- Advanced Package and Silicon combination for low $r_{DS(on)}$ and high efficiency
- SyncFET Schottky Body Diode
- MSL1 robust package design
- 100% UIL tested
- RoHS Compliant

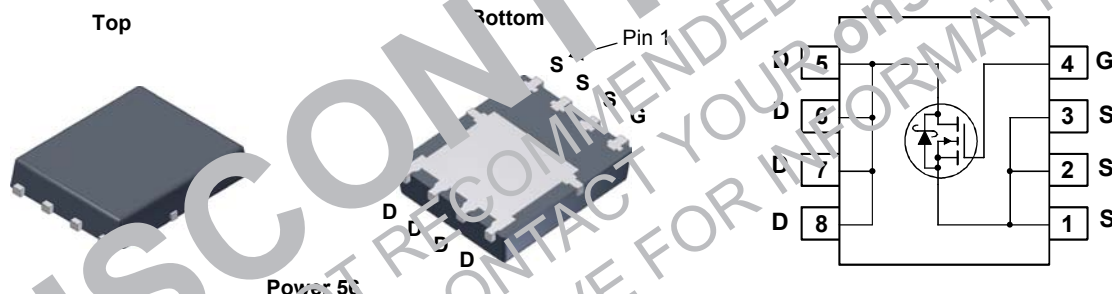


General Description

The FDMS7660AS has been designed to minimize losses in power conversion application. Advancements in both silicon and package technologies have been combined to offer the lowest $r_{DS(on)}$ while maintaining excellent switching performance. This device has the added benefit of an efficient monolithic Schottky body diode.

Applications

- Synchronous Rectifier for AC/DC Converters
- Notebook Voltage / GPU low side switch
- Networking Point-to-Point low side switch
- Telephony Secondary side rectification



MOSFET Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Ratings	Units
V_{DS}	Drain to Source Voltage	30	V
V_{GS}	Gate to Source Voltage (Note 4)	± 20	V
I_D	Drain Current -Continuous (Package limited) $T_C = 25^\circ\text{C}$	42	A
	-Continuous (Silicon limited) $T_C = 25^\circ\text{C}$	152	
	-Continuous $T_A = 25^\circ\text{C}$ (Note 1a)	26	
	-Pulsed	150	
dv/dt	MOSFET dv/dt	1.7	V/ns
E_{AS}	Single Pulse Avalanche Energy (Note 3)	128	mJ
P_D	Power Dissipation $T_C = 25^\circ\text{C}$	83	W
	Power Dissipation $T_A = 25^\circ\text{C}$ (Note 1a)	2.5	
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +150	$^\circ\text{C}$

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case	1.5	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	50	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMS7660AS	FDMS7660AS	Power 56	13"	12 mm	3000 units

Electrical Characteristics $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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Off Characteristics

BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 1\text{ mA}$, $V_{GS} = 0\text{ V}$	30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 10\text{ mA}$, referenced to 25°C		14		mV/ $^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 24\text{ V}$, $V_{GS} = 0\text{ V}$			500	μA
I_{GSS}	Gate to Source Leakage Current, Forward	$V_{GS} = 20\text{ V}$, $V_{DS} = 0\text{ V}$			100	nA

On Characteristics (Note 2)

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = 1\text{ mA}$	1.2	1.9	3.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 10\text{ mA}$, referenced to 25°C				mV/ $^\circ\text{C}$
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\text{ V}$, $I_D = 25\text{ A}$		1.9	2.4	m Ω
		$V_{GS} = 7\text{ V}$, $I_D = 23\text{ A}$		2.1	2.6	
		$V_{GS} = 4.5\text{ V}$, $I_D = 21\text{ A}$		2.5	3.0	
		$V_{GS} = 10\text{ V}$, $I_D = 25\text{ A}$, $T_J = 125^\circ\text{C}$		2.4	3.1	
g_{FS}	Forward Transconductance	$V_{DS} = 5\text{ V}$, $I_D = 25\text{ A}$		455		S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 15\text{ V}$, $V_{GS} = 0\text{ V}$, $f = 1\text{ MHz}$		4600	6120	pF
C_{oss}	Output Capacitance			1550	2065	pF
C_{rss}	Reverse Transfer Capacitance			125	190	pF
R_g	Gate Resistance			0.8	1.7	Ω

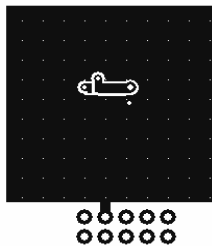
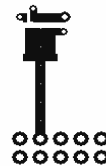
Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 15\text{ V}$, $I_D = 25\text{ A}$, $V_{GS} = 10\text{ V}$, $R_{GEN} = 6\text{ }\Omega$		19	34	ns
t_r	Rise Time			8	15	ns
$t_{d(off)}$	Turn-Off Delay Time			40	65	ns
t_f	Fall Time			5	10	ns
Q_g	Total Gate Charge			64	90	nC
Q_g	Total Gate Charge	$V_{GS} = 0\text{ V to }10\text{ V}$	$V_{DD} = 15\text{ V}$, $I_D = 25\text{ A}$	29	42	nC
Q_{gs}	Gate to Source Gate Charge	$V_{GS} = 0\text{ V to }4.5\text{ V}$		14.4		nC
Q_{gd}	Gate to Drain "Miller" Charge			5.9		nC

Source-Drain Diode Characteristics

V_{SD}	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{ V}$, $I_S = 2\text{ A}$ (Note 2)		0.41	0.7	V
		$V_{GS} = 0\text{ V}$, $I_S = 25\text{ A}$ (Note 2)		0.76	1.2	
t_{rr}	Reverse Recovery Time	$I_F = 25\text{ A}$, $di/dt = 300\text{ A}/\mu\text{s}$		39	62	ns
Q_{rr}	Reverse Recovery Charge			55	88	nC

Notes:

1. $R_{\theta JA}$ is determined with the device mounted on a 1 in² pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.a. 50°C/W when mounted on a
1 in² pad of 2 oz copper.b. 125°C/W when mounted on a
minimum pad of 2 oz copper.2. Pulse Test: Pulse Width < 300 μs , Duty cycle < 2.0%.3. E_{AS} of 128 mJ is based on starting $T_J = 25^\circ\text{C}$, $L = 1\text{ mH}$, $I_{AS} = 16\text{ A}$, $V_{DD} = 27\text{ V}$, $V_{GS} = 10\text{ V}$. 100% test at $L = 0.3\text{ mH}$, $I_{AS} = 25\text{ A}$.4. As an N-ch device, the negative V_{GS} rating is for low duty cycle pulse occurrence only. No continuous rating is implied.

Typical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

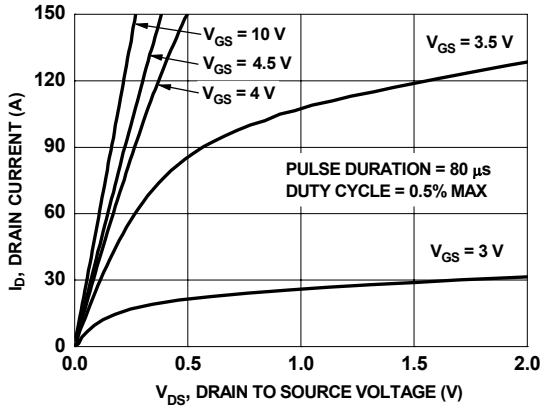


Figure 1. On-Region Characteristics

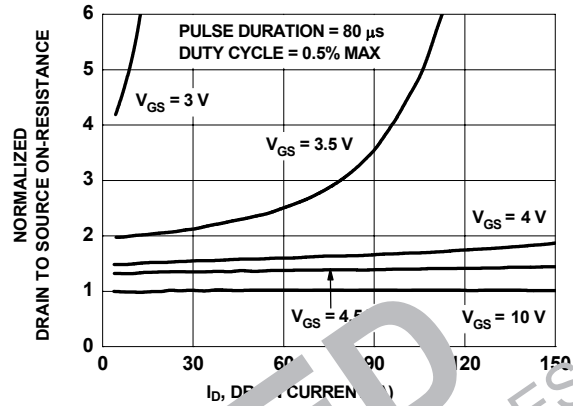


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

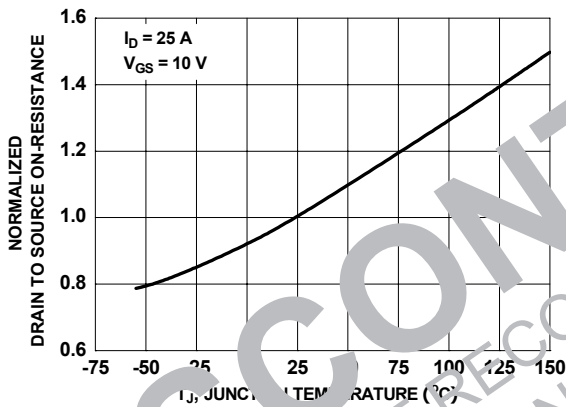


Figure 3. Normalized On-Resistance vs. Junction Temperature

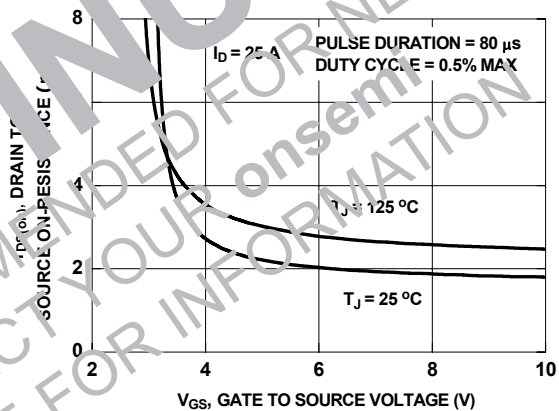


Figure 4. On-Resistance vs. Gate to Source Voltage

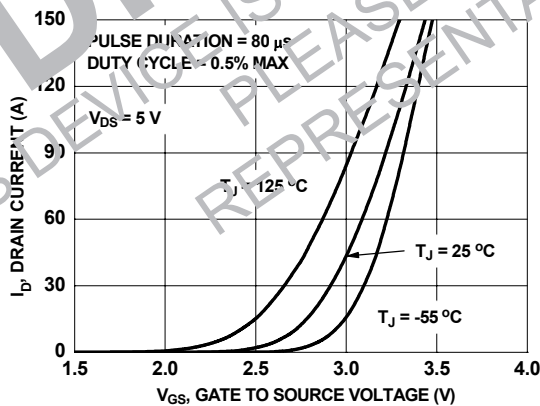


Figure 5. Transfer Characteristics

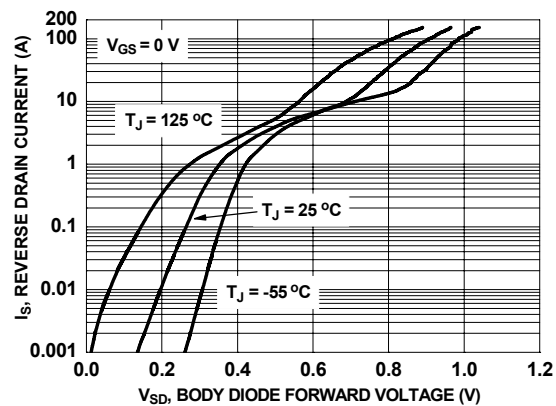


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

Typical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

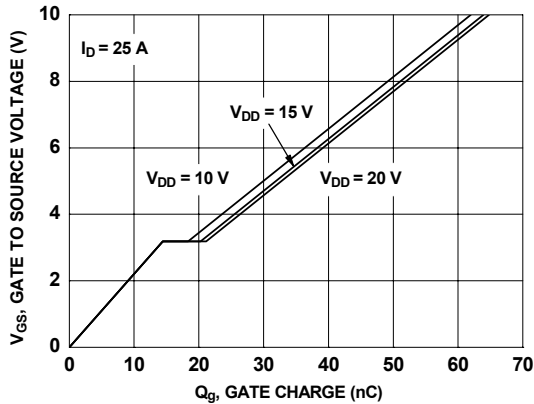


Figure 7. Gate Charge Characteristics

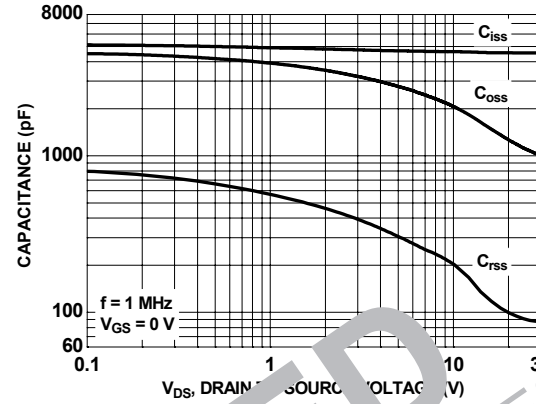


Figure 8. Capacitance vs Drain to Source Voltage

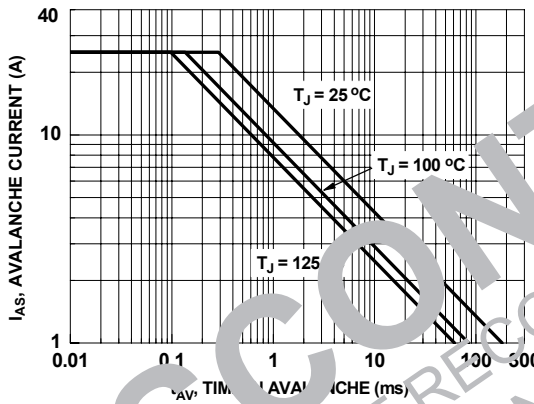


Figure 9. Unclamped Inductive Switching Capability

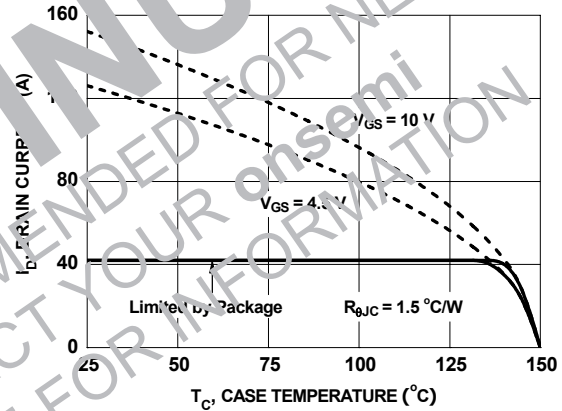


Figure 10. Maximum Continuous Drain Current vs Case Temperature

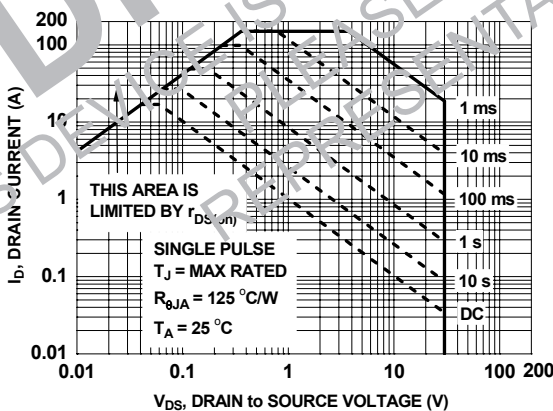


Figure 11. Forward Bias Safe Operating Area

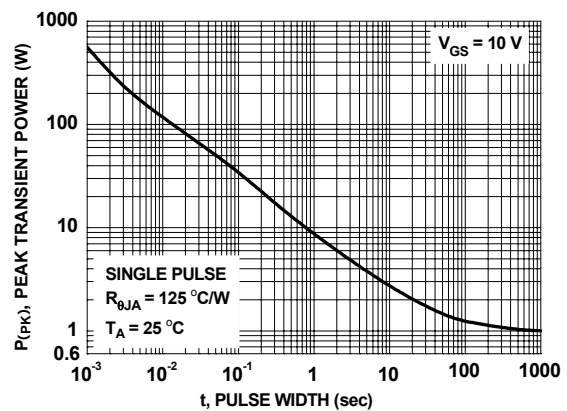
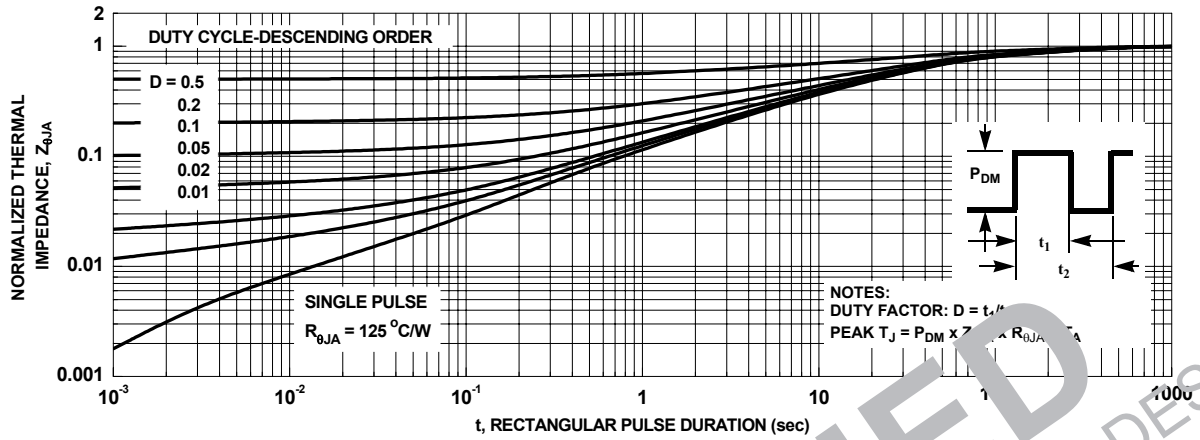


Figure 12. Single Pulse Maximum Power Dissipation

Typical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted



Typical Characteristics (continued)

SyncFET Schottky body diode Characteristics

Fairchild's SyncFET process embeds a Schottky diode in parallel with PowerTrench MOSFET. This diode exhibits similar characteristics to a discrete external Schottky diode in parallel with a MOSFET. Figure 14 shows the reverse recovery characteristic of the FDMS7660AS.

Schottky barrier diodes exhibit significant leakage at high temperature and high reverse voltage. This will increase the power in the device.

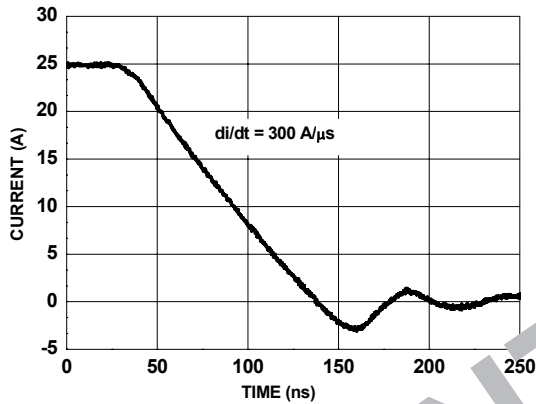


Figure 14. FDMS7660AS SyncFET Schottky body diode reverse recovery characteristic

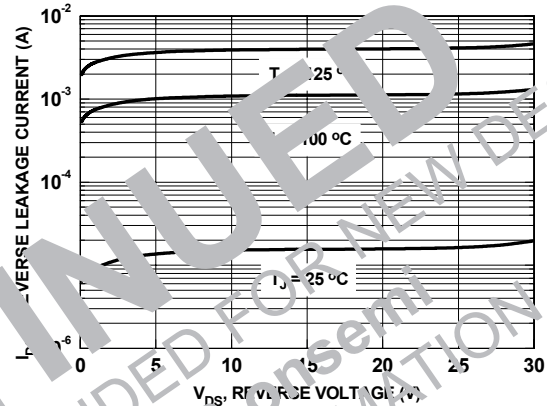


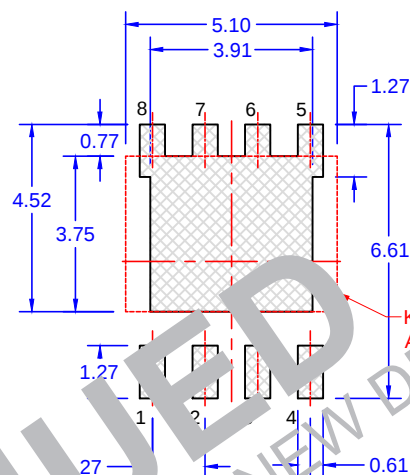
Figure 15. SyncFET body diode reverse leakage versus drain-source voltage

A mechanical drawing of a square package. The package is square with a central square area. Four pins are located at the corners of the package, labeled 1, 4, 5, and 8. Pin 1 is at the bottom-left corner, pin 4 is at the bottom-right corner, pin 5 is at the top-right corner, and pin 8 is at the top-left corner. The package has a central square area with a dashed red line indicating the center. The package is labeled 'PKG' with a center symbol (a circle with a cross) at the center. Dimensions are shown with blue arrows and labels: a horizontal dimension of 5.10 from the left edge to the center, a vertical dimension of 6.15 from the bottom edge to the center, and a vertical dimension of 6.15 from the center to the top edge. The package is labeled 'A' at the top-right corner and 'B' at the top-right corner.

SEE
DETAIL B

5.85

5.65



Technical drawing of a mechanical part with dimensions: 0.35, 0.15, 0.30, 0.05, and a 0°-12° angle.

[illegible]

- A. PACKAGE STANDARD REFERENCE: JEDEC MO-240, ISSUE A, VAR. AA,.
- B. DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.
- C. ALL DIMENSIONS ARE IN MILLIMETERS.
- D. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.
- E. IT IS RECOMMENDED TO HAVE NO TRACES OR VIAS WITHIN THE KEEP OUT AREA.

ON Semiconductor

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