

MOSFET – N-Channel, POWERTRENCH[®], DUAL COOL[®] 88

80 V, 164 A, 1.35 mΩ

FDMT1D3N08B

General Description

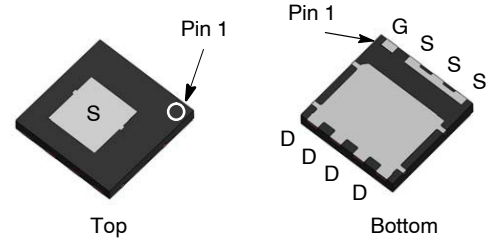
This N-Channel MOSFET is produced using onsemi's advanced POWERTRENCH process. Advancements in both silicon and DUAL COOL package technologies have been combined to offer the lowest $R_{DS(on)}$ while maintaining excellent switching performance by extremely low Junction-to-Ambient thermal resistance.

Features

- Max $R_{DS(on)}$ = 1.35 mΩ at $V_{GS} = 10\text{ V}$, $I_D = 36\text{ A}$
- Max $R_{DS(on)}$ = 1.8 mΩ at $V_{GS} = 8\text{ V}$, $I_D = 31\text{ A}$
- Advanced Package and Silicon Combination for Low $R_{DS(on)}$ and High Efficiency
- Next Generation Enhanced Body Diode Technology, Engineered for Soft Recovery
- Low Profile 8x8 mm MLP Package
- MSL1 Robust Package Design
- 100% UIL Tested
- RoHS Compliant

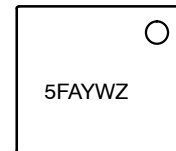
Applications

- OringFET / Load Switching
- Synchronous Rectification
- DC-DC Conversion

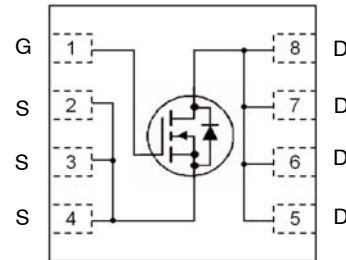


PQFN8 8X8, 2P
(DUAL COOL 88)
CASE 483AQ

MARKING DIAGRAM



5F	= Specific Device Code
A	= Assembly Plant Code
YW	= Date Code (Year & Week)
Z	= Lot Code



ORDERING INFORMATION

See detailed ordering, marking and shipping information on page 7 of this data sheet.

FDMT1D3N08B

MOSFET MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Rating	Unit
V_{DS}	Drain to Source Voltage	80	V
V_{GS}	Gate to Source Voltage	± 20	V
I_D	Drain Current – Continuous $T_C = 25^\circ\text{C}$ (Note 5)	164	A
	– Continuous $T_C = 100^\circ\text{C}$ (Note 5)	103	
	– Continuous $T_A = 25^\circ\text{C}$ (Note 1a)	36	
	– Pulsed (Note 4)	864	
E_{AS}	Single Pulse Avalanche Energy (Note 3)	1734	mJ
P_D	Power Dissipation $T_C = 25^\circ\text{C}$	178	W
	Power Dissipation $T_A = 25^\circ\text{C}$ (Note 1a)	3.3	
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +150	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

Symbol	Parameter	Ratings	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case (Top Source)	1.9	$^\circ\text{C}/\text{W}$
$R_{\theta JC}$	Thermal Resistance, Junction to Case (Bottom Drain)	0.7	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	38	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1b)	81	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1i)	15	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1j)	21	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1k)	9	

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
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OFF CHARACTERISTICS

BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 250 \mu\text{A}, V_{GS} = 0 \text{ V}$	80	–	–	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250 \mu\text{A}$, referenced to 25°C	–	50	–	$\text{mV}/^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 64 \text{ V}, V_{GS} = 0 \text{ V}$	–	–	1	μA
I_{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 20 \text{ V}, V_{DS} = 0 \text{ V}$	–	–	100	nA

ON CHARACTERISTICS

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250 \mu\text{A}$	2.0	3.2	4.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250 \mu\text{A}$, referenced to 25°C	–	-11	–	$\text{mV}/^\circ\text{C}$
$R_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10 \text{ V}, I_D = 36 \text{ A}$	–	1.1	1.35	m Ω
		$V_{GS} = 8 \text{ V}, I_D = 31 \text{ A}$	–	1.3	1.8	
		$V_{GS} = 10 \text{ V}, I_D = 36 \text{ A}, T_J = 125^\circ\text{C}$	–	1.8	2.2	
g_{FS}	Forward Transconductance	$V_{DS} = 5 \text{ V}, I_D = 36 \text{ A}$	–	116	–	S

FDMT1D3N08B

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted) (continued)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
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DYNAMIC CHARACTERISTICS

C _{iss}	Input Capacitance	V _{DS} = 40 V, V _{GS} = 0 V, f = 1 MHz	–	14000	19600	pF
C _{oss}	Output Capacitance		–	2050	2870	pF
C _{rss}	Reverse Transfer Capacitance		–	50	150	pF
R _g	Gate Resistance		0.1	1.4	2.1	Ω

SWITCHING CHARACTERISTICS

t _{d(on)}	Turn-On Delay Time	V _{DD} = 40 V, I _D = 36 A, V _{GS} = 10 V, R _{GEN} = 6 Ω	–	63	101	ns
t _r	Rise Time		–	56	90	ns
t _{d(off)}	Turn-Off Delay Time		–	68	109	ns
t _f	Fall Time		–	20	32	ns
Q _{g(TOT)}	Total Gate Charge	V _{GS} = 0 V to 10 V, V _{DD} = 40 V, I _D = 36 A	–	186	260	nC
		V _{GS} = 0 V to 8 V, V _{DD} = 40 V, I _D = 36 A	–	152	213	
Q _{gs}	Gate to Source Charge	V _{DD} = 40 V, I _D = 36 A	–	67	–	nC
Q _{gd}	Gate to Drain "Miller" Charge		–	37	–	nC
Q _{oss}	Output Charge	V _{DD} = 40 V, V _{GS} = 0 V	–	185	–	nC

DRAIN-SOURCE DIODE CHARACTERISTICS

V _{SD}	Source to Drain Diode Forward Voltage	V _{GS} = 0 V, I _S = 2.6 A (Note 2)	–	0.7	1.1	V
		V _{GS} = 0 V, I _S = 36 A (Note 2)	–	0.8	1.2	
t _{rr}	Reverse Recovery Time	I _F = 36 A, di/dt = 100 A/μs	–	83	132	ns
Q _{rr}	Reverse Recovery Charge		–	90	143	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

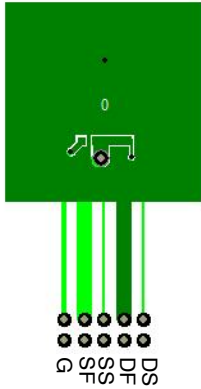
THERMAL CHARACTERISTICS

Symbol	Parameter	Ratings	Unit
R _{θJC}	Thermal Resistance, Junction to Case (Top Source)	1.9	°C/W
R _{θJC}	Thermal Resistance, Junction to Case (Bottom Drain)	0.7	
R _{θJA}	Thermal Resistance, Junction to Ambient (Note 1a)	38	
R _{θJA}	Thermal Resistance, Junction to Ambient (Note 1b)	81	
R _{θJA}	Thermal Resistance, Junction to Ambient (Note 1c)	26	
R _{θJA}	Thermal Resistance, Junction to Ambient (Note 1d)	34	
R _{θJA}	Thermal Resistance, Junction to Ambient (Note 1e)	14	
R _{θJA}	Thermal Resistance, Junction to Ambient (Note 1f)	16	
R _{θJA}	Thermal Resistance, Junction to Ambient (Note 1g)	26	
R _{θJA}	Thermal Resistance, Junction to Ambient (Note 1h)	60	
R _{θJA}	Thermal Resistance, Junction to Ambient (Note 1i)	15	
R _{θJA}	Thermal Resistance, Junction to Ambient (Note 1j)	21	
R _{θJA}	Thermal Resistance, Junction to Ambient (Note 1k)	9	
R _{θJA}	Thermal Resistance, Junction to Ambient (Note 1l)	11	

FDMT1D3N08B

NOTES:

1. $R_{\theta JA}$ is determined with the device mounted on a FR-4 board using a specified pad of 2 oz copper as shown below. $R_{\theta CA}$ is determined by the user's board design.



a) 38°C/W when mounted on a 1 in² pad of 2 oz copper.



b) 81°C/W when mounted on a minimum pad of 2 oz copper.

- c) Still air, 20.9 x 10.4 x 12.7 mm Aluminum Heat Sink, 1 in² pad of 2 oz copper
- d) Still air, 20.9 x 10.4 x 12.7 mm Aluminum Heat Sink, minimum pad of 2 oz copper
- e) Still air, 45.2 x 41.4 x 11.7 mm Aavid Thermalloy Part # 10-L41B-11 Heat Sink, 1 in² pad of 2 oz copper
- f) Still air, 45.2 x 41.4 x 11.7 mm Aavid Thermalloy Part # 10-L41B-11 Heat Sink, minimum pad of 2 oz copper
- g) 200FPM Airflow, No Heat Sink, 1 in² pad of 2 oz copper
- h) 200FPM Airflow, No Heat Sink, minimum pad of 2 oz copper
- i) 200FPM Airflow, 20.9 x 10.4 x 12.7 mm Aluminum Heat Sink, 1 in² pad of 2 oz copper
- j) 200FPM Airflow, 20.9 x 10.4 x 12.7 mm Aluminum Heat Sink, minimum pad of 2 oz copper
- k) 200FPM Airflow, 45.2 x 41.4 x 11.7 mm Aavid Thermalloy Part # 10-L41B-11 Heat Sink, 1 in² pad of 2 oz copper
- l) 200FPM Airflow, 45.2 x 41.4 x 11.7 mm Aavid Thermalloy Part # 10-L41B-11 Heat Sink, minimum pad of 2 oz copper

2. Pulse Test: Pulse Width < 300 μ s, Duty cycle < 2.0%.

3. E_{AS} of 1734 mJ is based on starting $T_J = 25^\circ\text{C}$; N-ch: $L = 3$ mH, $I_{AS} = 34$ A, $V_{DD} = 80$ V, $V_{GS} = 10$ V. 100% test at $L = 0.3$ mH, $I_{AS} = 77$ A.

4. Pulsed I_d please refer to Figure 11 SOA graph for more details.

5. Computed continuous current limited to Max Junction Temperature only, actual continuous current will be limited by thermal & electro-mechanical application board design.

FDMT1D3N08B

TYPICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

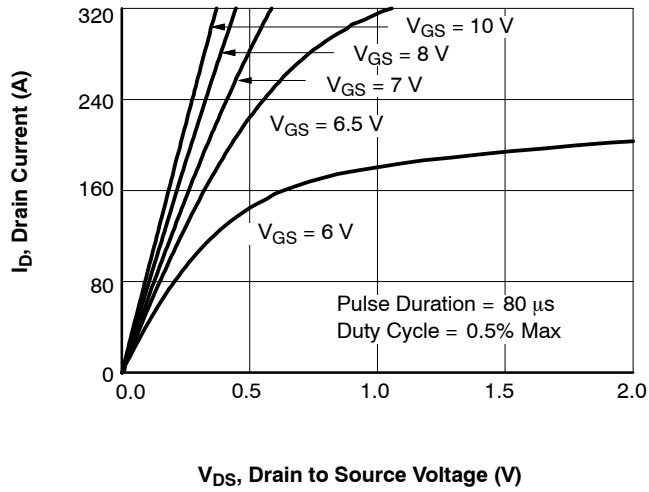


Figure 1. On-Region Characteristics

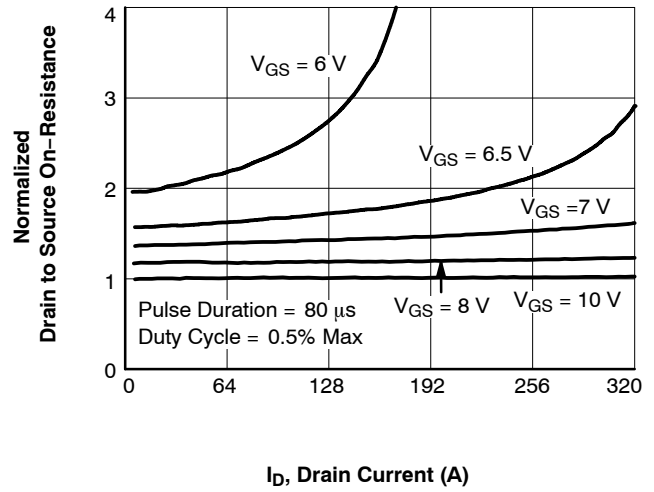


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

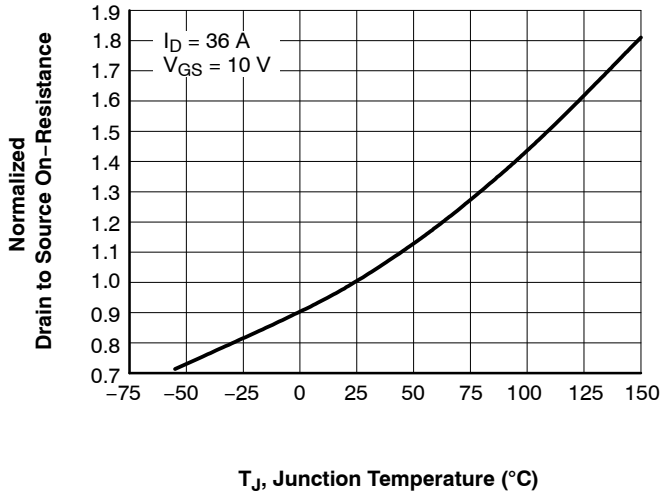


Figure 3. Normalized On-Resistance vs. Junction Temperature

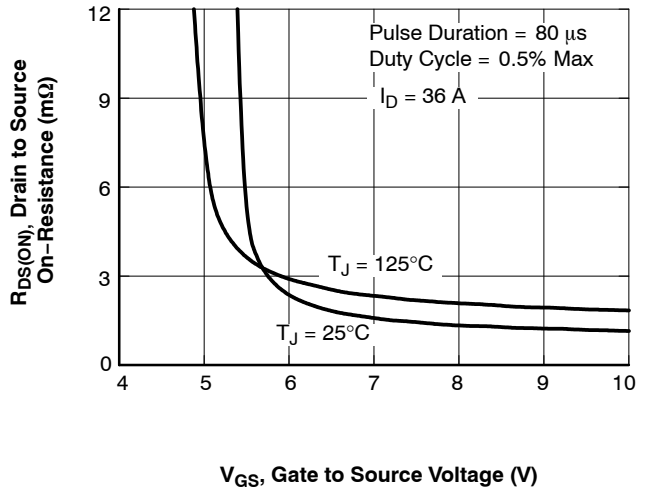


Figure 4. On-Resistance vs Gate-to-Source Voltage

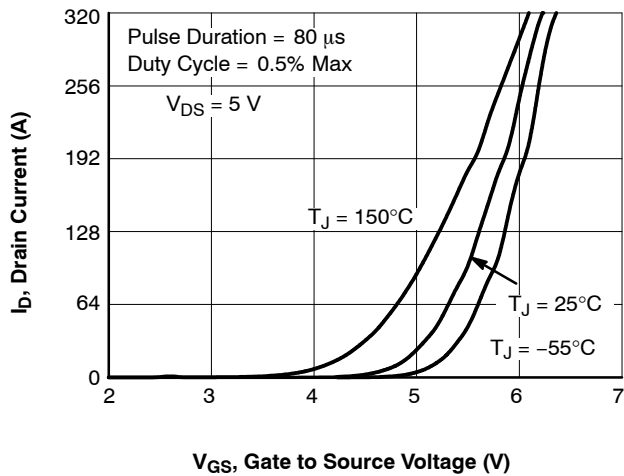


Figure 5. Transfer Characteristics

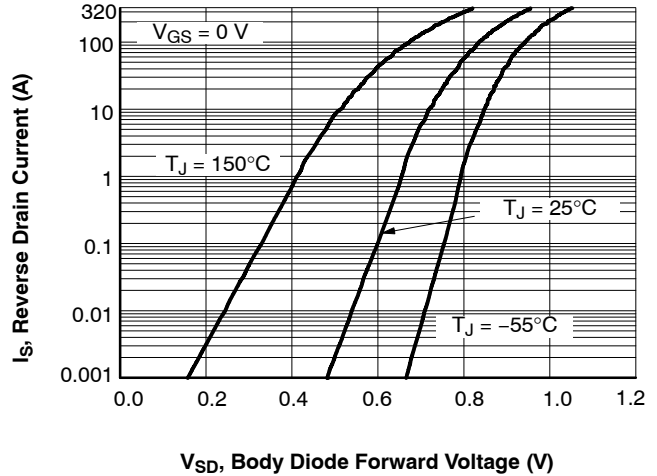


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

FDMT1D3N08B

TYPICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted)(continued)

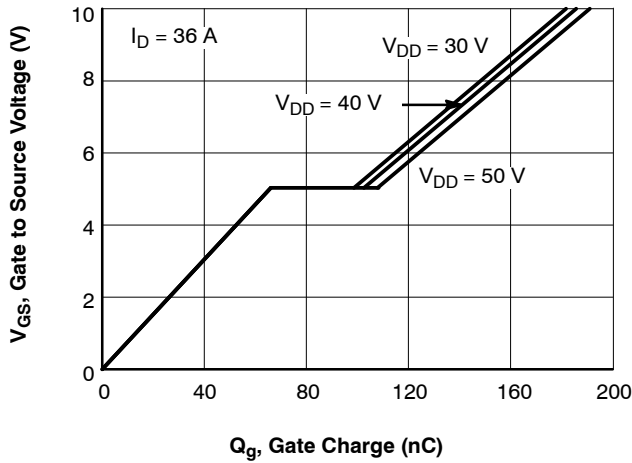


Figure 7. Gate Charge Characteristics

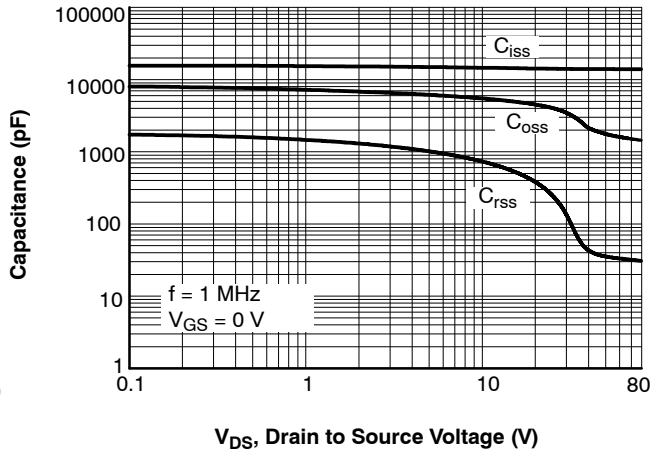


Figure 8. Capacitance vs Drain to Source Voltage

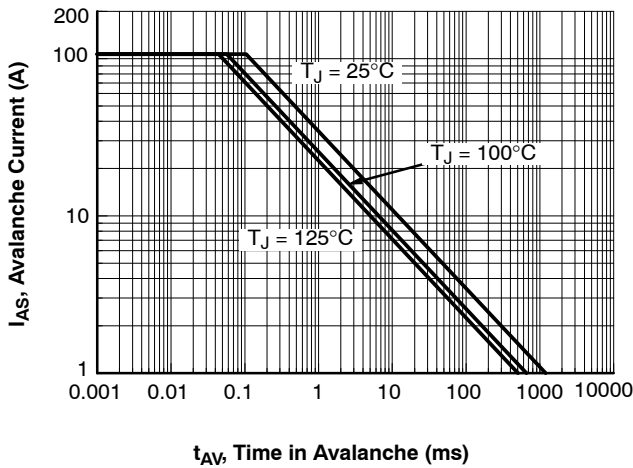


Figure 9. Unclamped Inductive Switching Capability

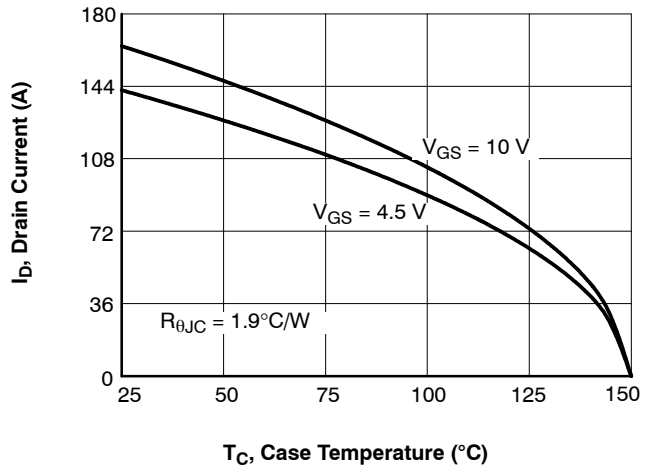


Figure 10. Maximum Continuous Drain Current vs. Case Temperature

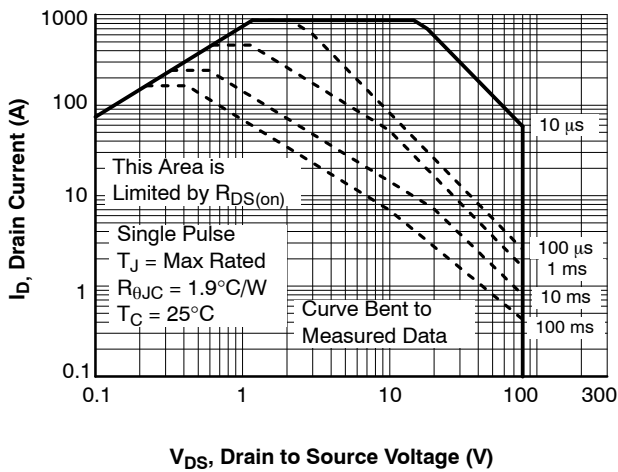


Figure 11. Forward Bias Safe Operating Area

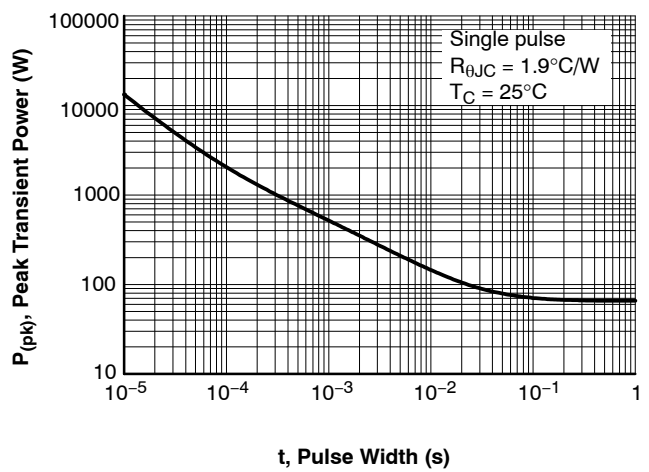


Figure 12. Single Pulse Maximum Power Dissipation

FDMT1D3N08B

TYPICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted)(continued)

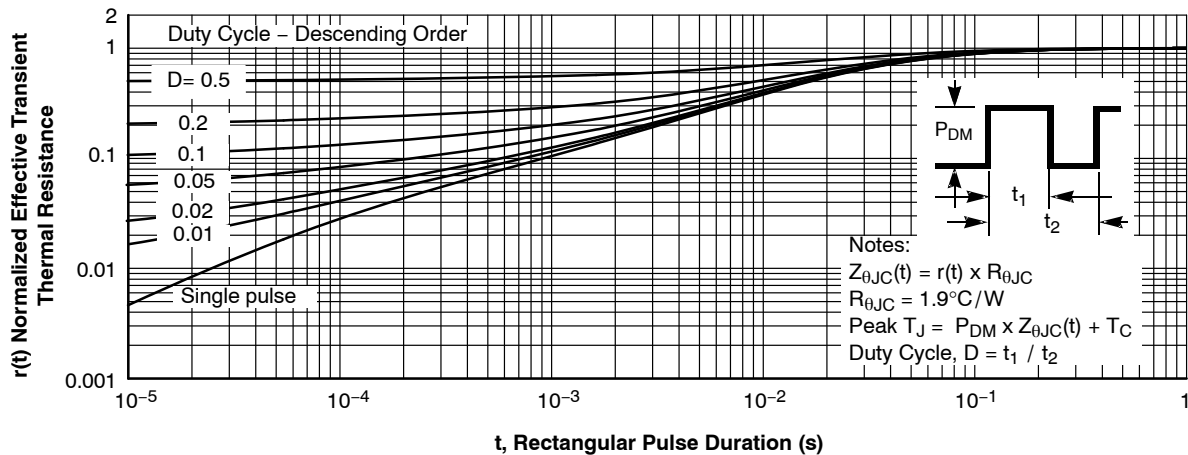


Figure 13. Junction-to-Case Transient Thermal Response Curve

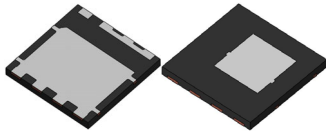
ORDERING INFORMATION

Device	Device Marking	Package	Reel Size	Tape Width	Shipping [†]
FDMT1D3N08B	5F	PQFN8 8X8, 2P, (DUAL COOL 88)	13"	13.3 mm	3000 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

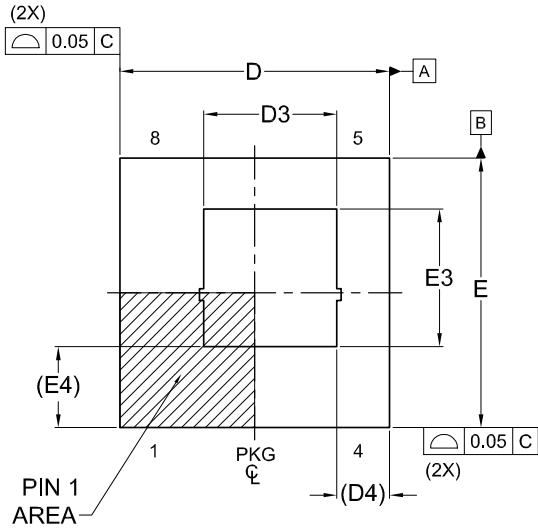
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MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

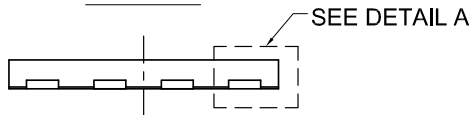


PQFN8 8X8, 2P
CASE 483AQ
ISSUE B

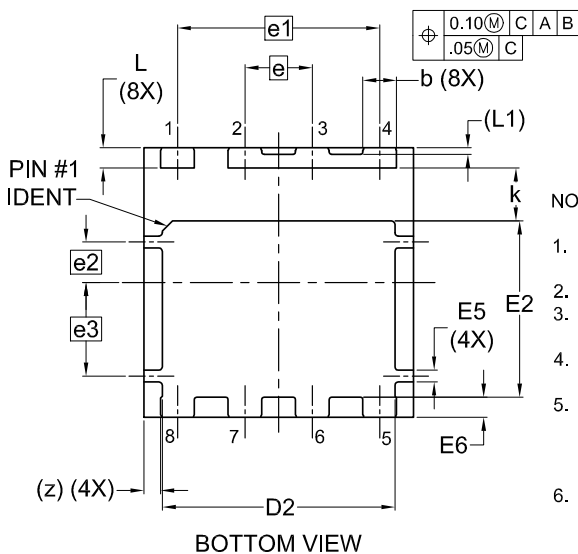
DATE 24 OCT 2022



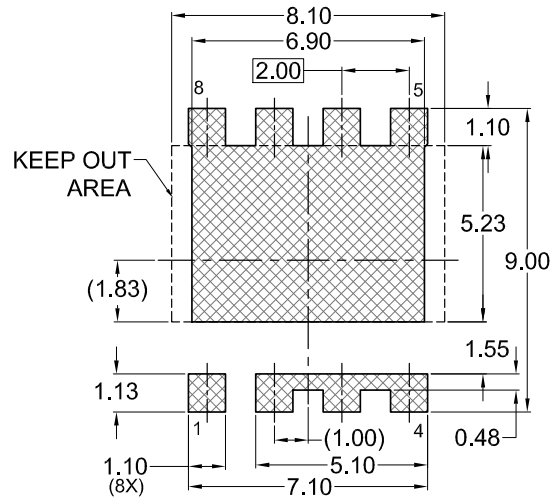
TOP VIEW



FRONT VIEW

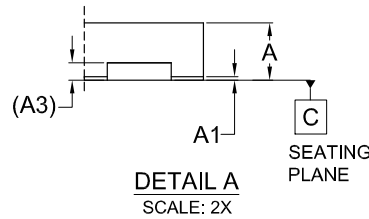


BOTTOM VIEW



LAND PATTERN RECOMMENDATION

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.



DETAIL A
SCALE: 2X

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.
4. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
5. SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.
6. IT IS RECOMMENDED TO HAVE NO TRACES OR VIAS WITHIN THE KEEP OUT AREA.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.75	0.85	0.95
A1	0.00	-	0.05
A3	0.25 REF		
b	0.90	1.00	1.10
D	7.90	8.00	8.10
D2	6.80	6.90	7.00
D3	3.68	3.86	4.03
D4	1.56 REF		
E	7.90	8.00	8.10
E2	5.13	5.23	5.33
E3	3.99	4.09	4.19
E4	2.41 REF		
E5	0.35 REF		
E6	0.60 REF		
e	2.00 BSC		
e1	6.00 BSC		
e2	1.20 BSC		
e3	2.78 BSC		
k	1.48	1.58	1.68
L	0.50	0.60	0.70
L1	0.20 REF		
z	0.50 REF		

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