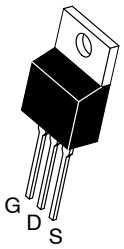
MOSFET – N 沟道, POWERTRENCH®

150 V, 130 A, 7.5 mΩ

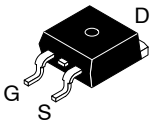
FDP075N15A, FDB075N15A

V_{DSS}	$R_{DS(ON)}$ MAX	I_D MAX
150 V	7.5 mΩ @ 10 V	130 A

*封装限制电流为 120 A。



TO−220
CASE 221A−09



D²PAK−3 (TO−263, 3−LEAD)
CASE 418AJ

说明

此 N 沟道 MOSFET 采用 **onsemi** 先进 POWERTRENCH 工艺生产，这一先进工艺是专为最大限度地降低导通电阻并保持卓越开关性能而定制的。

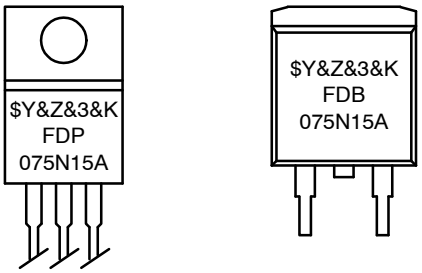
特性

- $R_{DS(on)}$ = 6.25 mΩ (典型值) @ V_{GS} = 10 V, I_D = 100 A
- 快速开关
- 低栅极电荷
- 高性能沟道技术可实现极低的 $R_{DS(on)}$
- 高功率和高电流处理能力
- 符合 RoHS 标准

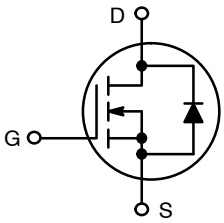
应用

- 用于 ATX / 服务器 / 电信 PSU 的同步整流
- 电池保护电路
- 电机驱动和不间断电源
- 微型太阳能逆变器

MARKING DIAGRAM



$Y	= **onsemi** logo
FDP075N15A FDB075N15A	= Device Code
&Z	= Assembly Plant Code
&3	= 3−Digit Date Code Format
&K	= 2−Digits Lot Run Traceability Code



N−Channel

ORDERING INFORMATION

See detailed ordering and shipping information on page 9 of this data sheet.

MOSFET 最大额定值 (T_C = 25°C 除非另有说明。)

符号	参数		FDP075N15A−F102 FDB075N15A	单位
V_{DSS}	漏极－源极电压		150	V
V_{GSS}	栅极－源极电压		±20	V
I_D	漏极电流	− 连续 (T_C = 25°C)	130*	A
		− 连续 (T_C = 100°C)	92	
I_{DM}	漏极电流	− 脉冲 (说明 1)	522	A
E_{AS}	单脉冲雪崩能量 (说明 2)		588	mJ
dv/dt	二极管恢复 dv/dt 峰值 (说明 3)		6.0	V/ns
P_D	功耗	(T_C = 25°C)	333	W
		− 降低至 25°C 以上	2.22	W/°C
T_J, T_{STG}	工作和存储温度范围		−55 至 +175	°C
T_L	用于焊接的最大引线温度，距离外壳 1/8”，持续 5 秒		300	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
(参考译文)
如果电压超过最大额定值表中列出的值范围，器件可能会损坏。如果超过任何这些限值，将无法保证器件功能，可能会导致器件损坏，影响可靠性。
*封装限制电流为 120 A。
1. 重复额定值：脉冲宽度受限于最大结温。
2. 开始 T_J = 25°C， L = 3 mH， I_{AS} = 19.8 A。
3. $I_{SD} \le$ 100 A, di/dt ≤ 200 A/μs, $V_{DD} \le BV_{DSS}$, 开始 T_J = 25°C.

热性能

符号	参数	FDP075N15A−F102 FDB075N15A	单位
$R_{\theta JC}$	结至外壳热阻最大值	0.45	°C/W
$R_{\theta JA}$	结至环境热阻 (最小尺寸的 2 盎司焊盘) 最大值。	62.5	
	结至环境热阻 D2−PAK (1 in^2 2 盎司焊盘) 最大值。	40	

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

符号	参数	测试条件	最小值	典型值	最大值	单位
关断特性						
BV_{DSS}	漏极－源极击穿电压	I_D = 250 μA, V_{GS} = 0 V	150	–	–	V
ΔBV_{DSS} / ΔT_J	击穿电压温度系数	I_D = 250 μA, 温度参考 25°C	–	0.1	–	V/°C
I_{DSS}	零栅极电压漏极电流	V_{DS} = 120 V, V_{GS} = 0 V	–	–	1	μA
		V_{DS} = 120 V, T_C = 150°C	–	–	500	
I_{GSS}	栅极−体漏电流	V_{GS} = ±20 V, V_{DS} = 0 V	–	–	±100	nA
导通特性						
$V_{GS(th)}$	栅极阈值电压	V_{GS} = V_{DS}, I_D = 250 μA	2.0	–	4.0	V
$R_{DS(on)}$	漏极至源极静态导通电阻	V_{GS} = 10 V, I_D = 100 A	–	6.25	7.5	mΩ
g_{FS}	正向跨导	V_{DS} = 10 V, I_D = 100 A	–	164	–	S
动态特性						
C_{iss}	输入电容	V_{DS} = 75 V, V_{GS} = 0 V, f = 1 MHz	–	5525	7350	pF
C_{oss}	输出电容		–	516	685	pF
C_{rss}	反向传输电容		–	21	–	pF
$C_{oss(er)}$	能量相关输出电容	V_{DS} = 75 V, V_{GS} = 0 V	–	909	–	pF
$Q_{g(tot)}$	10 V 的栅极电荷总量	V_{DS} = 75 V, I_D = 100 A, V_{GS} = 10 V (说明 4)	–	77	100	nC
Q_{gs}	栅极 − 源极栅极电荷		–	26	–	nC
Q_{gs2}	栅极平台电荷阈值		–	11	–	nC
Q_{gd}	栅极 − 漏极 “米勒” 电荷		–	16	–	nC
ESR	等效串联电阻 (G−S)	f = 1 MHz	–	2.29	–	Ω
开关特性						
$t_{d(on)}$	导通延迟时间	V_{DD} = 75 V, I_D = 100 A, V_{GS} = 10 V, R_G = 4.7 Ω (说明 4)	–	28	66	ns
t_r	开通上升时间		–	37	84	ns
$t_{d(off)}$	关断延迟时间		–	62	134	ns
t_f	关断下降时间		–	21	52	ns
漏极 − 源极二极管特性						
I_S	漏极 − 源极二极管最大正向连续电流		–	–	130*	A
I_{SM}	漏极 − 源极二极管最大正向脉冲电流		–	–	520	A
V_{SD}	漏极 − 源极二极管正向电压	V_{GS} = 0 V, I_{SD} = 100 A	–	–	1.25	V
t_{rr}	反向恢复时间	V_{GS} = 0 V, V_{DD} = 75 V, I_{SD} = 100 A, dI_F/dt = 100 A/μs	–	97	–	ns
Q_{rr}	反向恢复电荷		–	264	–	nC

4. 本质上独立于工作温度的典型特性。

典型性能特征

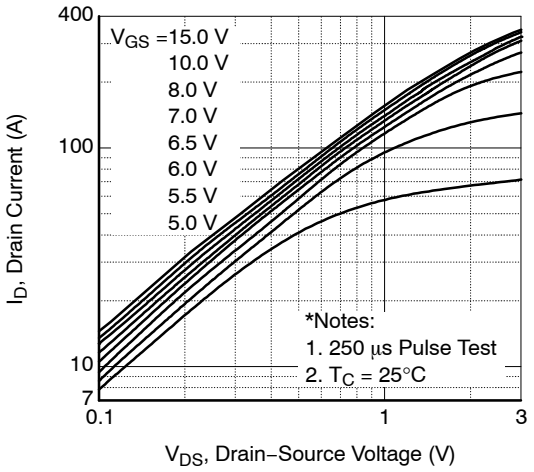


图 1. 导通区域特性

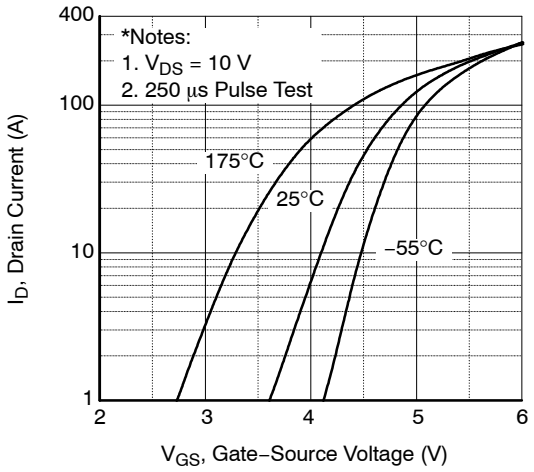


图 2. 传输特性

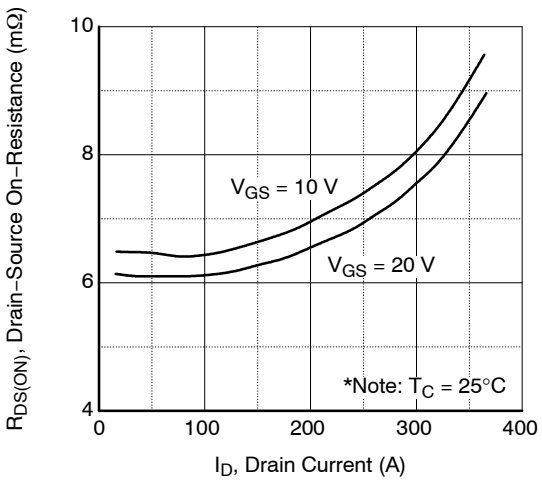


图 3. 导通电阻变化与漏极电流和栅极电压

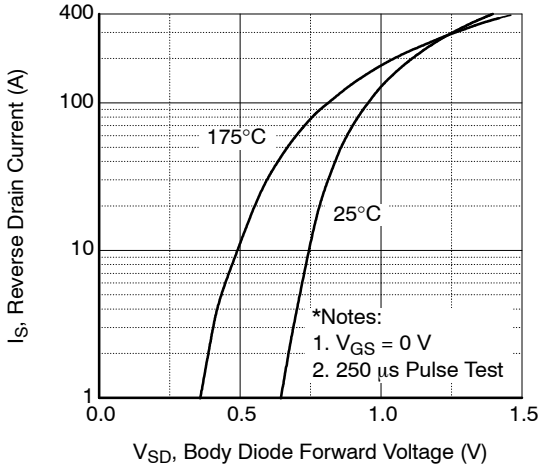


图 4. 体二极管正向电压变化与源极电流和温度

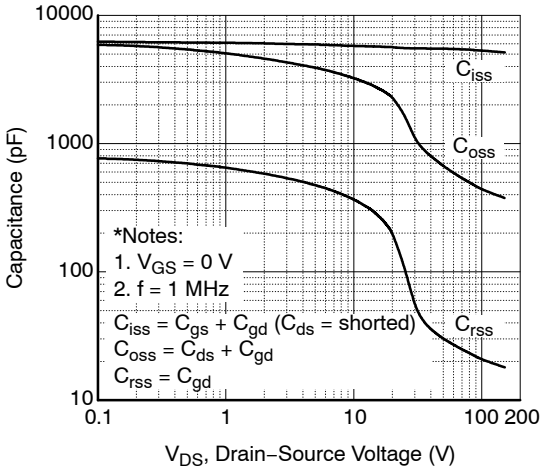


图 5. 电容特性

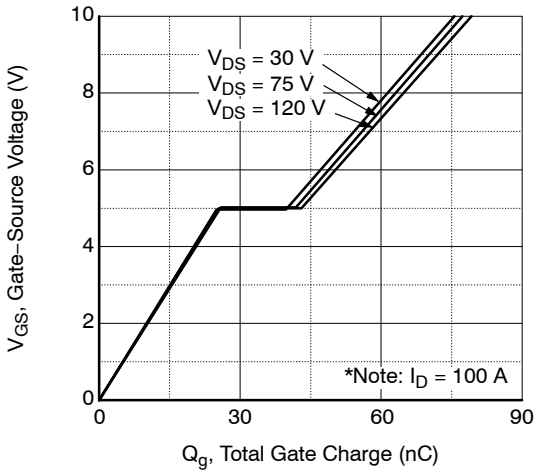


图 6. 栅极电荷

典型性能特征 (接上页)

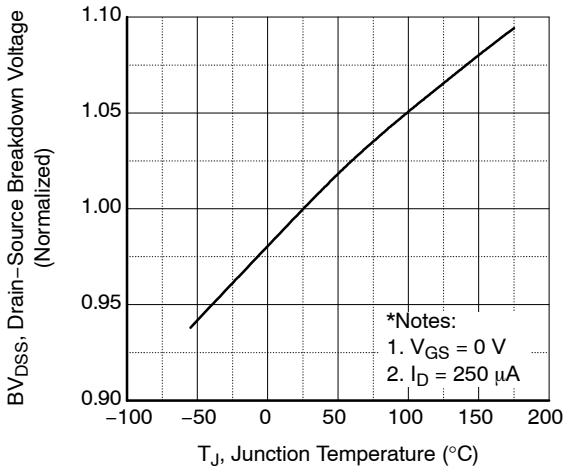


图 7. 击穿电压变化与温度

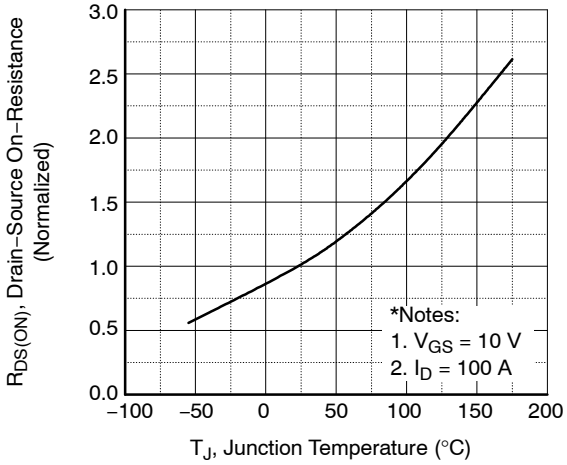


图 8. 导通电阻变化与温度

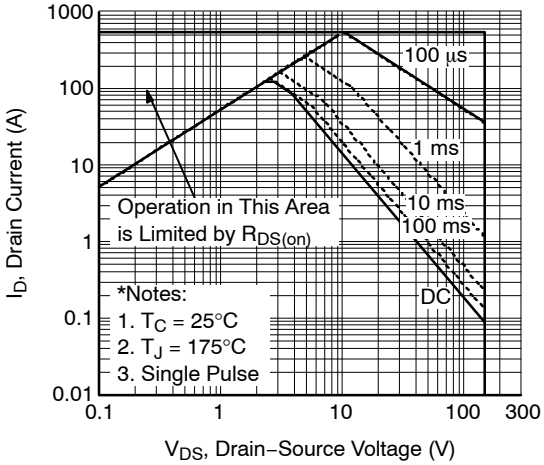


图 9. 最大安全工作区

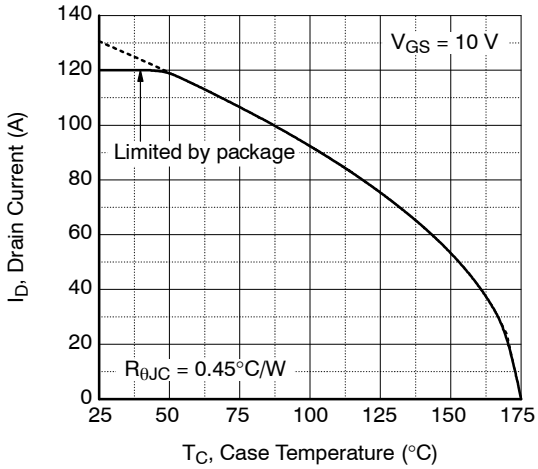


图 10. 最大漏极电流与外壳温度

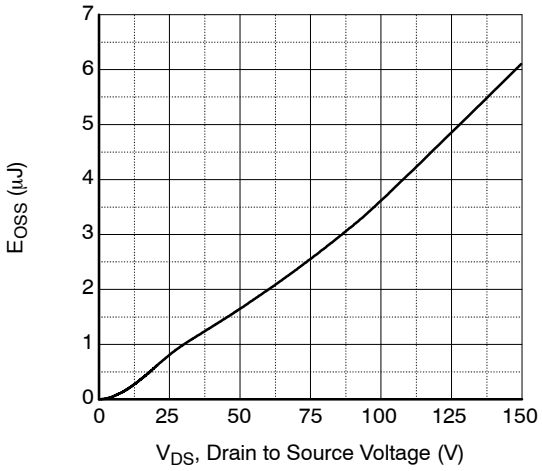


图 11. 输出电容 (Eoss) 与漏极 − 源极电

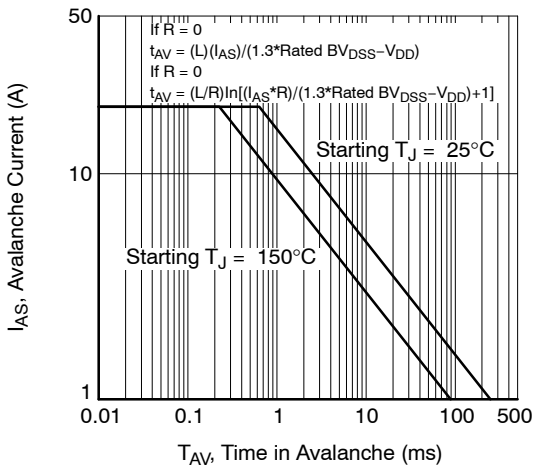


图 12. 非箝位电感开关能力

典型性能特征 (接上页)

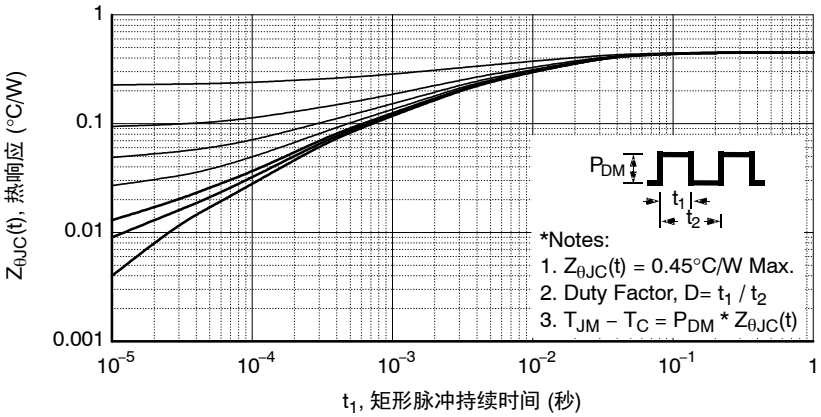


图 13. 瞬态热响应曲线

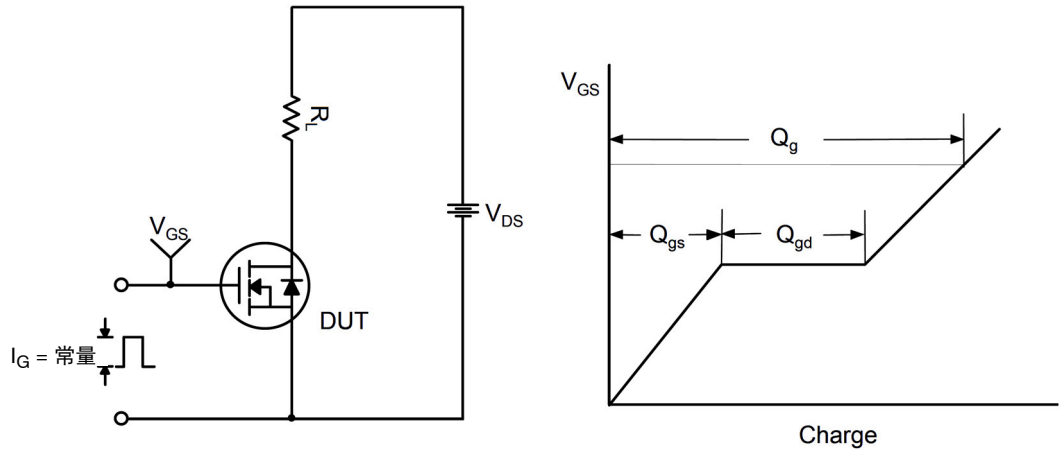


图 14. 栅极电荷测试电路与波形

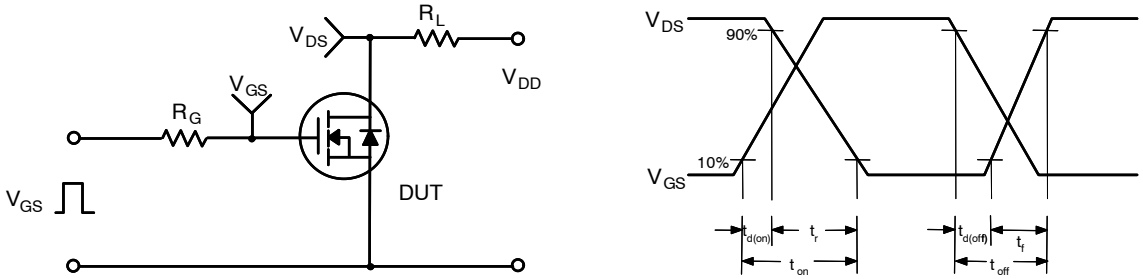


图 15. 阻性开关测试电路与波形

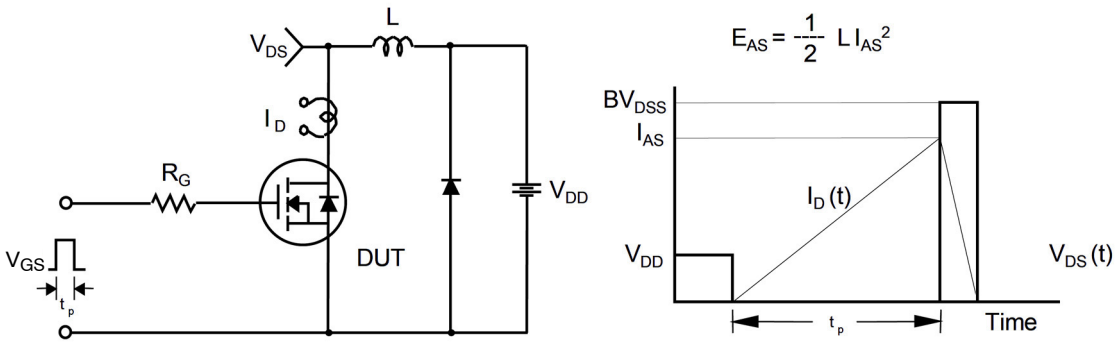


图 16. 非箝位电感开关测试电路与波形

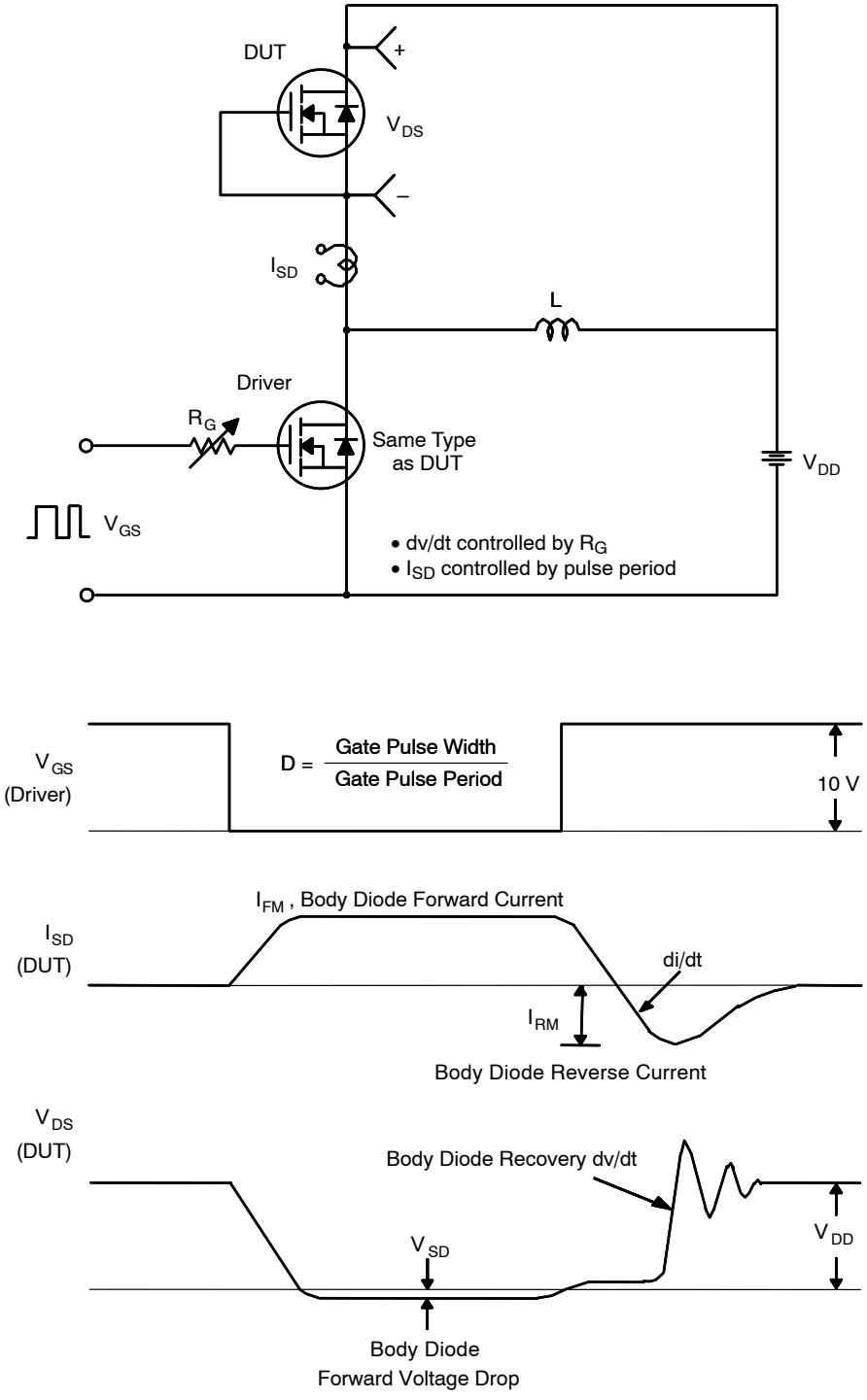


图 17. 二极管恢复 dv/dt 峰值测试电路与波形

封装标识与定购信息

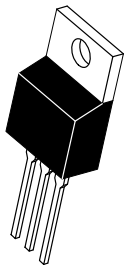
器件编号	顶标	封装	包装方法†	卷尺寸	带宽	数量
FDP075N15A−F102	FDP075N15A	TO−220	塑料管	不适用	不适用	50 个
FDB075N15A	FDB075N15A	D^2−PAK	卷带	330 mm	24 mm	800 个

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

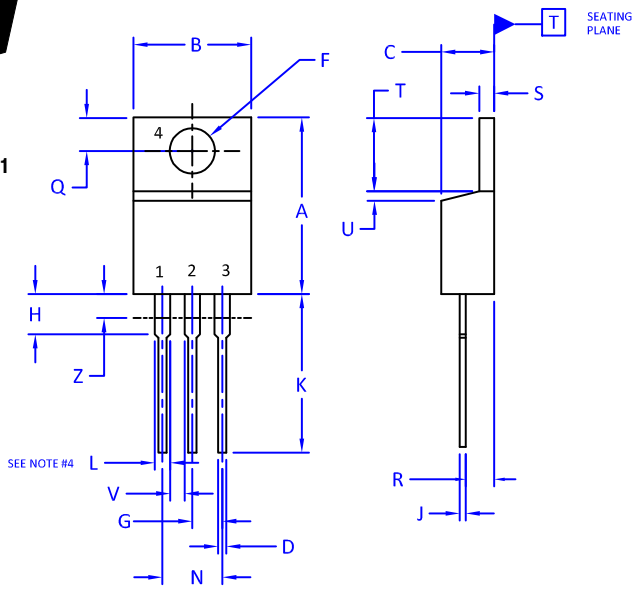
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

TO−220
CASE 221A
ISSUE AK

DATE 13 JAN 2022



SCALE 1:1



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 2009.
2. CONTROLLING DIMENSION: INCHES
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.
4. MAX WIDTH FOR F102 DEVICE = 1.35MM

	INCHES		MILLIMETERS	
DIM	MIN.	MAX.	MIN.	MAX.
A	0.570	0.620	14.48	15.75
B	0.380	0.415	9.66	10.53
C	0.160	0.190	4.07	4.83
D	0.025	0.038	0.64	0.96
F	0.142	0.161	3.60	4.09
G	0.095	0.105	2.42	2.66
H	0.110	0.161	2.80	4.10
J	0.014	0.024	0.36	0.61
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.15	1.41
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
V	0.045	----	1.15	---
Z	----	0.080	---	2.04

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:
PIN 1. BASE
2. EMITTER
3. COLLECTOR
4. EMITTER

STYLE 3:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

STYLE 4:
PIN 1. MAIN TERMINAL 1
2. MAIN TERMINAL 2
3. GATE
4. MAIN TERMINAL 2

STYLE 5:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 6:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE

STYLE 7:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. ANODE

STYLE 8:
PIN 1. CATHODE
2. ANODE
3. EXTERNAL TRIP/DELAY
4. ANODE

STYLE 9:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 10:
PIN 1. GATE
2. SOURCE
3. DRAIN
4. SOURCE

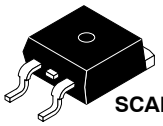
STYLE 11:
PIN 1. DRAIN
2. SOURCE
3. GATE
4. SOURCE

STYLE 12:
PIN 1. MAIN TERMINAL 1
2. MAIN TERMINAL 2
3. GATE
4. NOT CONNECTED

DOCUMENT NUMBER:	**98ASB42148B**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	**TO−220**	**PAGE 1 OF 1**

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

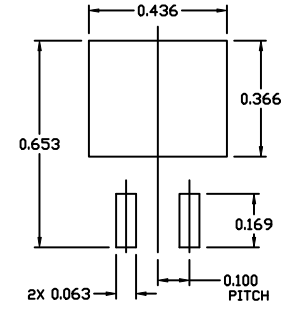
ON Semiconductor®



SCALE 1:1

D²PAK–3 (TO–263, 3–LEAD)
CASE 418AJ
ISSUE F

DATE 11 MAR 2021



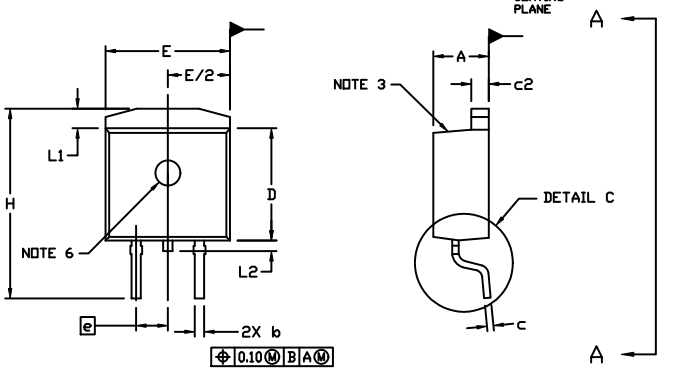
RECOMMENDED
MOUNTING FOOTPRINT

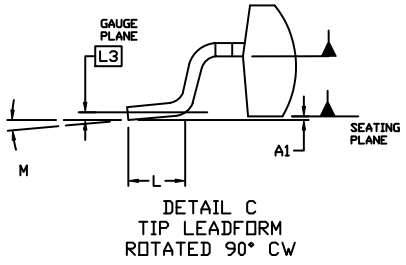
* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

NOTES:

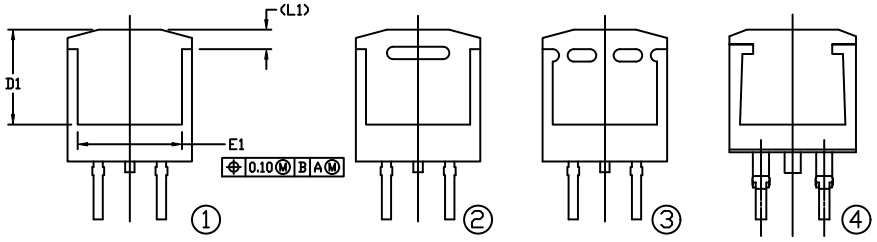
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: INCHES
3. CHAMFER OPTIONAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.005 PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY AT DATUM H.
5. THERMAL PAD CONTOUR IS OPTIONAL WITHIN DIMENSIONS E, L1, D1, AND E1.
6. OPTIONAL MOLD FEATURE.
7. ①, ② ... OPTIONAL CONSTRUCTION FEATURE CALL OUTS.

	INCHES		MILLIMETERS	
DIM	MIN.	MAX.	MIN.	MAX.
A	0.160	0.190	4.06	4.83
A1	0.000	0.010	0.00	0.25
b	0.020	0.039	0.51	0.99
c	0.012	0.029	0.30	0.74
c2	0.045	0.065	1.14	1.65
D	0.330	0.380	8.38	9.65
D1	0.260	---	6.60	---
E	0.380	0.420	9.65	10.67
E1	0.245	---	6.22	---
e	0.100 BSC		2.54 BSC	
H	0.575	0.625	14.60	15.88
L	0.070	0.110	1.78	2.79
L1	---	0.066	---	1.68
L2	---	0.070	---	1.78
L3	0.010 BSC		0.25 BSC	
M	0°	8°	0°	8°





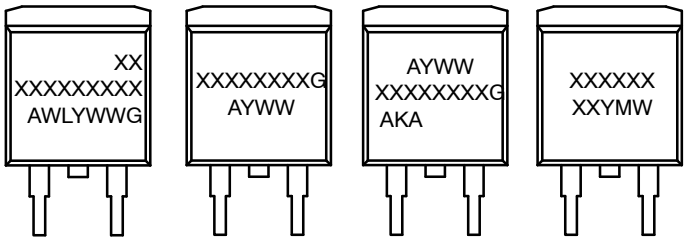
DETAIL C
TIP LEADFORM
ROTATED 90° CW



VIEW A–A

VIEW A–A
OPTIONAL CONSTRUCTIONS

GENERIC MARKING DIAGRAMS*



IC | Standard | Rectifier | SSG

XXXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
W = Week Code (SSG)
M = Month Code (SSG)
G = Pb–Free Package
AKA = Polarity Indicator

*This information is generic. Please refer to device data sheet for actual part marking. Pb–Free indicator, “G” or microdot “ ▪”, may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	**D²PAK–3 (TO–263, 3–LEAD)**	**PAGE 1 OF 1**

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