

MOSFET – N-Channel, POWERTRENCH®

150 V, 37 A, 36 mΩ

FDP2552, FDB2552

Features

- $R_{DS(on)} = 32\text{ m}\Omega$ (Typ.), $V_{GS} = 10\text{ V}$, $I_D = 16\text{ A}$
- $Q_g(tot) = 39\text{ nC}$ (Typ.), $V_{GS} = 10\text{ V}$
- Low Miller Charge
- Low Q_{RR} Body Diode
- UIS Capability (Single Pulse and Repetitive Pulse)
- These Devices are Pb-Free, Halide Free and are RoHS Compliant

Applications

- DC/DC Converters and Off-line UPS
- Distributed Power Architectures and VRMs
- Primary Switch for 24 V and 48 V Systems
- High Voltage Synchronous Rectifier

MOSFET MAXIMUM RATINGS ($T_C = 25^\circ\text{C}$, unless otherwise noted)

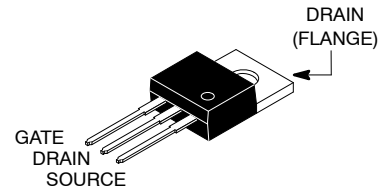
Symbol	Parameter	Ratings	Unit
V_{DSS}	Drain to Source Voltage	150	V
V_{GS}	Gate to Source Voltage	± 20	V
I_D	Drain Current		A
	Continuous ($T_C = 25^\circ\text{C}$, $V_{GS} = 10\text{ V}$)	37	
	Continuous ($T_C = 100^\circ\text{C}$, $V_{GS} = 10\text{ V}$)	26	
	Continuous ($T_{amb} = 25^\circ\text{C}$, $V_{GS} = 10\text{ V}$, with $R_{\theta JA} = 43^\circ\text{C/W}$)	5	
	Pulsed	Figure 4	
E_{AS}	Single Pulse Avalanche Energy (Note 1)	390	mJ
P_D	Power Dissipation	150	W
	Derate above 25°C	1.0	W/ $^\circ\text{C}$
T_J, T_{STG}	Operating and Storage Temperature	-55 to 175	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

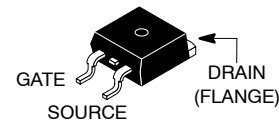
THERMAL CHARACTERISTICS

Symbol	Parameter	Ratings	Unit
$R_{\theta JC}$	Thermal Resistance Junction to Case TO-220, TO-263	1.0	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance Junction to Ambient TO-220, TO-263 (Note 2)	62	
$R_{\theta JA}$	Thermal Resistance Junction to Ambient TO-263, 1 in ² Copper Pad Area	43	

V_{DS}	$R_{DS(on)}\text{ MAX}$	$I_D\text{ MAX}$
150 V	36 mΩ @ 10 V	37 A

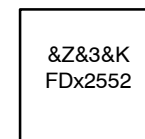


TO-220-3LD
CASE 340AT
FDP SERIES

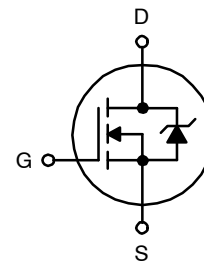


D2PAK-3
(TO-263, 3-LEAD)
CASE 418AJ
FDB SERIES

MARKING DIAGRAM



- &Z = Assembly Plant Code
- &3 = 3-Digit Date Code
- &K = 2-Digits Lot Run Traceability Code
- FDx2552 = Device Code (x = P, B)



N-Channel

ORDERING INFORMATION

See detailed ordering and shipping information on page 12 of this data sheet.

FDP2552, FDB2552

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

B _{VDSS}	Drain to Source Breakdown Voltage	I _D = 250 μA, V _{GS} = 0 V	150	–	–	V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 120 V, V _{GS} = 0 V	–	–	1	μA
		V _{DS} = 120 V, V _{GS} = 0 V, T _C = 150°C	–	–	250	
I _{GSS}	Gate to Source Leakage Current	V _{GS} = ±20 V	–	–	±100	nA

ON CHARACTERISTICS

V _{GS(TH)}	Gate to Source Threshold Voltage	V _{GS} = V _{DS} , I _D = 250 μA	2	–	4	V
R _{DS(on)}	Drain to Source On Resistance	I _D = 16 A, V _{GS} = 10 V	–	0.032	0.036	Ω
		I _D = 8 A, V _{GS} = 6 V	–	0.036	0.054	
		I _D = 16 A, V _{GS} = 10 V, T _J = 175°C	–	0.084	0.097	

DYNAMIC CHARACTERISTICS

C _{ISS}	Input Capacitance	V _{DS} = 25 V, V _{GS} = 0 V, f = 1 MHz	–	2800	–	pF
C _{OSS}	Output Capacitance		–	285	–	pF
C _{RSS}	Reverse Transfer Capacitance		–	55	–	pF
Q _{g(TOT)}	Total Gate Charge at 10 V	V _{GS} = 0 V to 10 V, V _{DD} = 75 V, I _D = 16 A, I _g = 1.0 mA	–	39	51	nC
Q _{g(TH)}	Threshold Gate Charge	V _{GS} = 0 V to 2 V, V _{DD} = 75 V, I _D = 16 A, I _g = 1.0 mA	–	5.2	6.8	nC
Q _{gs}	Gate to Source Gate Charge	V _{DD} = 75 V, I _D = 16 A, I _g = 1.0 mA	–	13.5	–	nC
Q _{gs2}	Gate Charge Threshold to Plateau		–	8.4	–	nC
Q _{gd}	Gate to Drain "Miller" Charge		–	8.3	–	nC

SWITCHING CHARACTERISTICS (V_{GS} = 10 V)

t _{ON}	Turn-On Time	V _{DD} = 75 V, I _D = 16 A, V _{GS} = 10 V, R _{GS} = 8.2 Ω	–	–	62	ns
t _{d(ON)}	Turn-On Delay Time		–	12	–	ns
t _r	Rise Time		–	29	–	ns
t _{d(OFF)}	Turn-Off Delay Time		–	36	–	ns
t _f	Fall Time		–	29	–	ns
t _{OFF}	Turn-Off Time		–	–	97	ns

DRAIN-SOURCE CHARACTERISTICS

V _{SD}	Source to Drain Diode Voltage	I _{SD} = 16 A	–	–	1.25	V
		I _{SD} = 8 A	–	–	1.0	V
t _{rr}	Reverse Recovery Time	I _{SD} = 16 A, dI _{SD} /dt = 100 A/μs	–	–	90	ns
Q _{RR}	Reverse Recovery Charge	I _{SD} = 16 A, dI _{SD} /dt = 100 A/μs	–	–	242	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

- Starting T_J = 25°C, L = 7.8 mH, I_{AS} = 10 A.
- Pulse Width = 100 μs.

FDP2552, FDB2552

Typical Characteristics ($T_C = 25^\circ\text{C}$, unless otherwise noted)

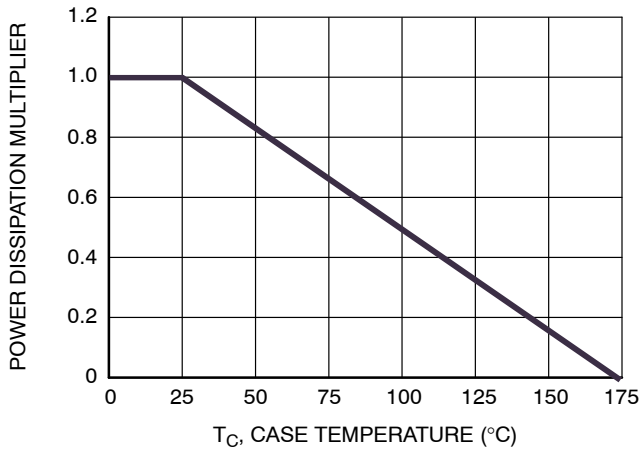


Figure 1. Normalized Power Dissipation vs. Ambient Temperature

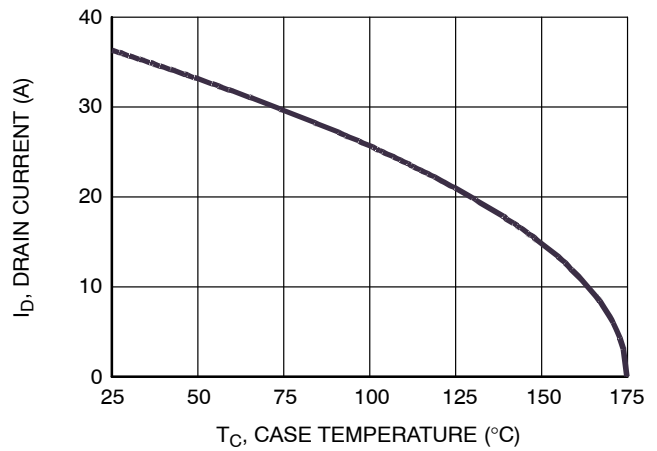


Figure 2. Maximum Continuous Drain Current vs. Case Temperature

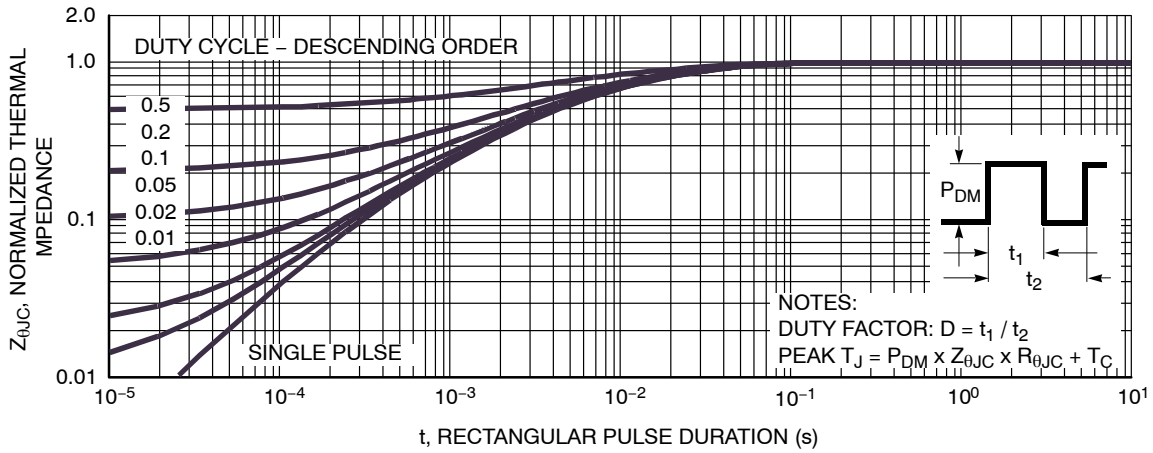


Figure 3. Normalized Maximum Transient Thermal Impedance

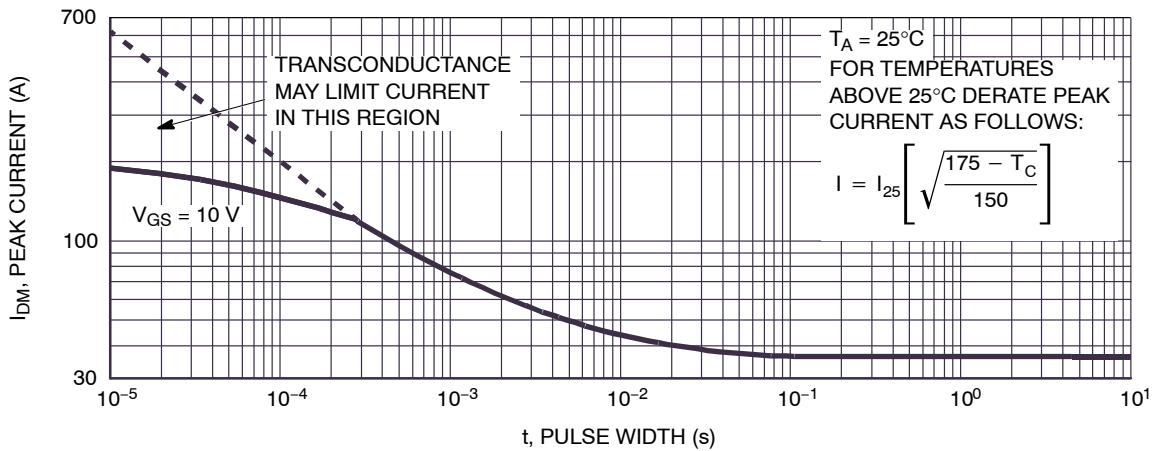


Figure 4. Peak Current Capability

Typical Characteristics ($T_C = 25^\circ\text{C}$, unless otherwise noted) (continued)

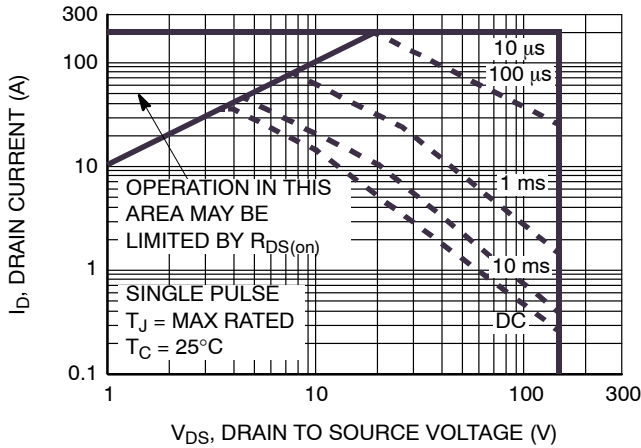
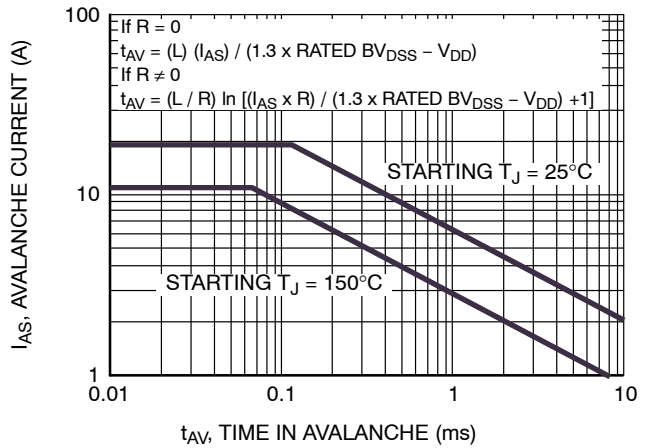


Figure 5. Forward Bias Safe Operating Area



NOTE: Refer to onsemi Application Notes AN7514 and AN7515

Figure 6. Unclamped Inductive Switching Capability

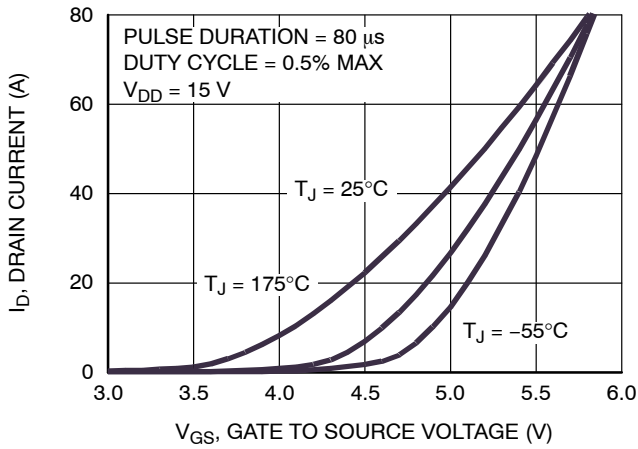


Figure 7. Transfer Characteristics

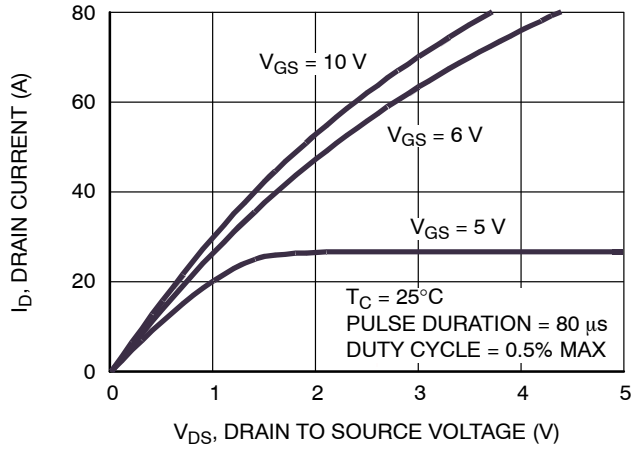


Figure 8. Saturation Characteristics

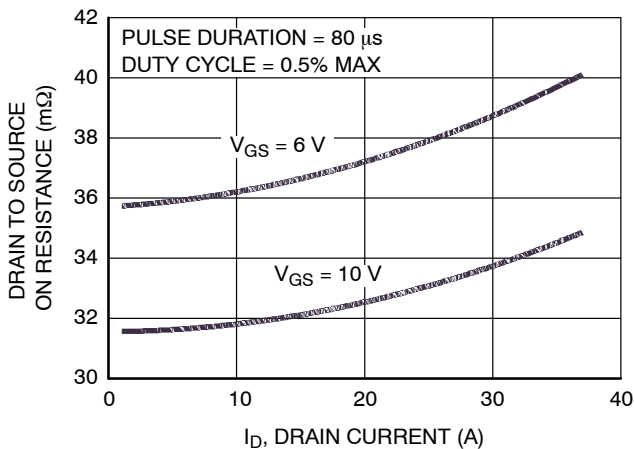


Figure 9. Drain to Source On Resistance vs. Drain Current

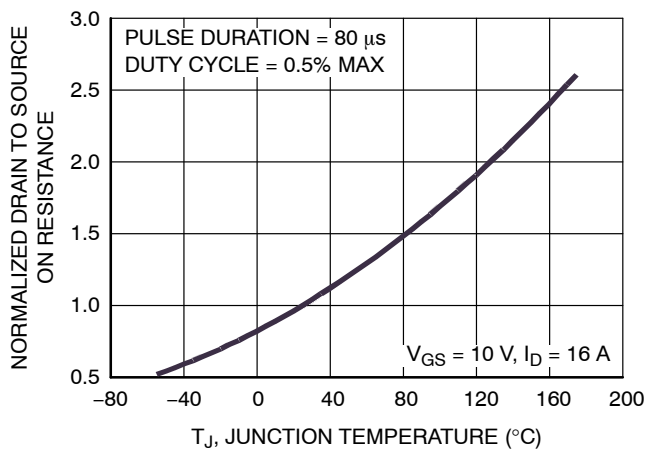


Figure 10. Normalized Drain to Source On Resistance vs. Junction Temperature

Typical Characteristics ($T_C = 25^\circ\text{C}$, unless otherwise noted) (continued)

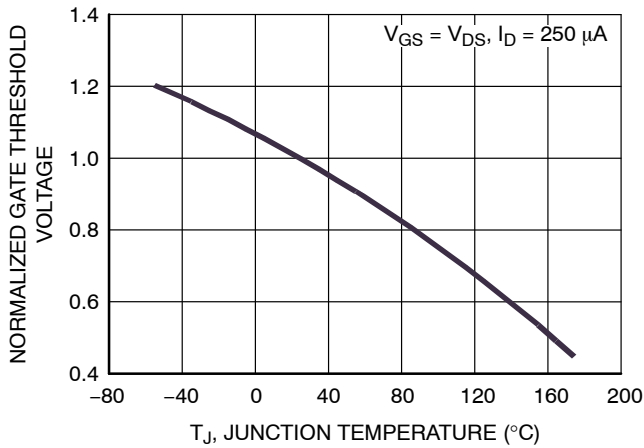


Figure 11. Normalized Gate Threshold Voltage vs. Junction Temperature

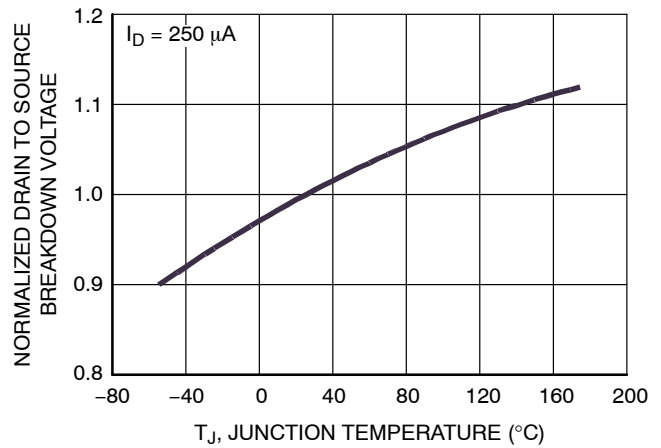


Figure 12. Normalized Drain to Source Breakdown Voltage vs. Junction Temperature

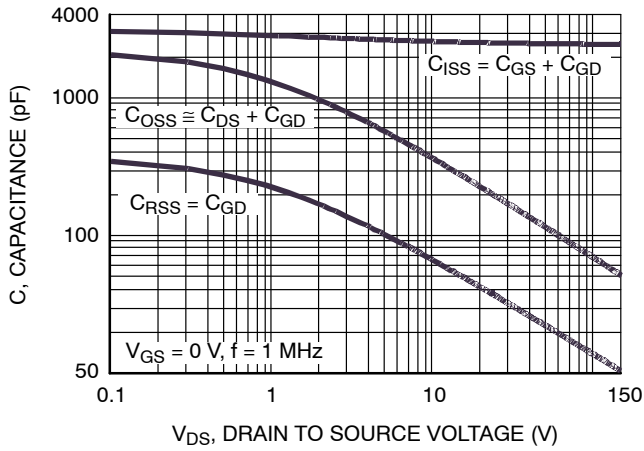


Figure 13. Capacitance vs. Drain to Source Voltage

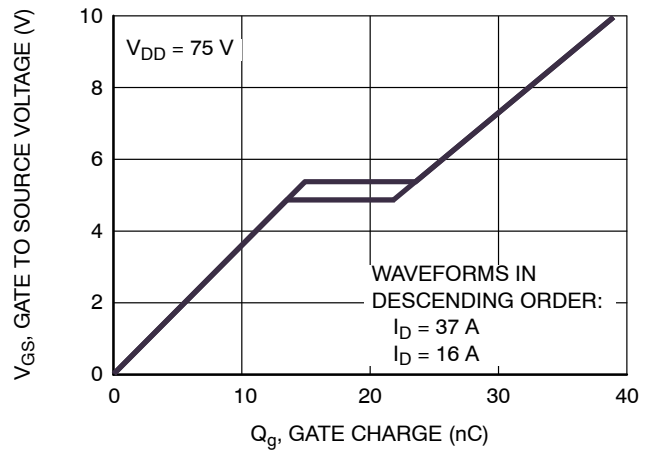


Figure 14. Gate Charge Waveforms for Constant Gate Currents

Test Circuits and Waveforms

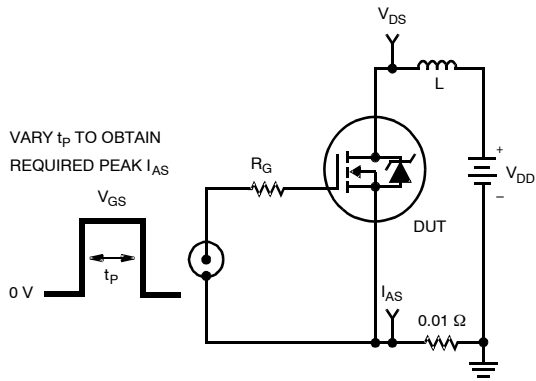


Figure 15. Unclamped Energy Test Circuit

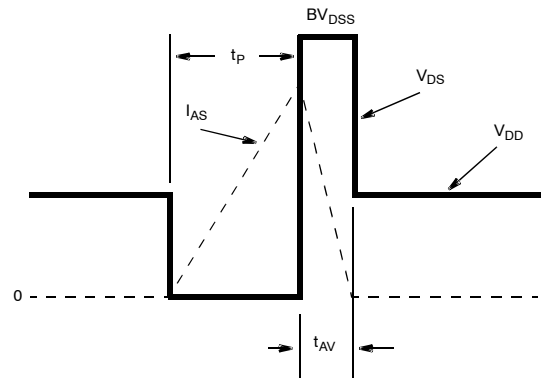


Figure 16. Unclamped Energy Waveforms

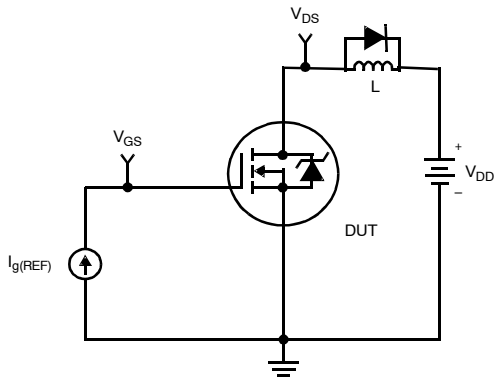


Figure 17. Gate Charge Test Circuit

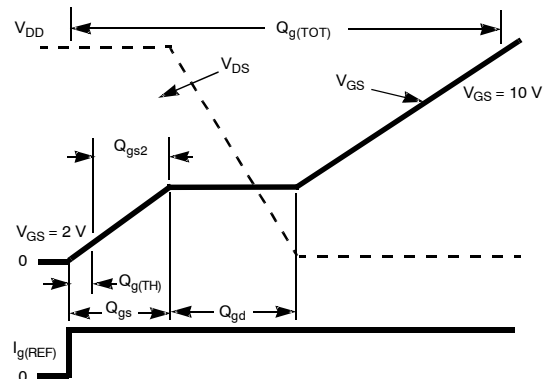


Figure 18. Gate Charge Waveforms

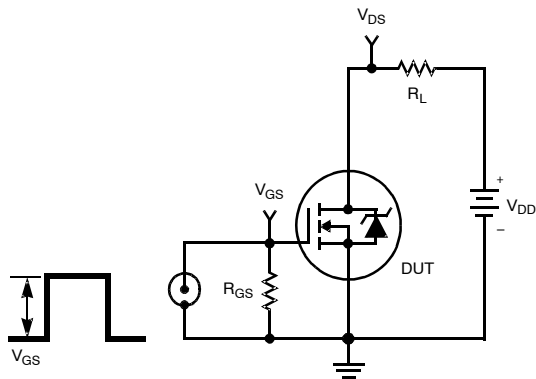


Figure 19. Switching Time Test Circuit

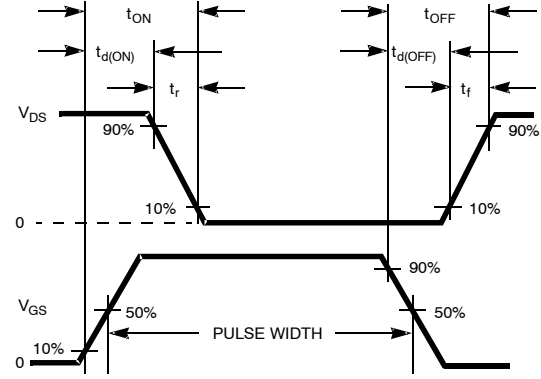


Figure 20. Switching Time Waveforms

Thermal Resistance vs. Mounting Pad Area

The maximum rated junction temperature, T_{JM} , and the thermal resistance of the heat dissipating path determines the maximum allowable device power dissipation, P_{DM} , in an application. Therefore the application’s ambient temperature, T_A (°C), and thermal resistance $R_{\theta JA}$ (°C/W) must be reviewed to ensure that T_{JM} is never exceeded. Equation 1 mathematically represents the relationship and serves as the basis for establishing the rating of the part.

$$P_{DM} = \frac{(T_{JM} - T_A)}{R_{\theta JA}} \quad \text{(eq. 1)}$$

In using surface mount devices such as the TO–263 package, the environment in which it is applied will have a significant influence on the part’s current and maximum power dissipation ratings. Precise determination of P_{DM} is complex and influenced by many factors:

1. Mounting pad area onto which the device is attached and whether there is copper on one side or both sides of the board.
2. The number of copper layers and the thickness of the board.
3. The use of external heat sinks.
4. The use of thermal vias.
5. Air flow and board orientation.
6. For non steady state applications, the pulse width, the duty cycle and the transient thermal response of the part, the board and the environment they are in.

onsemi provides thermal information to assist the designer’s preliminary application evaluation. Figure 21 defines the $R_{\theta JA}$ for the device as a function of the top copper (component side) area. This is for a horizontally positioned FR–4 board with 1 oz copper after 1000 seconds of steady state power with no air flow. This graph provides the necessary information for calculation of the steady state junction temperature or power dissipation. Pulse applications

can be evaluated using the **onsemi** device Spice thermal model or manually utilizing the normalized maximum transient thermal impedance curve.

Thermal resistances corresponding to other copper areas can be obtained from Figure 21 or by calculation using Equation 2 or 3. Equation 2 is used for copper area defined in inches square and Equation 3 is for area in centimeters square. The area, in square inches or square centimeters is the top copper area including the gate and source pads.

$$R_{\theta JA} = 26.51 + \frac{19.84}{(0.262 + \text{Area})} \quad \text{(eq. 2)}$$

Area in Inches Squared

$$R_{\theta JA} = 26.51 + \frac{128}{(1.69 + \text{Area})} \quad \text{(eq. 3)}$$

Area in Centimeters Squared

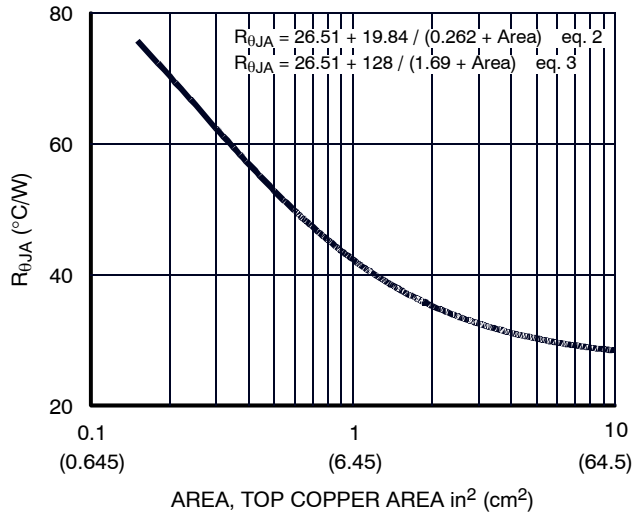


Figure 21. Thermal Resistance vs. Mounting Pad Area

FDP2552, FDB2552

PSPICE Electrical Model

.SUBCKT FDP2552 2 1 3 ; rev May 2002

Ca 12 8 1e-9

Cb 15 14 1e-9

Cin 6 8 2.65e-9

Dbody 7 5 DbodyMOD

Dbreak 5 11 DbreakMOD

Dplcap 10 5 DplcapMOD

Ebreak 11 7 17 18 178

Eds 14 8 5 8 1

Egs 13 8 6 8 1

Esg 6 10 6 8 1

Evthres 6 21 19 8 1

Evttemp 20 6 18 22 1

It 8 17 1

Lgate 1 9 7.15e-9

Ldrain 2 5 1.0e-9

Lsource 3 7 2.3e-9

RLgate 1 9 71.5

RLdrain 2 5 10

RLsource 3 7 23

Mmed 16 6 8 8 MmedMOD

Mstro 16 6 8 8 MstroMOD

Mweak 16 21 8 8 MweakMOD

Rbreak 17 18 RbreakMOD 1

Rdrain 50 16 RdrainMOD 2.5e-2

Rgate 9 20 1.04

RSLC1 5 51 RSLCMOD 1.0e-6

RSLC2 5 50 1.0e3

Rsource 8 7 RsourceMOD 4.6e-3

Rvthres 22 8 RvthresMOD 1

Rvtemp 18 19 RvtempMOD 1

S1a 6 12 13 8 S1AMOD

S1b 13 12 13 8 S1BMOD

S2a 6 15 14 13 S2AMOD

S2b 13 15 14 13 S2BMOD

Vbat 22 19 DC 1

ESLC 51 50 VALUE={ (V(5,51)/ABS(V(5,51))) * (PWR(V(5,51)/(1e-6*75),3)) }

.MODEL DbodyMOD D (IS=2.6E-11 N=1.09 RS=2.6e-3 TRS1=3.0e-3 TRS2=1.5e-6
+ CJO=1.9e-9 M=0.62 TT=5.1e-8 XTI=4.2)

.MODEL DbreakMOD D (RS=0.3 TRS1=3.0e-3 TRS2=-8.9e-6)

.MODEL DplcapMOD D (CJO=5.7e-10 IS=1.0e-30 N=10 M=0.58)

.MODEL MmedMOD NMOS (VTO=3.5 KP=6 IS=1e-30 N=10 TOX=1 L=1u W=1u RG=1.04)

.MODEL MstroMOD NMOS (VTO=4.15 KP=80 IS=1e-30 N=10 TOX=1 L=1u W=1u)

.MODEL MweakMOD NMOS (VTO=2.91 KP=0.03 IS=1e-30 N=10 TOX=1 L=1u W=1u RG=10.4 RS=0.1)

FDP2552, FDB2552

```

.MODEL RbreakMOD RES (TC1=1.1e-3 TC2=-2e-6)
.MODEL RdrainMOD RES (TC1=8.5e-3 TC2=2.5e-5)
.MODEL RSLCMOD RES (TC1=3.4e-3 TC2=1.5e-6)
.MODEL RsourceMOD RES (TC1=4.0e-3 TC2=1.0e-6)
.MODEL RvthresMOD RES (TC1=-4.3e-3 TC2=-1.6e-5)
.MODEL RvtempMOD RES (TC1=-4.1e-3 TC2=1.5e-6)

.MODEL S1AMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-6.0 VOFF=-4.0)
.MODEL S1BMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-4.0 VOFF=-6.0)
.MODEL S2AMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-2 VOFF=-0.5)
.MODEL S2BMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-0.5 VOFF=-2)

```

.ENDS

NOTE: Note: For further discussion of the PSPICE model, consult *A New PSPICE Sub-Circuit for the Power MOSFET Featuring Global Temperature Options*; IEEE Power Electronics Specialist Conference Records, 1991, written by William J. Hepp and C. Frank Wheatley.

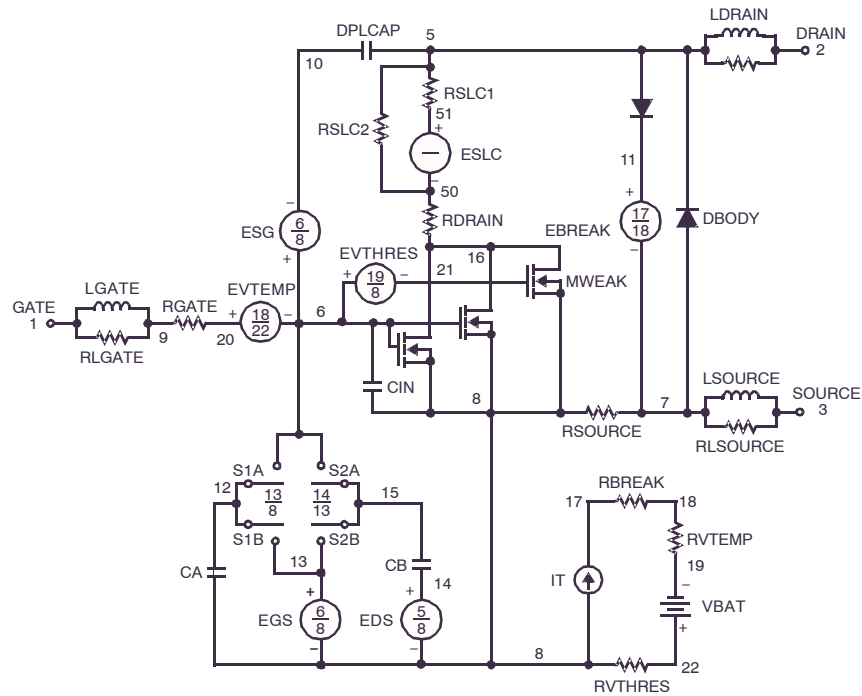


Figure 22.

FDP2552, FDB2552

SABER Electrical Model

REV May 2002

template FDP2552 n2,n1,n3

electrical n2,n1,n3

```
{
var i iscl
dp..model dbodymod = (isl=2.6e-11,nl=1.09,rs=2.6e-3,trs1=3.0e-3,trs2=1.5e-6,cjo=1.9e-9,m=0.62,tt=5.1e-8,xti=4.2)
dp..model dbreakmod = (rs=0.3,trs1=3.0e-3,trs2=-8.9e-6)
dp..model dplcapmod = (cjo=5.7e-10,isl=10.0e-30,nl=10,m=0.58)
m..model mmedmod = (type=_n,vto=3.5,kp=6,is=1e-30, tox=1)
m..model mstrongmod = (type=_n,vto=4.15,kp=80,is=1e-30, tox=1)
m..model mweakmod = (type=_n,vto=2.91,kp=0.03,is=1e-30, tox=1,rs=0.1)
sw_vcsp..model s1amod = (ron=1e-5,roff=0.1,von=-6.0,voff=-4.0)
sw_vcsp..model s1bmod = (ron=1e-5,roff=0.1,von=-4.0,voff=-6.0)
sw_vcsp..model s2amod = (ron=1e-5,roff=0.1,von=-2,voff=-0.5)
sw_vcsp..model s2bmod = (ron=1e-5,roff=0.1,von=-0.5,voff=-2)
c.ca n12 n8 = 1e-9
c.cb n15 n14 = 1e-9
c.cin n6 n8 = 2.65e-9
```

```
dp.dbody n7 n5 = model=dbodymod
dp.dbreak n5 n11 = model=dbreakmod
dp.dplcap n10 n5 = model=dplcapmod
```

```
spe.ebreak n11 n7 n17 n18 = 178
spe.eds n14 n8 n5 n8 = 1
spe.egs n13 n8 n6 n8 = 1
spe.esg n6 n10 n6 n8 = 1
spe.evthres n6 n21 n19 n8 = 1
spe.evtemp n20 n6 n18 n22 = 1
```

```
i.it n8 n17 = 1
```

```
l.lgate n1 n9 = 7.15e-9
l.l drain n2 n5 = 1.0e-9
l.l source n3 n7 = 2.3e-9
```

```
res.rlgate n1 n9 = 71.5
res.rl drain n2 n5 = 10
res.rl source n3 n7 = 23
```

```
m.mmed n16 n6 n8 n8 = model=mmedmod, l=1u, w=1u
m.mstrong n16 n6 n8 n8 = model=mstrongmod, l=1u, w=1u
m.mweak n16 n21 n8 n8 = model=mweakmod, l=1u, w=1u
```

```
res.rbreak n17 n18 = 1, tc1=1.1e-3,tc2=-2e-6
res.r drain n50 n16 = 2.5e-2, tc1=8.5e-3,tc2=2.5e-5
res.r gate n9 n20 = 1.04
res.rslc1 n5 n51 = 1.0e-6, tc1=3.4e-3,tc2=1.5e-6
res.rslc2 n5 n50 = 1.0e3
res.r source n8 n7 = 4.6e-3, tc1=4.0e-3,tc2=1.0e-6
res.rvthres n22 n8 = 1, tc1=-4.3e-3,tc2=-1.6e-5
res.rvtemp n18 n19 = 1, tc1=-4.1e-3,tc2=1.5e-6
```

FDP2552, FDB2552

```

sw_vcsp.s1a n6 n12 n13 n8 = model=s1amod
sw_vcsp.s1b n13 n12 n13 n8 = model=s1bmod
sw_vcsp.s2a n6 n15 n14 n13 = model=s2amod
sw_vcsp.s2b n13 n15 n14 n13 = model=s2bmod

```

v.vbat n22 n19 = dc=1

equations {

i (n51->n50) +=iscl

iscl: v(n51,n50) = ((v(n5,n51)/(1e-9+abs(v(n5,n51))))*((abs(v(n5,n51)*1e6/75))** 3))

}
}

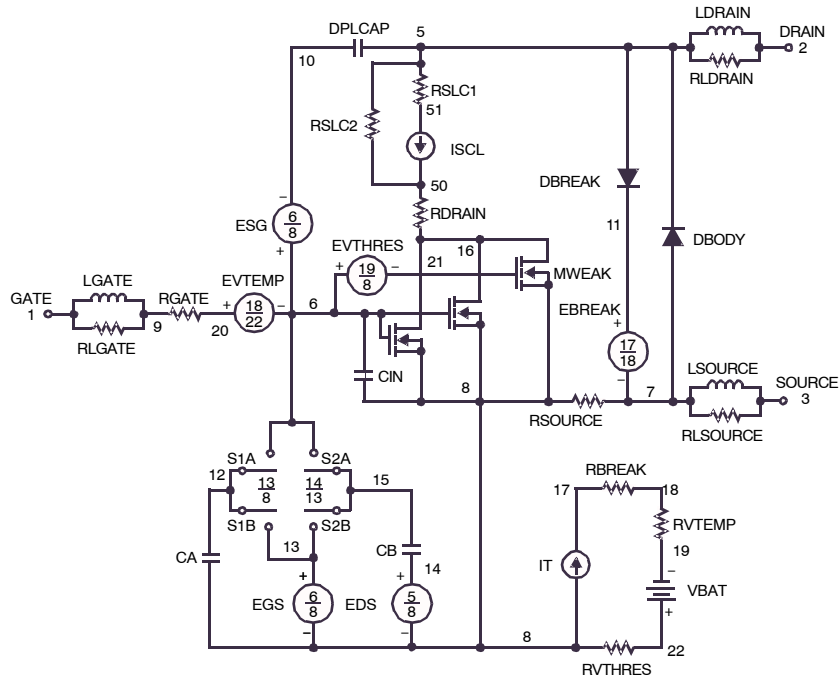


Figure 23.

FDP2552, FDB2552

SPICE THERMAL MODEL

REV 23 May 2002

FDP2552T

CTHERM1 TH 6 1e-2
 CTHERM2 6 5 1.5e-2
 CTHERM3 5 4 2e-2
 CTHERM4 4 3 2.1e-2
 CTHERM5 3 2 2.2e-2
 CTHERM6 2 TL 9e-2

RTHERM1 TH 6 2.7e-2
 RTHERM2 6 5 2.8e-2
 RTHERM3 5 4 7.8e-2
 RTHERM4 4 3 9e-2
 RTHERM5 3 2 2.7e-1
 RTHERM6 2 TL 2.87e-1

SABER THERMAL MODEL

SABER thermal model FDP2552T

template thermal_model th tl
 thermal_c th, tl

```
{
ctherm.ctherm1 th 6 =1e-2
ctherm.ctherm2 6 5 =1.5e-2
ctherm.ctherm3 5 4 =2e-2
ctherm.ctherm4 4 3 =2.1e-2
ctherm.ctherm5 3 2 =2.2e-2
ctherm.ctherm6 2 tl =9e-2
```

```
rtherm.rtherm1 th 6 =2.7e-2
rtherm.rtherm2 6 5 =2.8e-2
rtherm.rtherm3 5 4 =7.8e-2
rtherm.rtherm4 4 3 =9e-2
rtherm.rtherm5 3 2 =2.7e-1
rtherm.rtherm6 2 tl =2.87e-1
}
```

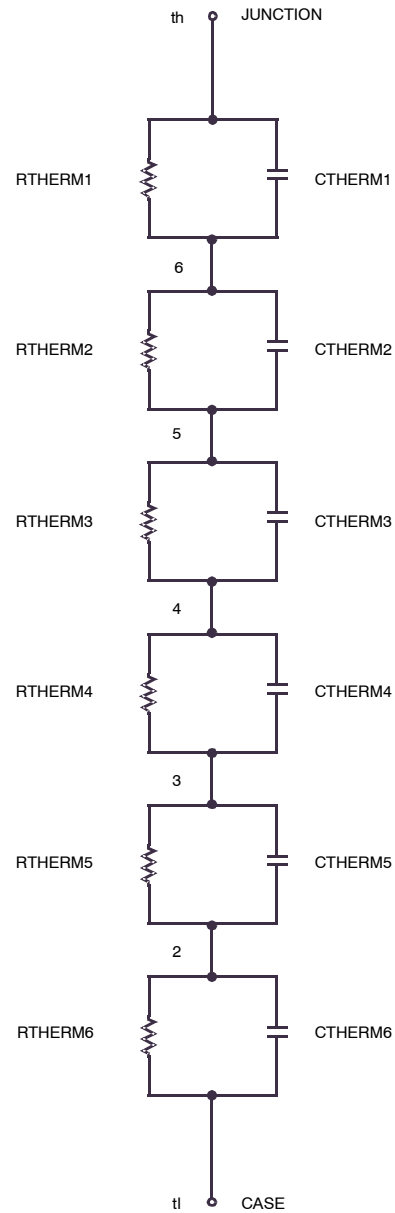


Figure 24.

PACKAGE MARKING AND ORDERING INFORMATION

Device	Device Marking	Package	Reel Size	Tape Width	Quantity†
FDB2552	FDB2552	TO-263, 3-LEAD (Pb-Free, Halide Free)	330 mm	24 mm	800 Units / Tape & Reel
FDP2552	FDP2552	TO-220-3LD (Pb-Free, Halide Free)	Tube	N/A	8000 Units / Tube

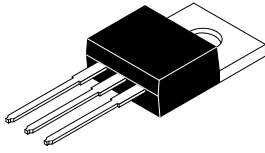
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

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MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

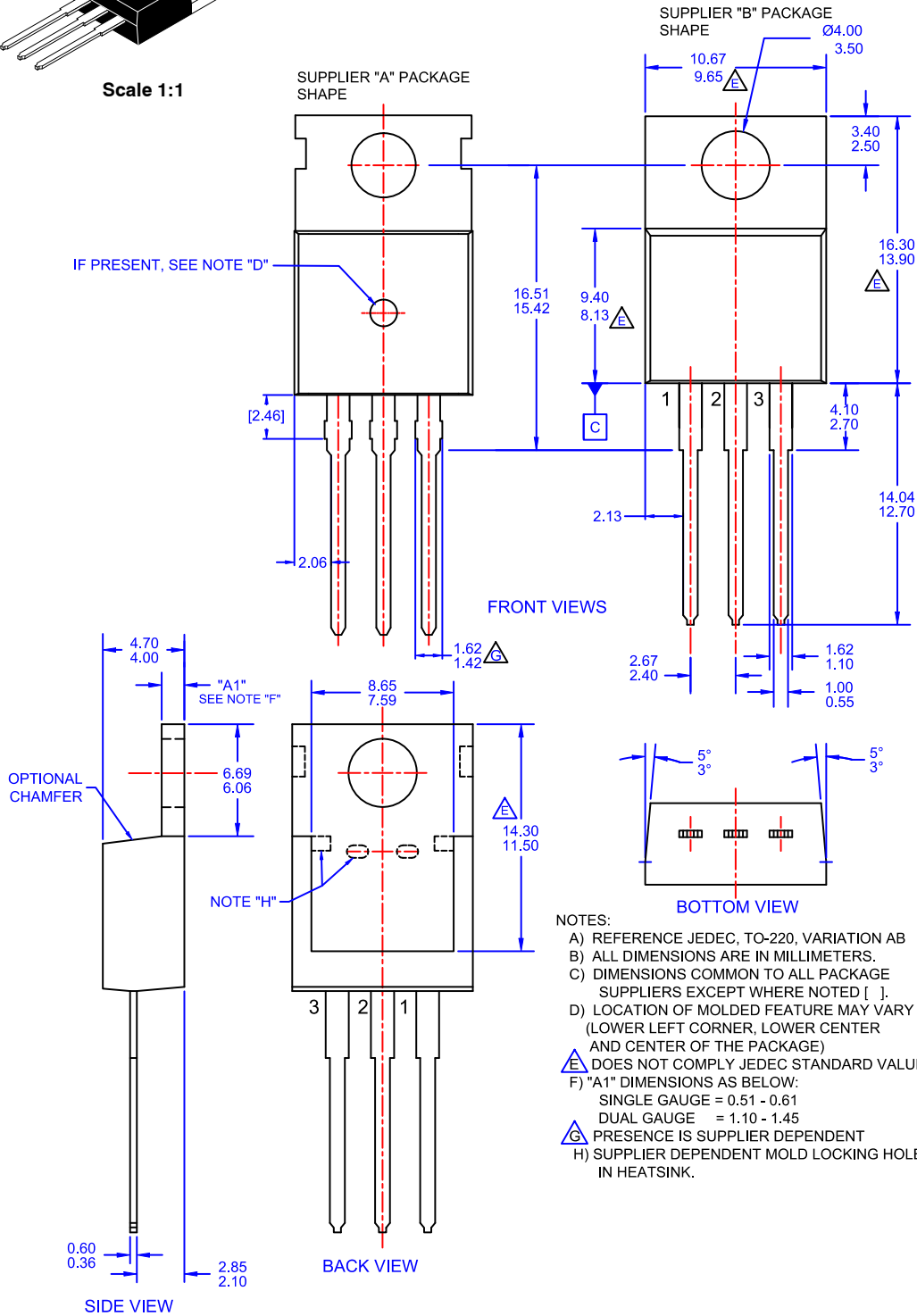
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Scale 1:1

TO-220-3LD CASE 340AT ISSUE A

DATE 03 OCT 2017



- NOTES:
- A) REFERENCE JEDEC, TO-220, VARIATION AB
 - B) ALL DIMENSIONS ARE IN MILLIMETERS.
 - C) DIMENSIONS COMMON TO ALL PACKAGE SUPPLIERS EXCEPT WHERE NOTED [].
 - D) LOCATION OF MOLDED FEATURE MAY VARY (LOWER LEFT CORNER, LOWER CENTER AND CENTER OF THE PACKAGE)
 - E) DOES NOT COMPLY JEDEC STANDARD VALUE.
 - F) "A1" DIMENSIONS AS BELOW:
 SINGLE GAUGE = 0.51 - 0.61
 DUAL GAUGE = 1.10 - 1.45
 - G) PRESENCE IS SUPPLIER DEPENDENT
 - H) SUPPLIER DEPENDENT MOLD LOCKING HOLES IN HEATSINK.

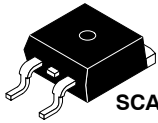
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DESCRIPTION:	TO-220-3LD	PAGE 1 OF 1

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MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

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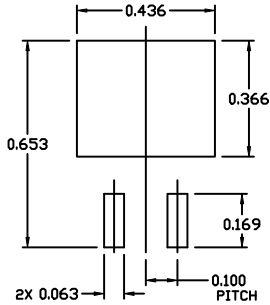
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D²PAK-3 (TO-263, 3-LEAD)

CASE 418AJ

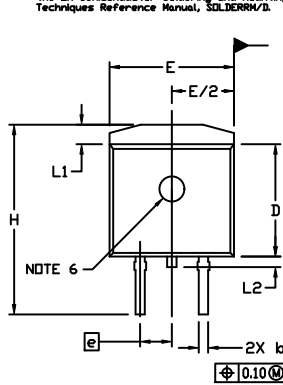
ISSUE F

DATE 11 MAR 2021



RECOMMENDED MOUNTING FOOTPRINT

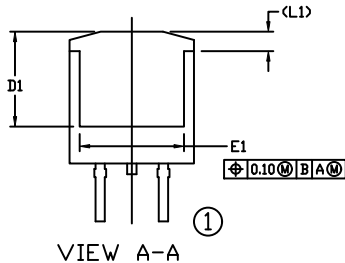
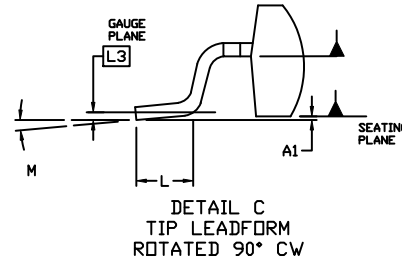
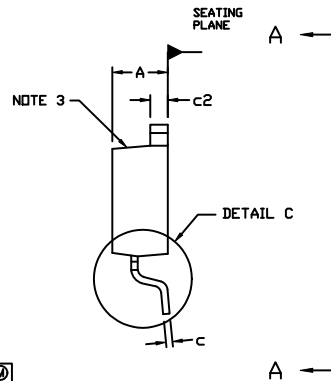
For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.



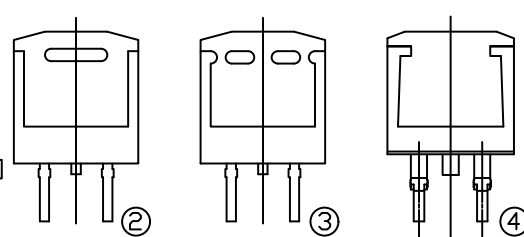
NOTES:

- DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
- CONTROLLING DIMENSION: INCHES
- CHAMFER OPTIONAL.
- DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.005 PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY AT DATUM H.
- THERMAL PAD CONTOUR IS OPTIONAL WITHIN DIMENSIONS E, L1, D1, AND E1.
- OPTIONAL MOLD FEATURE.
- ①, ② ... OPTIONAL CONSTRUCTION FEATURE CALL OUTS.

DIM	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	0.160	0.190	4.06	4.83
A1	0.000	0.010	0.00	0.25
b	0.020	0.039	0.51	0.99
c	0.012	0.029	0.30	0.74
c2	0.045	0.065	1.14	1.65
D	0.330	0.380	8.38	9.65
D1	0.260	---	6.60	---
E	0.380	0.420	9.65	10.67
E1	0.245	---	6.22	---
e	0.100	BSC	2.54	BSC
H	0.575	0.625	14.60	15.88
L	0.070	0.110	1.78	2.79
L1	---	0.066	---	1.68
L2	---	0.070	---	1.78
L3	0.010	BSC	0.25	BSC
M	0*	8*	0*	8*

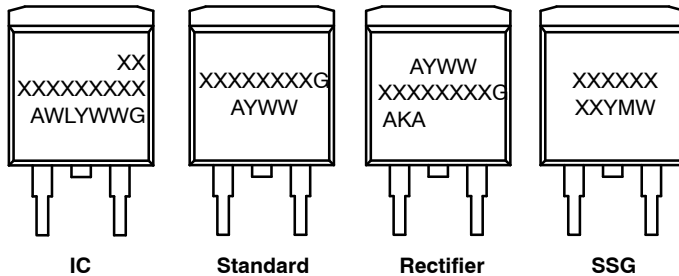


VIEW A-A



VIEW A-A
OPTIONAL CONSTRUCTIONS

GENERIC MARKING DIAGRAMS*



IC

Standard

Rectifier

SSG

- XXXXXX = Specific Device Code
- A = Assembly Location
- WL = Wafer Lot
- Y = Year
- WW = Work Week
- W = Week Code (SSG)
- M = Month Code (SSG)
- G = Pb-Free Package
- AKA = Polarity Indicator

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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