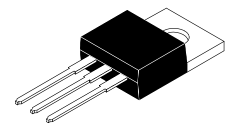
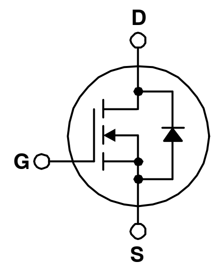
MOSFET – N-Channel, POWERTRENCH®

105 V, 41 A, 33 mΩ

FDP3672



TO−220−3LD
CASE 340AT



Features

- $R_{DS(on)}$ = 25 mΩ (Typ.) @ V_{GS} = 10 V, I_D = 41 A
- $Q_{G(tot)}$ = 28 nC (Typ.) @ V_{GS} = 10 V
- Low Miller Charge
- Low Q_{rr} Body Diode
- Optimized Efficiency at High Frequencies
- UIS Capability (Single Pulse and Repetitive Pulse)

Applications

- Consumer Appliances
- Synchronous Rectification
- Battery Protection Circuit
- Motor Drives and Uninterruptible Power Supplies
- Micro Solar Inverter

MOSFET MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

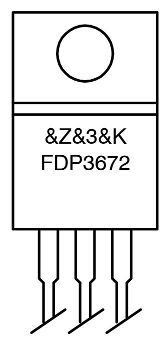
Symbol	Parameter	Value	Unit
V_{DSS}	Drain to Source Voltage	105	V
V_{GS}	Gate to Source Voltage	±20	V
I_D	Drain Current Continuous (T_C = 25°C, V_{GS} = 10 V) Continuous (T_C = 100°C, V_{GS} = 10 V) Continuous (T_{amb} = 25°C, V_{GS} = 10 V, $R_{\theta JA}$ = 62°C/W) Pulsed	 41 31 5.9 Fig. 4	A
E_{AS}	Single Pulsed Avalanche Energy (Note 1)	48	mJ
P_D	Power Dissipation Derate above 25°C	135 0.9	W W/°C
T_J, T_{STG}	Operating and Storage Temperature	−55 to 175	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	1.11	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max. (Note 2)	62	

MARKING DIAGRAM



&Z = Assembly Location
&3 = Date Code (Year & Week)
&K = Lot Run Traceability Code
FDP3672 = Specific Device Code

ORDERING INFORMATION

Device	Package	Shipping
FDP3672	TO−220−3LD	800 Units / Tube

© Semiconductor Components Industries, LLC, 2002

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 250 μA, V_{GS} = 0 V	105	–	–	V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 80 V	–	–	1	μA
		V_{GS} = 0 V, T_C = 150°C	–	–	250	
I_{GSS}	Gate to Body Leakage Current	V_{GS} = ±20	–	–	±100	nA
ON CHARACTERISTICS						
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 250 μA	2	–	4	V
$R_{DS(on)}$	Drain to Source On Resistance	I_D = 41 A, V_{GS} = 10 V I_D = 21 A, V_{GS} = 6 V I_D = 41 A, V_{GS} = 10 V, T_C = 175°C	– – –	0.025 0.031 0.063	0.033 0.055 0.070	Ω
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = 25 V, V_{GS} = 0 V, f = 1 MHz	–	1670	–	pF
C_{oss}	Output Capacitance		–	240	–	
C_{rss}	Reverse Transfer Capacitance		–	55	–	
$Q_{g(tot)}$	Total Gate Charge at 10 V	V_{GS} = 0 V to 10 V, V_{DD} = 50 V, I_D = 41 A, I_G = 1.0 mA	–	28	37	nC
$Q_{g(th)}$	Threshold Gate Charge	V_{GS} = 0 V to 2 V, V_{DD} = 50 V, I_D = 41 A, I_G = 1.0 mA	–	3.9	5	
Q_{gs}	Gate to Source Gate Charge	V_{DD} = 50 V, I_D = 41 A, I_G = 1.0 mA	–	12	–	
Q_{gs2}	Gate Charge Threshold to Plateau		–	8.0	–	
Q_{gd}	Gate to Drain “Miller” Charge		–	6.5	–	
RESISTIVE SWITCHING CHARACTERISTICS (V_{GS} = 10 V)						
$t_{(on)}$	Turn–On Time	V_{DD} = 50 V, I_D = 41 A, V_{GS} = 10 V, R_{GS} = 11.0 Ω	–	–	90	ns
$t_{d(on)}$	Turn–On Delay Time		–	12	–	
t_r	Rise Time		–	48	–	
$t_{d(off)}$	Turn–Off Delay Time		–	24	–	
t_f	Fall Time		–	27	–	
$t_{(off)}$	Turn–Off Time		–	–	77	
DRAIN–SOURCE DIODE CHARACTERISTICS						
V_{SD}	Source to Drain Diode Voltage	I_{SD} = 41 A	–	–	1.25	V
		I_{SD} = 21 A	–	–	1.0	
t_{rr}	Reverse Recovery Time	I_{SD} = 41 A, dI_{SD}/dt = 100 A/μs	–	–	39	ns
Q_{rr}	Reverse Recovered Charge	I_{SD} = 41 A, dI_{SD}/dt = 100 A/μs	–	–	42	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTES:
1. Starting T_J = 25°C, L = 0.11 mH, I_{AS} = 30 A.
2. Pulse Width = 100 s.

TYPICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

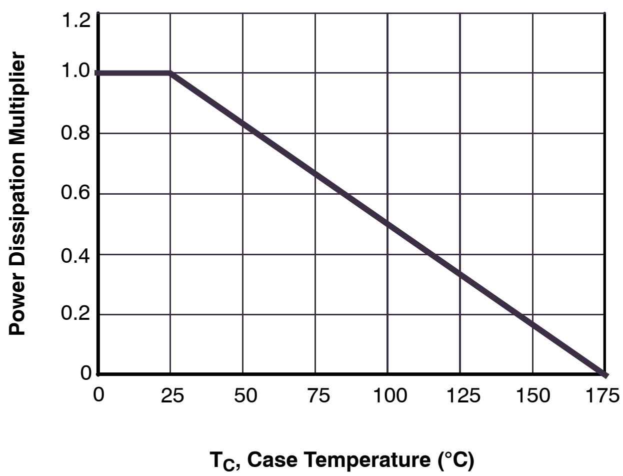


Figure 2. Normalized Power Dissipation vs Ambient Temperature

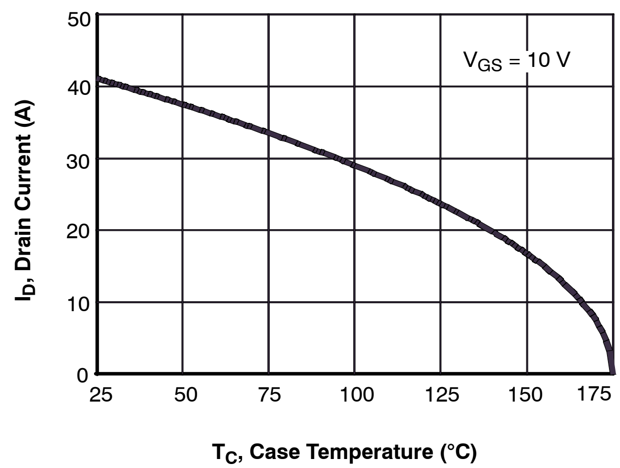


Figure 1. Maximum Continuous Drain Current vs Case Temperature

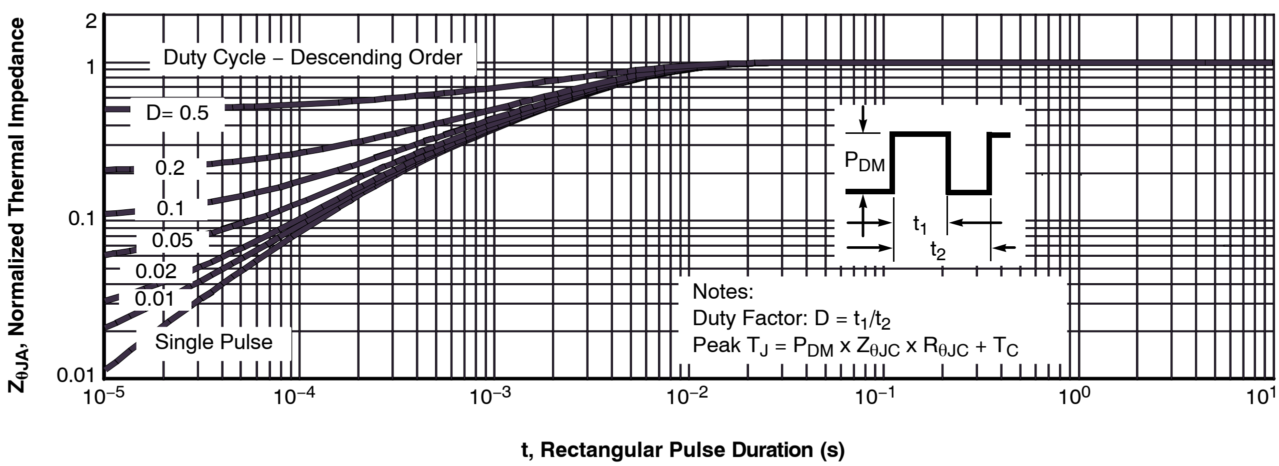


Figure 3. Normalized Maximum Transient Thermal Impedance

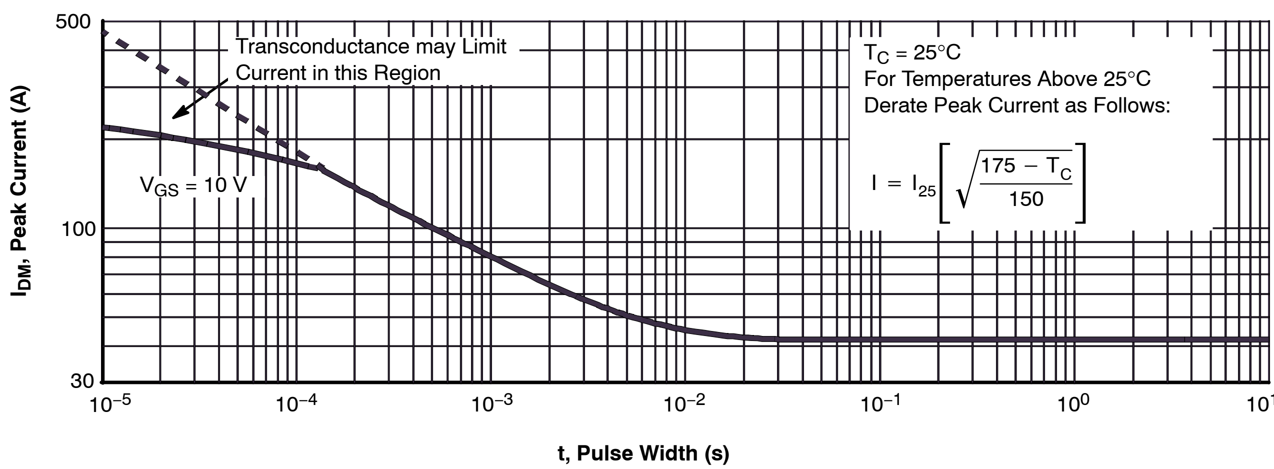


Figure 4. Peak Current Capability

TYPICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted) (continued)

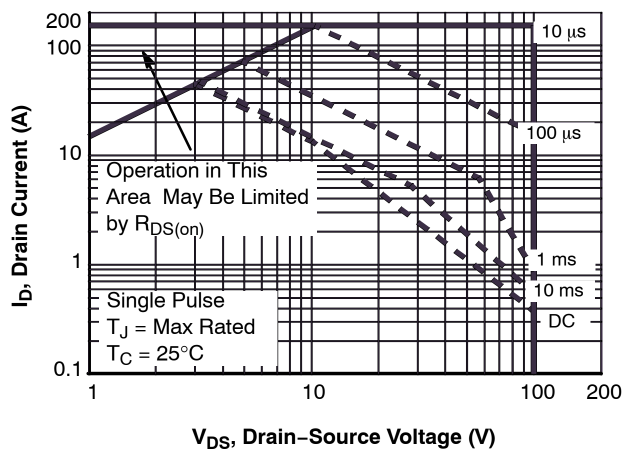
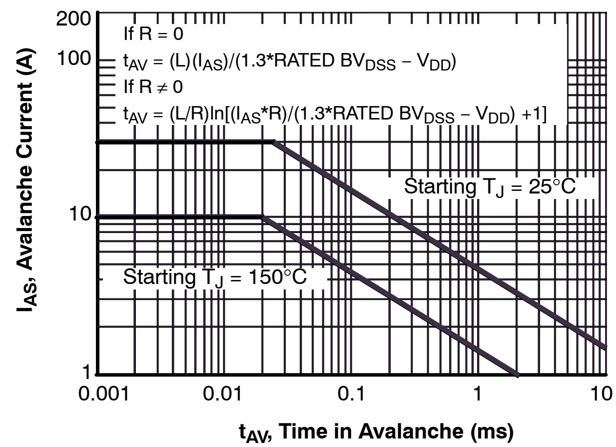


Figure 5. Forward Bias Safe Operating Area



NOTES: Refer to Application Notes AN7514 and AN7515

Figure 6. Unclamped Inductive Switching Capability

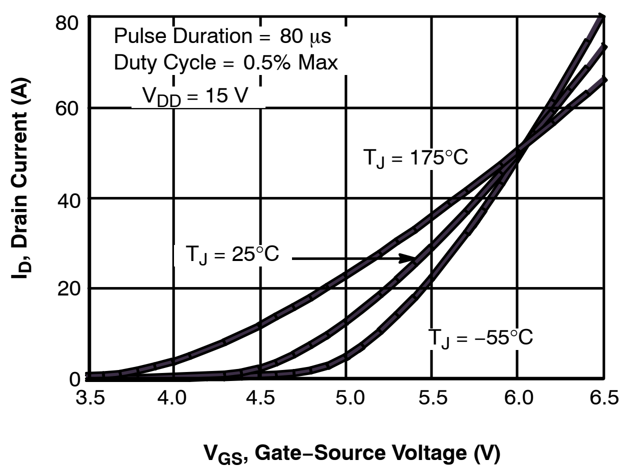


Figure 7. Transfer Characteristics

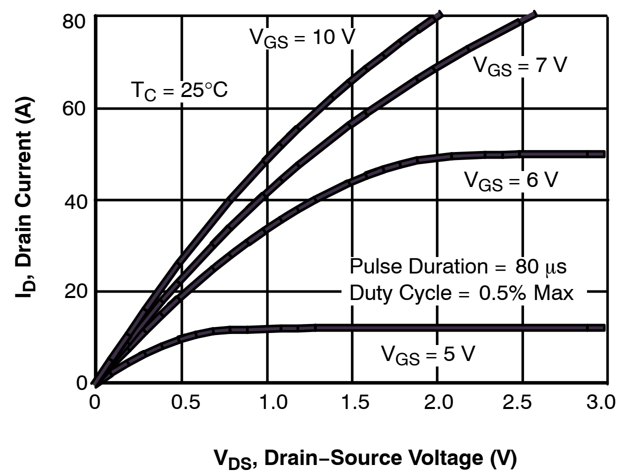


Figure 8. Saturation Characteristics

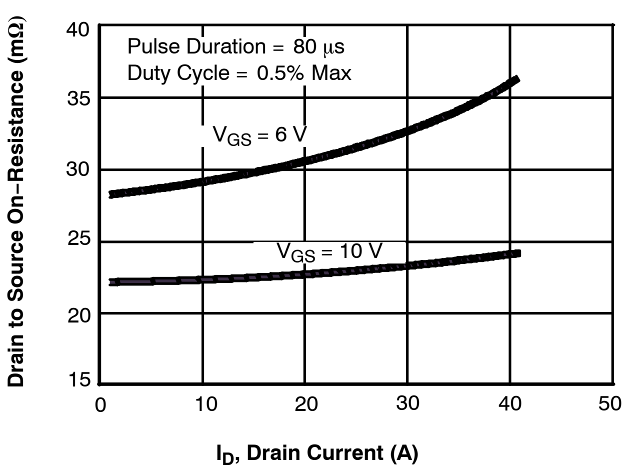


Figure 9. Drain to Source On Resistance vs Drain Current

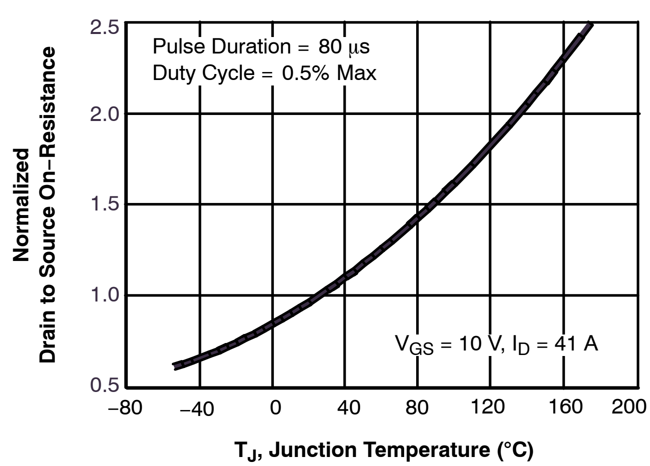


Figure 10. Normalized Drain to Source On Resistance vs Junction Temperature

TYPICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted) (continued)

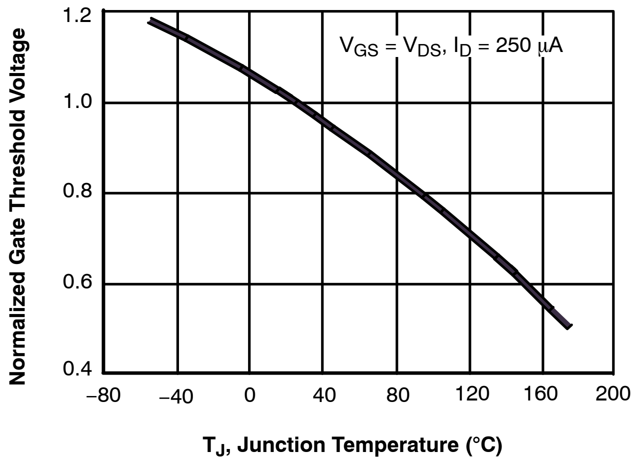


Figure 11. Normalized Gate Threshold Voltage vs Junction Temperature

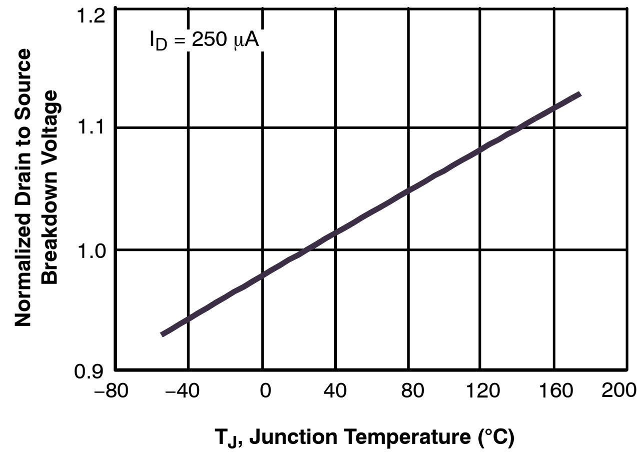


Figure 12. Normalized Drain to Source Breakdown Voltage vs Junction Temperature

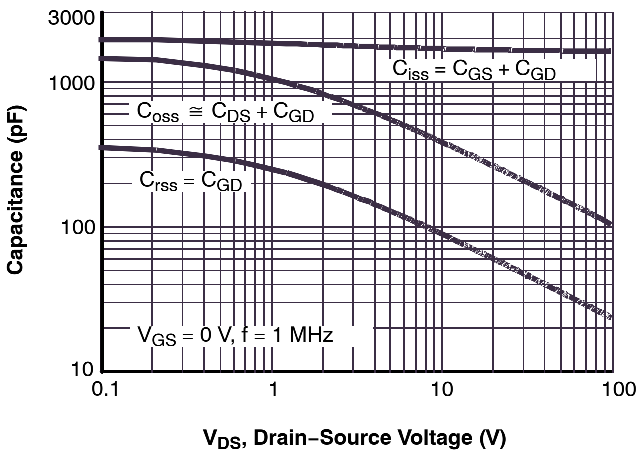


Figure 13. Capacitance vs Drain to Source Voltage

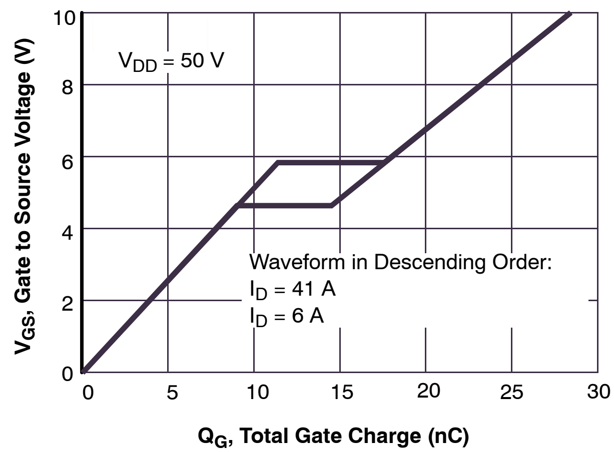


Figure 14. Gate Charge Waveforms for Constant Gate Currents

TEST CIRCUITS AND WAVEFORMS

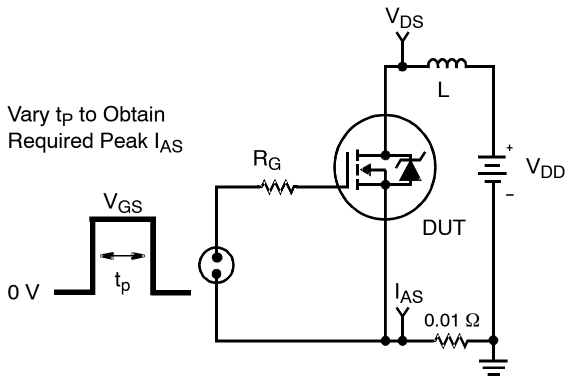


Figure 15. Unclamped Energy Test Circuit

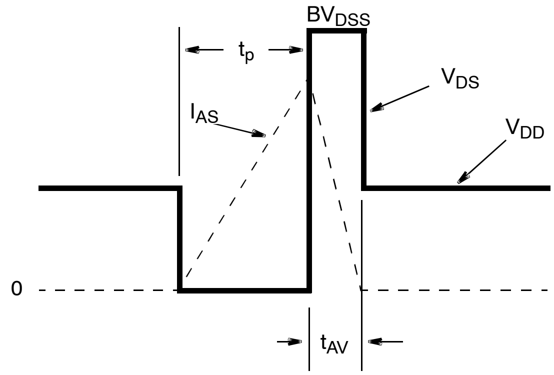


Figure 16. Unclamped Energy Waveforms

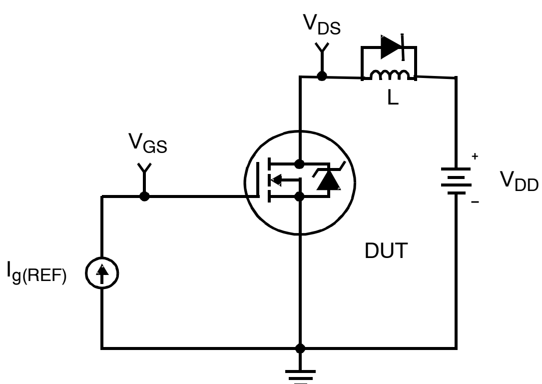


Figure 17. Gate Charge Test Circuit

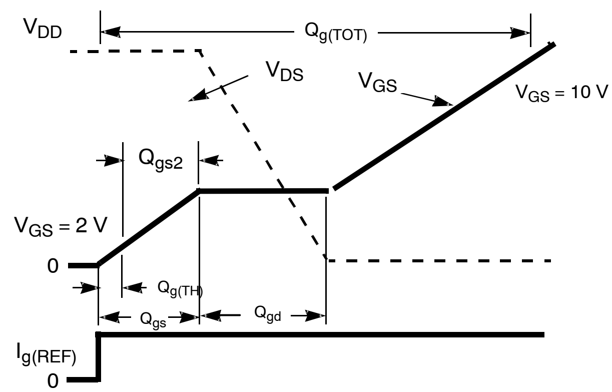


Figure 18. Gate Charge Waveforms

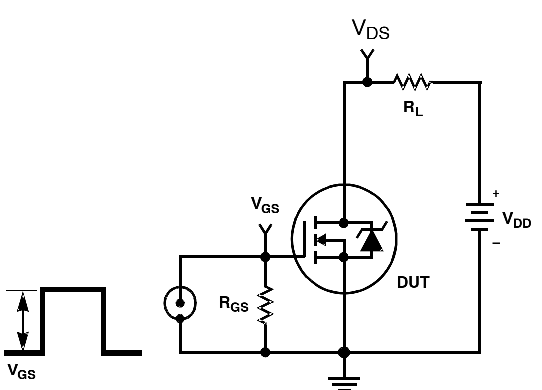


Figure 19. Switching Time Test Circuit

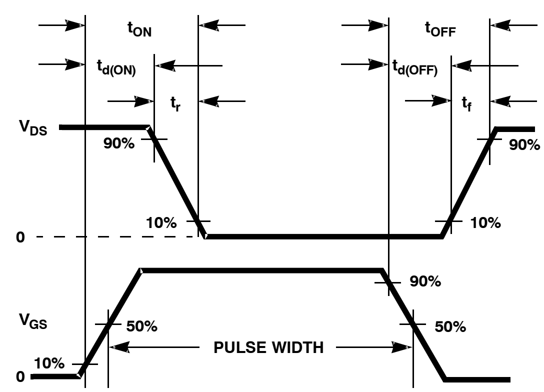
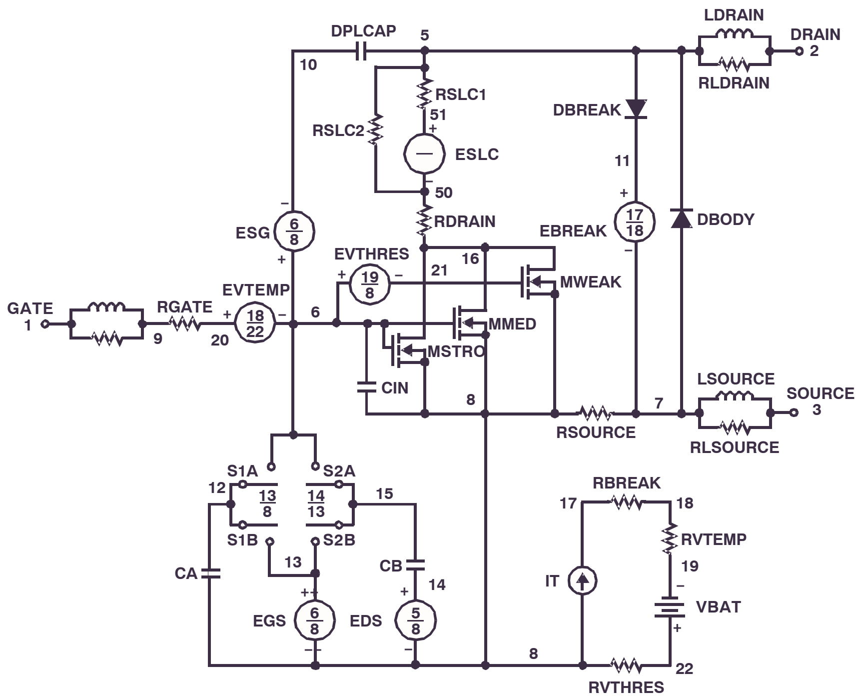


Figure 20. Switching Time Waveforms

PSPICE ELECTRICAL MODEL



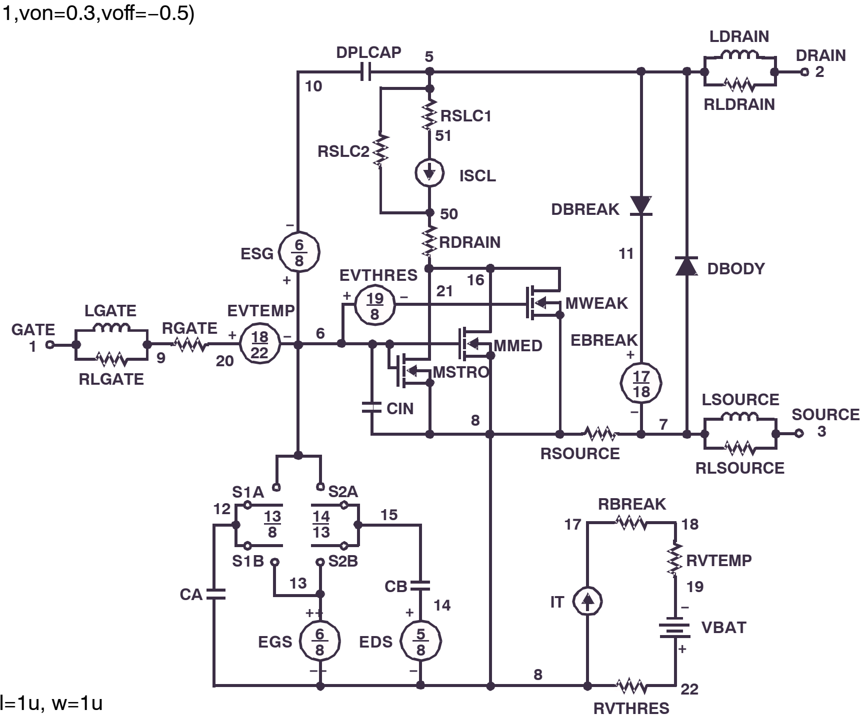

```
.SUBCKT FDP3672 2 1 3 ;      rev October 2002
Ca 12 8 5.8e–10
Cb 15 14 6.8e–10
Cin 6 8 1.6e–9

Dbody 7 5 DbodyMOD
Dbreak 5 11 DbreakMOD
Dplcap 10 5 DplcapMOD

Ebreak 11 7 17 18 105
Eds 14 8 5 8 1
Egs 13 8 6 8 1
Esg 6 10 6 8 1
Evthres 6 21 19 8 1
Evtemp 20 6 18 22 1

It 8 17 1

Lgate 1 9 9.56e–9
Ldrain 2 5 1.0e–9
Lsource 3 7 4.45e–9

RLgate 1 9 95.6
RLdrain 2 5 10
RLsource 3 7 44.5

Mmed 16 6 8 8 MmedMOD
Mstro 16 6 8 8 MstroMOD
MweakMOD 16 21 8 8 MweakMOD

Rbreak 17 18 RbreakMOD 1
Rdrain 50 16 RdrainMOD 6.0e–3
Rgate 9 20 1.5
RSLC1 5 51 RSLCMOD 1.0e–6
RSLC2 5 50 1.0e3
Rsource 8 7 RsourceMOD 9.5e–3
Rvthres 22 8 RvthresMOD 1
Rvtemp 18 19 RvtempMOD 1
S1a 6 12 13 8 S1AMOD
S1b 13 12 13 8 S1BMOD
S2a 6 15 14 13 S2AMOD
S2b 13 15 14 13 S2BMOD

Vbat 22 19 DC 1
ESLC 51 50 VALUE={(V(5,51)/ABS(V(5,51)))*(PWR(V(5,51)/(1e–6*98),3))}

.MODEL DbodyMOD D (IS=1.0E–11 N=1.05 RS=3.7e–3 TRS1=2.5e–3 TRS2=1.0e–6
+ CJO=1.2e–9 M=0.58 TT=3.75e–8 XTI=4.0)
.MODEL DbreakMOD D (RS=15 TRS1=4.0e–3 TRS2=–5.0e–6)
.MODEL DplcapMOD D (CJO=3.8e–10 IS=1.0e–30 N=10 M=0.60)

.MODEL MmedMOD NMOS (VTO=3.6 KP=3 IS=1e–40 N=10 TOX=1 L=1u W=1u RG=1.5)
.MODEL MstroMOD NMOS (VTO=4.3 KP=59 IS=1e–30 N=10 TOX=1 L=1u W=1u)
..MODEL MweakMOD NMOS (VTO=3.09 KP=0.05 IS=1e–30 N=10 TOX=1 L=1u W=1u RG=15 RS=0.1)

.MODEL RbreakMOD RES (TC1=9.0e–4 TC2=–1.0e–7)
.MODEL RdrainMOD RES (TC1=11.0e–3 TC2= 6.1e–5)
.MODEL RSLCMOD RES (TC1=3.0e–3 TC2=1.0e–6)
.MODEL RsourceMOD RES (TC1=4.0e–3 TC2=1.0e–6)
.MODEL RvthresMOD RES (TC1=–3.5e–3 TC2=–1.5e–5)
.MODEL RvtempMOD RES (TC1=–4.3e–3 TC2=1.5e–6)
```

```
.MODEL S1AMOD VSWITCH (RON=1e−5 ROFF=0.1 VON=−5.0 VOFF=−3.5)
.MODEL S1BMOD VSWITCH (RON=1e−5 ROFF=0.1 VON=−3.5 VOFF=−5.0)
.MODEL S2AMOD VSWITCH (RON=1e−5 ROFF=0.1 VON=−0.5 VOFF=0.3)
.MODEL S2BMOD VSWITCH (RON=1e−5 ROFF=0.1 VON=0.3 VOFF=−0.5)

.ENDS
```

For further discussion of the PSPICE model, consult *A New PSPICE Sub−Circuit for the Power MOSFET Featuring Global Temperature Options;* IEEE Power Electronics Specialist Conference Records, 1991, written by William J. Hepp and C. Frank Wheatley.

SABER ELECTRICAL MODEL

```
REV October 2002
template  FDP3672 n2,n1,n3
electrical n2,n1,n3
{
var i iscl
dp..model dbodymod = (isl=1.0e−11,nl=1.05,rs=3.7e−3,trs1=2.5e−3,trs2=1.0e−6,cjo=1.2e−9,
m=0.58,tt=3.75e−8, ti=4.0)
dp..model dbreakmod = (rs=15,trs1=4.0e−3,trs2=−5.0e−6)
dp..model dplcapmod = (cjo=3.8e−10,isl=10.0e−30,nl=10,m=0.60)
m..model mmedmod = (type=_n,vto=3.6,kp=3,is=1e−40, tox=1)
m..model mstrongmod = (type=_n,vto=4.3,kp=59,is=1e−30, tox=1)
m..model mweakmod = (type=_n,vto=3.09,kp=0.05,is=1e−30, tox=1,rs=0.1)
sw_vcsp..model s1amod = (ron=1e−5,roff=0.1,von=−5.0,voff=−3.5)
sw_vcsp..model s1bmod = (ron=1e−5,roff=0.1,von=−3.5,voff=−5.0)
sw_vcsp..model s2amod = (ron=1e−5,roff=0.1,von=−0.5,voff=0.3)
sw_vcsp..model s2bmod = (ron=1e−5,roff=0.1,von=0.3,voff=−0.5)
c.ca n12 n8 = 5.8e−10
c.cb n15 n14 = 6.8e−10
c.cin n6 n8 = 1.6e−9

dp.dbody n7 n5 = model=dbodymod
dp.dbreak n5 n11 = model=dbreakmod
dp.dplcap n10 n5 = model=dplcapmod

spe.ebreak n11 n7 n17 n18 = 105
spe.eds n14 n8 n5 n8 = 1
spe.egs n13 n8 n6 n8 = 1
spe.esg n6 n10 n6 n8 = 1
spe.evthres n6 n21 n19 n8 = 1
spe.evtemp n20 n6 n18 n22 = 1

i.it n8 n17 = 1

l.lgate n1 n9 = 95.6e−9
l.ldrain n2 n5 = 1.0e−9
l.lsource n3 n7 = 4.45e−9

res.rlgate n1 n9 = 9.56
res.rldrain n2 n5 = 10
res.rlsource n3 n7 = 44.5

m.mmed n16 n6 n8 n8 = model=mmedmod, l=1u, w=1u
m.mstrong n16 n6 n8 n8 = model=mstrongmod, l=1u, w=1u
m.mweak n16 n21 n8 n8 = model=mweakmod, l=1u, w=1u

res.rbreak n17 n18 = 1, tc1=9.0e−4,tc2=−1.0e−7
res.rdrain n50 n16 = 6.0e−3, tc1=11.0e−3,tc2=6.1e−5
res.rgate n9 n20 = 1.5
res.rslc1 n5 n51 = 1.0e−6, tc1=3.0e−3,tc2=1.0e−6
res.rslc2 n5 n50 = 1.0e3
res.rsource n8 n7 = 9.5e−3, tc1=4.0e−3,tc2=1.0e−6
res.rvthres n22 n8 = 1, tc1=−3.5e−3,tc2=−1.5e−5
res.rvtemp n18 n19 = 1, tc1=−4.3e−3,tc2=1.5e−6
sw_vcsp.s1a n6 n12 n13 n8 = model=s1amod
sw_vcsp.s1b n13 n12 n13 n8 = model=s1bmod
sw_vcsp.s2a n6 n15 n14 n13 = model=s2amod
sw_vcsp.s2b n13 n15 n14 n13 = model=s2bmod

v.vbat n22 n19 = dc=1
equations {
i (n51−>n50) +=iscl
iscl: v(n51,n50) = ((v(n5,n51)/(1e−9+abs(v(n5,n51))))*((abs(v(n5,n51)*1e6/98))** 3))
}
```



SPICE THERMAL MODEL

REV October 2002
FDP3672

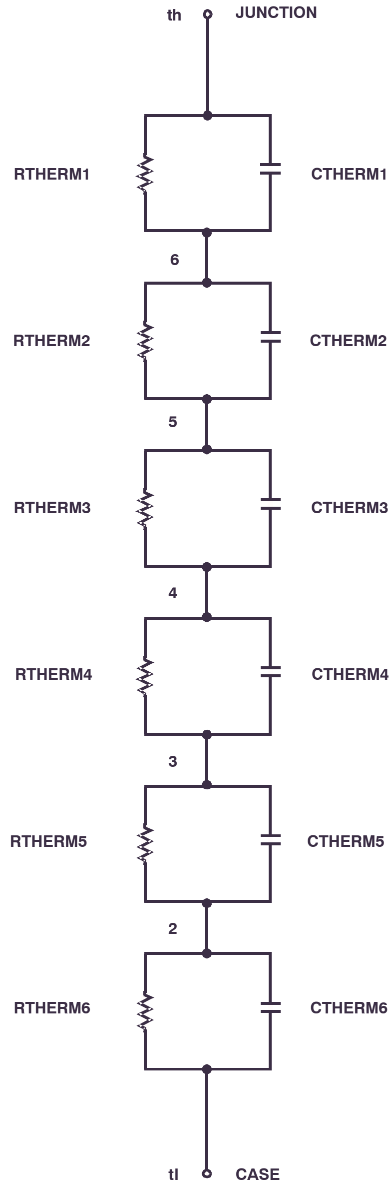
CTHERM1 TH 6 3.2e–3
CTHERM2 6 5 3.3e–3
CTHERM3 5 4 3.4e–3
CTHERM4 4 3 3.5e–3
CTHERM5 3 2 6.4e–3
CTHERM6 2 TL 1.9e–2

RTHERM1 TH 6 5.5e–4
RTHERM2 6 5 5.0e–3
RTHERM3 5 4 4.5e–2
RTHERM4 4 3 10.5e–2
RTHERM5 3 2 3.4e–1
RTHERM6 2 TL 3.5e–1

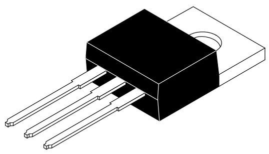
SABER THERMAL MODEL

SABER thermal model FDP3672
template thermal_model th tl
thermal_c th, tl
{
cctherm.ctherm1 th 6 =3.2e–3
ctherm.ctherm2 6 5 =3.3e–3
ctherm.ctherm3 5 4 =3.4e–3
ctherm.ctherm4 4 3 =3.5e–3
ctherm.ctherm5 3 2 =6.4e–3
ctherm.ctherm6 2 tl =1.9e–2

rtherm.rtherm1 th 6 =5.5e–4
rtherm.rtherm2 6 5 =5.0e–3
rtherm.rtherm3 5 4 =4.5e–2
rtherm.rtherm4 4 3 =10.5e–2
rtherm.rtherm5 3 2 =3.4e–1
rtherm.rtherm6 2 tl =3.5e–1
}



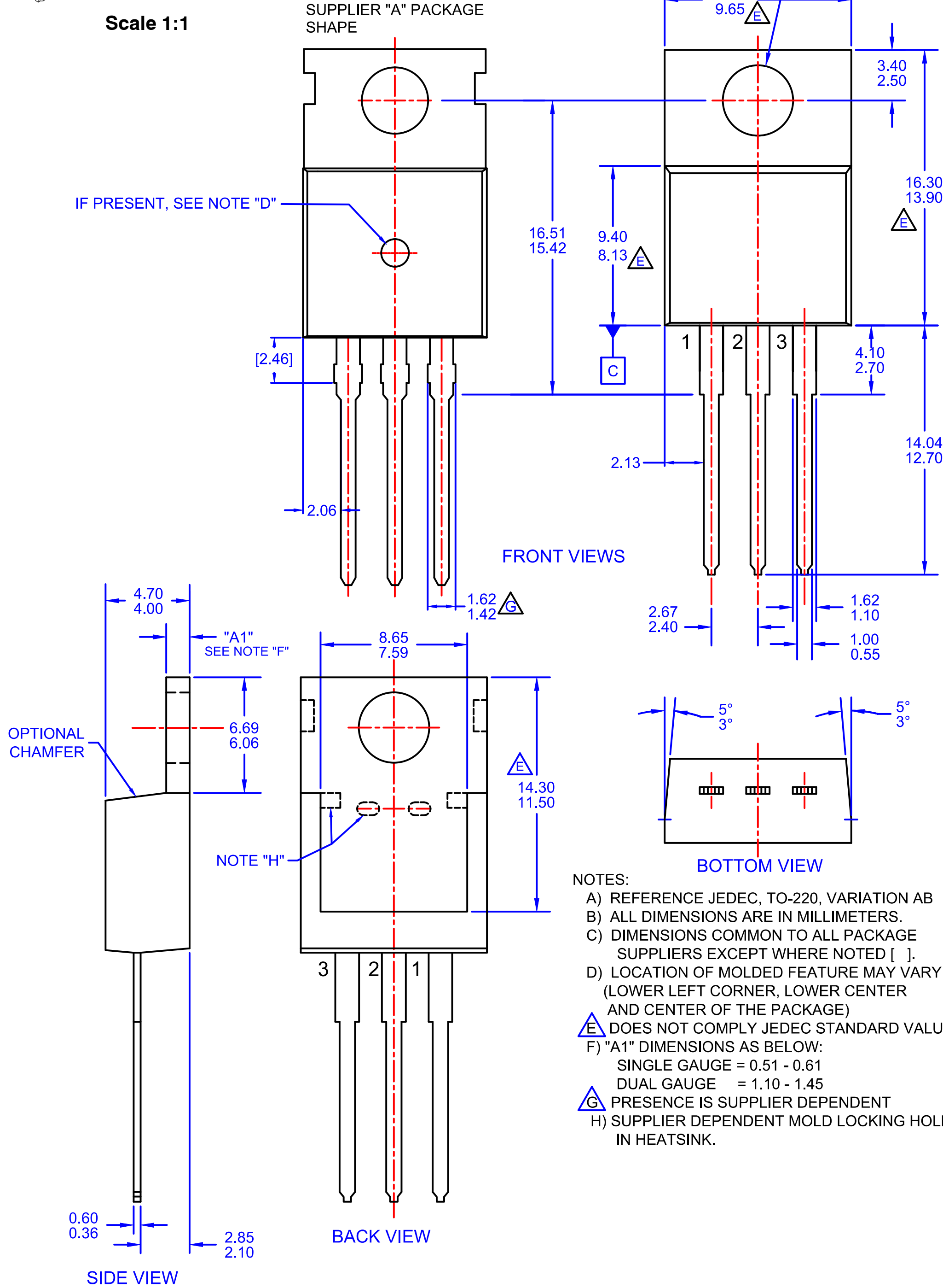
POWERTRENCH is a registered trademark of Semiconductor Components Industries, LLC dba “**onsemi**” or its affiliates and/or subsidiaries in the United States and/or other countries.



Scale 1:1

TO−220−3LD
CASE 340AT
ISSUE A

DATE 03 OCT 2017



NOTES:

A) REFERENCE JEDEC, TO-220, VARIATION AB
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS COMMON TO ALL PACKAGE SUPPLIERS EXCEPT WHERE NOTED [ ].
D) LOCATION OF MOLDED FEATURE MAY VARY (LOWER LEFT CORNER, LOWER CENTER AND CENTER OF THE PACKAGE)
E) DOES NOT COMPLY JEDEC STANDARD VALUE.
F) "A1" DIMENSIONS AS BELOW:
   SINGLE GAUGE = 0.51 - 0.61
   DUAL GAUGE = 1.10 - 1.45
G) PRESENCE IS SUPPLIER DEPENDENT
H) SUPPLIER DEPENDENT MOLD LOCKING HOLES IN HEATSINK.

DOCUMENT NUMBER:	**98AON13818G**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	**TO−220−3LD**	**PAGE 1 OF 1**

ON Semiconductor and ON are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. ON Semiconductor does not convey any license under its patent rights nor the rights of others.

onsemi, onsemi, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent−Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as−is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
Technical Library: www.onsemi.com/design/resources/technical−documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support
For additional information, please contact your local Sales Representative at www.onsemi.com/support/sales

◊