

MOSFET – Dual, N-Channel, Asymmetric, POWERTRENCH[®], Power Clip 25 V FDPC8016S

General Description

This device includes two specialized N-Channel MOSFETs in a dual package. The switch node has been internally connected to enable easy placement and routing of synchronous buck converters. The control MOSFET (Q1) and synchronous SyncFET[™] (Q2) have been designed to provide optimal power efficiency.

Features

Q1: N-Channel

- Max $R_{DS(on)}$ = 3.8 m Ω at V_{GS} = 10 V, I_D = 20 A
- Max $R_{DS(on)}$ = 4.7 m Ω at V_{GS} = 4.5 V, I_D = 18 A

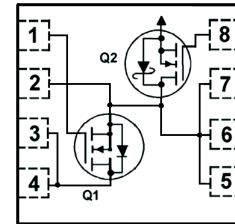
Q2: N-Channel

- Max $R_{DS(on)}$ = 1.4 m Ω at V_{GS} = 10 V, I_D = 35 A
- Max $R_{DS(on)}$ = 1.7 m Ω at V_{GS} = 4.5 V, I_D = 32 A
- Low Inductance Packaging Shortens Rise/Fall Times, Resulting in Lower Switching Losses
- MOSFET Integration Enables Optimum Layout for Lower Circuit Inductance and Reduced Switch Node Ringing
- These Devices are Pb-Free and are RoHS Compliant

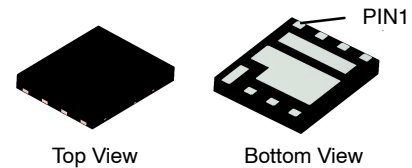
Applications

- Computing
- Communications
- General Purpose Point of Load

ELECTRICAL CONNECTION

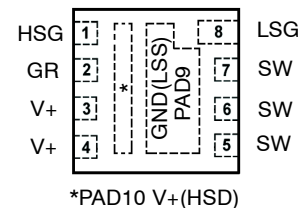


N-Channel MOSFET

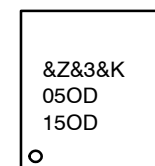


PQFN8 5.00x6.00x0.75, 1.27P
(Power Clip 56)
CASE 483AR

PIN ASSIGNMENT



MARKING DIAGRAM



&Z	= Assembly Plant Code
&3	= Numeric Date Code
&K	= Lot Code
05OD 15OD	= Specific Device Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

FDPC8016S

PINOUT DESCRIPTION

Pin	Name	Description	Pin	Name	Description	Pin	Name	Description
1	HSG	High Side Gate	3, 4, 10	V+(HSD)	High Side Drain	8	LSG	Low Side Gate
2	GR	Gate Return	5, 6, 7	SW	Switching Node, Low Side Drain	9	GND(LSS)	Low Side Source

MOSFET MAXIMUM RATINGS (T_A = 25°C, Unless otherwise specified)

Symbol	Parameter	Q1	Q2	Unit
V _{DS}	Drain to Source Voltage	25 (Note 5)	25 (Note 5)	V
V _{GS}	Gate to Source Voltage	±12	±12	V
I _D	Drain Current Continuous (T _C = 25°C) Continuous (T _A = 25°C) Pulsed (T _A = 25°C) (Note 4)	60 20 (Note 1a) 75	100 35 (Note 1b) 140	A
E _{AS}	Single Pulsed Avalanche Energy (Note 3)	73	216	mJ
P _D	Power Dissipation for Single Operation (T _C = 25°C) (T _A = 25°C)	21 2.1 (Note 1a)	42 2.3 (Note 1b)	W
T _J , T _{STG}	Operating and Storage Junction Temperature Range	-55 to +150		°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

Symbol	Parameter	Q1	Q2	Unit
R _{θJC}	Thermal Resistance, Junction to Case	6.0	3.0	°C/W
R _{θJA}	Thermal Resistance, Junction to Ambient	60 (Note 1a)	55 (Note 1b)	°C/W
R _{θJA}	Thermal Resistance, Junction to Ambient	130 (Note 1c)	120 (Note 1d)	°C/W

PACKAGE MARKING AND ORDERING INFORMATION

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
05OD/15OD	FDPC8016S	PQFN8	13"	12 mm	3,000 Units

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

BV _{DSS}	Drain to Source Breakdown Voltage	I _D = 250 μA, V _{GS} = 0 V I _D = 1 mA, V _{GS} = 0 V	Q1 Q2	25 25	– –	– –	V
ΔBV _{DSS} /ΔT _J	Breakdown Voltage Temperature Coefficient	I _D = 250 μA, referenced to 25°C I _D = 10 mA, referenced to 25°C	Q1 Q2	– –	24 28	– –	mV/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 20 V, V _{GS} = 0 V V _{DS} = 20 V, V _{GS} = 0 V	Q1 Q2	– –	– –	1 500	μA
I _{GSS}	Gate to Source Leakage Current, Forward	V _{GS} = 12 V / –8 V, V _{DS} = 0 V V _{GS} = 12 V / –8 V, V _{DS} = 0 V	Q1 Q2	– –	– –	±100 ±100	nA nA

ON CHARACTERISTICS

V _{GS(th)}	Gate to Source Threshold Voltage	V _{GS} = V _{DS} , I _D = 250 μA V _{GS} = V _{DS} , I _D = 1 mA	Q1 Q2	0.8 1.0	1.3 1.5	2.5 2.5	V
ΔV _{GS(th)} /ΔT _J	Gate to Source Threshold Voltage Temperature Coefficient	I _D = 250 μA, referenced to 25°C I _D = 10 mA, referenced to 25°C	Q1 Q2	– –	–4 –3	– –	mV/°C

FDPC8016S

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Unit
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ON CHARACTERISTICS

R _{DS(on)}	Drain to Source On Resistance	V _{GS} = 10 V, I _D = 20 A V _{GS} = 4.5 V, I _D = 18 A V _{GS} = 10 V, I _D = 20 A, T _J = 125°C	Q1	–	2.8	3.8	mΩ
		V _{GS} = 10 V, I _D = 35 A V _{GS} = 4.5 V, I _D = 32 A V _{GS} = 10 V, I _D = 35 A, T _J = 125°C	Q2	–	1.1	1.4	
g _{FS}	Forward Transconductance	V _{DS} = 5 V, I _D = 20 A	Q1	–	182	–	S
		V _{DS} = 5 V, I _D = 35 A	Q2	–	241	–	

DYNAMIC CHARACTERISTICS

C _{iss}	Input Capacitance	Q1: V _{DS} = 13 V, V _{GS} = 0 V, f = 1 MHz Q2: V _{DS} = 13 V, V _{GS} = 0 V, f = 1 MHz	Q1	–	1695	2375	pF
C _{oss}	Output Capacitance		Q2	–	4715	6600	
C _{rss}	Reverse Transfer Capacitance		Q1	–	495	710	pF
			Q2	–	1195	1675	
R _g	Gate Resistance		Q1	0.1	0.4	1.2	Ω
			Q2	0.1	0.5	1.5	

SWITCHING CHARACTERISTICS

t _{d(on)}	Turn-On Delay Time	Q1: V _{DD} = 13 V, I _D = 20 A, R _{GEN} = 6 Ω Q2: V _{DD} = 13 V, I _D = 35 A, R _{GEN} = 6 Ω	Q1	–	8	16	ns
t _r	Rise Time		Q2	–	13	24	
t _{d(off)}	Turn-Off Delay Time		Q1	–	2	10	ns
t _f	Fall Time		Q2	–	4	10	
Q _g	Total Gate Charge	V _{GS} = 0 V to 10 V Q1: V _{DD} = 13 V, I _D = 20 A Q2: V _{DD} = 13 V, I _D = 35 A	Q1	–	25	35	nC
			Q2	–	67	94	
Q _g	Total Gate Charge	V _{GS} = 0 V to 4.5 V Q1: V _{DD} = 13 V, I _D = 20 A Q2: V _{DD} = 13 V, I _D = 35 A	Q1	–	11	16	nC
			Q2	–	31	44	
Q _{gs}	Gate to Source Gate Charge	Q1: V _{DD} = 13 V, I _D = 20 A Q2: V _{DD} = 13 V, I _D = 35 A	Q1	–	3.4	–	nC
			Q2	–	10	–	
Q _{gd}	Gate to Drain “Miller” Charge	Q1: V _{DD} = 13 V, I _D = 20 A Q2: V _{DD} = 13 V, I _D = 35 A	Q1	–	2.2	–	nC
			Q2	–	6.3	–	

DRAIN-SOURCE DIODE CHARACTERISTICS

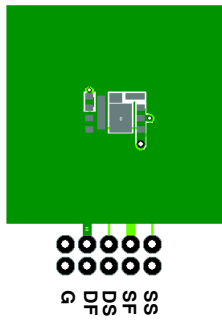
V _{SD}	Source to Drain Diode Forward Voltage	V _{GS} = 0 V, I _S = 20 A V _{GS} = 0 V, I _S = 35 A (Note 2)	Q1	–	0.8	1.2	V
t _{rr}	Reverse Recovery Time	Q1: I _F = 20 A, di/dt = 100 A/μs Q2: I _F = 35 A, di/dt = 200 A/μs	Q1	–	25	40	
Q _{rr}	Reverse Recovery Charge		Q2	–	33	53	nC
			Q1	–	10	20	
			Q2	–	31	50	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

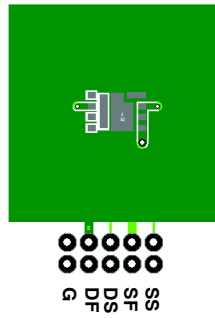
NOTES:

1. R_{θJA} is determined with the device mounted on a 1 in² pad 2 oz copper pad on a 1.5 × 1.5 in. board of FR-4 material. R_{θCA} is determined by the user's board design.

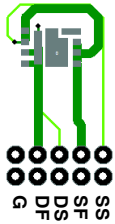
FDPC8016S



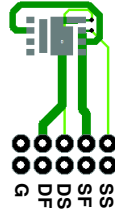
a) 60°C/W when mounted on a 1 in² pad of 2 oz copper.



b) 55°C/W when mounted on a 1 in² pad of 2 oz copper.



c) 130°C/W when mounted on a minimum pad of 2 oz copper.



d) 120°C/W when mounted on a minimum pad of 2 oz copper.

2. Pulse Test: Pulse Width < 300 μ s, Duty cycle < 2.0%.

3. Q1:

E_{AS} of 73 mJ is based on starting $T_J = 25^\circ\text{C}$; N-ch: $L = 3$ mH, $I_{AS} = 7$ A, $V_{DD} = 30$ V, $V_{GS} = 10$ V, 100% tested at $L = 0.1$ mH, $I_{AS} = 24$ A.

Q2:

E_{AS} of 216 mJ is based on starting $T_J = 25^\circ\text{C}$; N-ch: $L = 3$ mH, $I_{AS} = 12$ A, $V_{DD} = 25$ V, $V_{GS} = 10$ V, 100% tested at $L = 0.1$ mH, $I_{AS} = 39$ A.

4. Pulsed I_d limited by junction temperature, $t_d \leq 10$ μ s. Please refer to SOA curve for more details.

5. The continuous V_{DS} rating is 25 V; However, a pulse of 30 V peak voltage for no longer than 100 ns duration at 600 KHz frequency can be applied.

TYPICAL CHARACTERISTICS (Q1 N-CHANNEL)

($T_J = 25^\circ\text{C}$ unless otherwise noted)

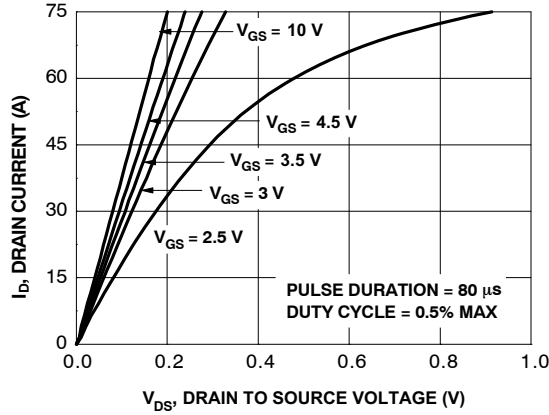


Figure 1. On-Region Characteristics

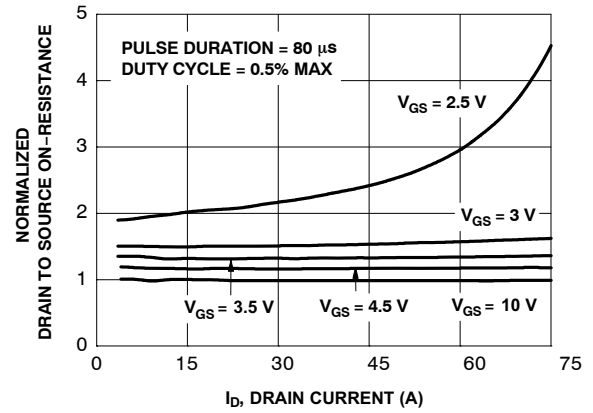


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

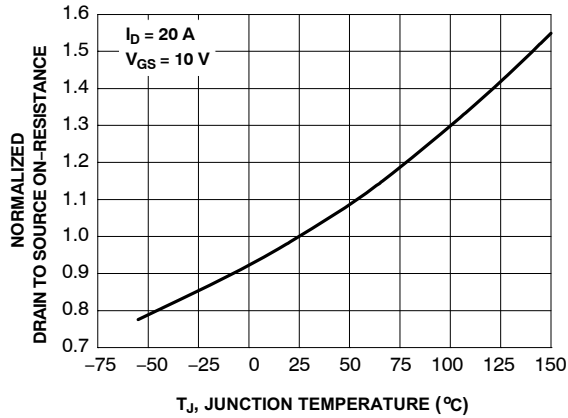


Figure 3. Normalized On-Resistance vs. Junction Temperature

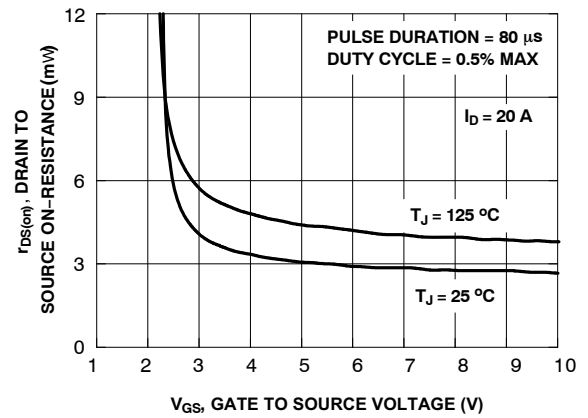


Figure 4. On-Resistance vs. Gate to Source Voltage

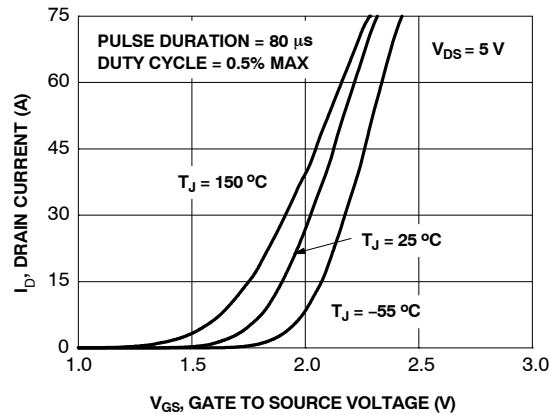


Figure 5. Transfer Characteristics

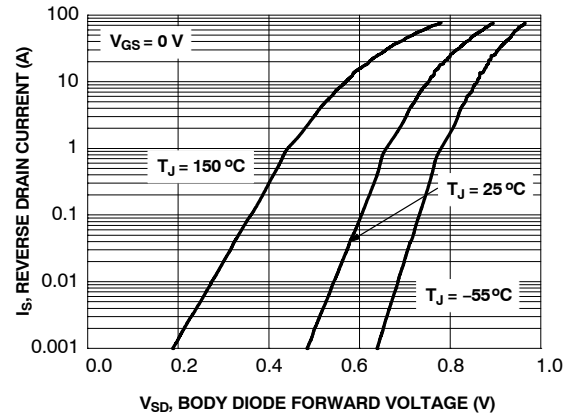


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

TYPICAL CHARACTERISTICS (Q1 N-CHANNEL)

($T_J = 25^\circ\text{C}$ unless otherwise noted)

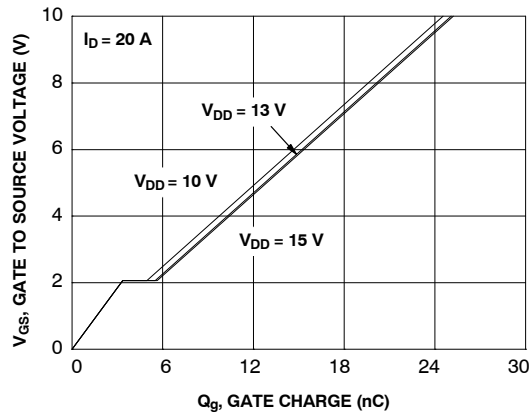


Figure 7. Gate Charge Characteristics

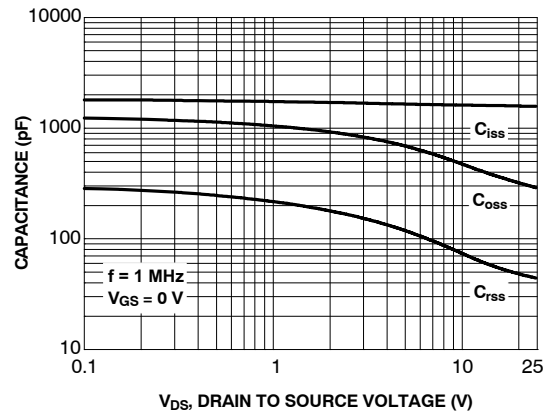


Figure 8. Capacitance vs. Drain to Source Voltage

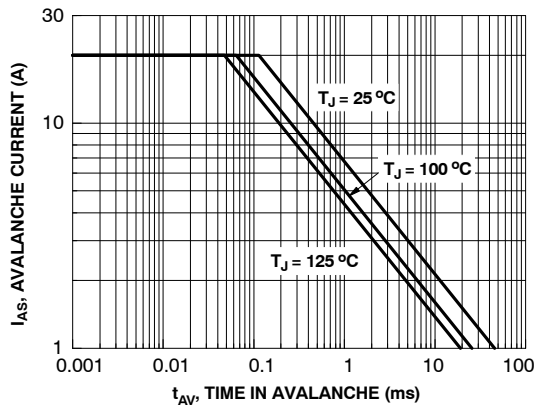


Figure 9. Unclamped Inductive Switching Capability

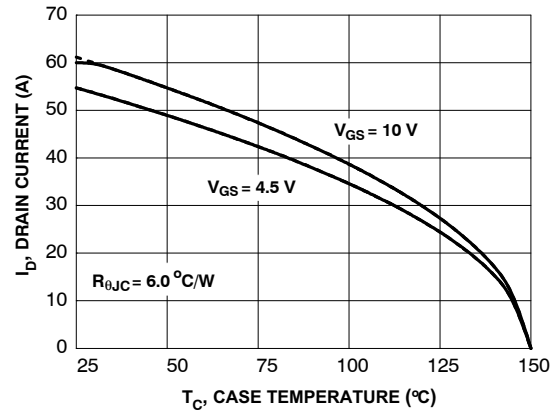


Figure 10. Maximum Continuous Drain Current vs. Case Temperature

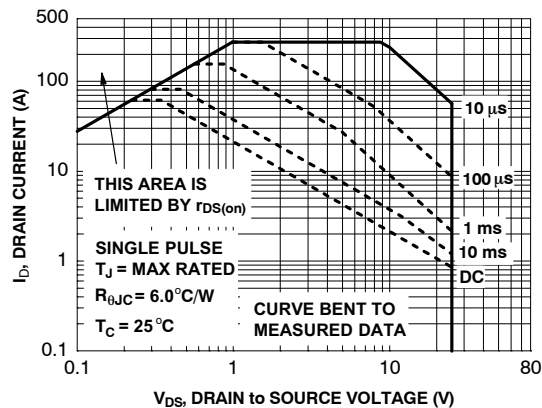


Figure 11. Forward Bias Safe Operating Area

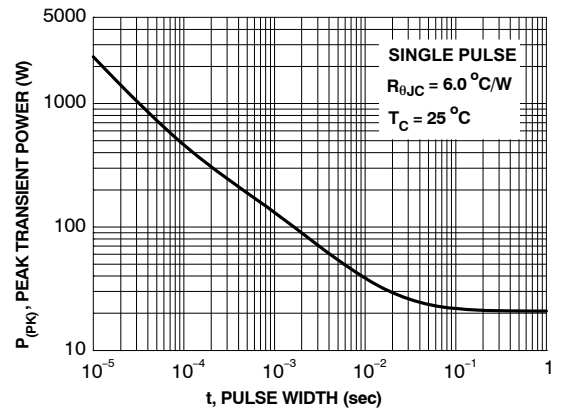


Figure 12. Single Pulse Maximum Power Dissipation

TYPICAL CHARACTERISTICS (Q1 N-CHANNEL)

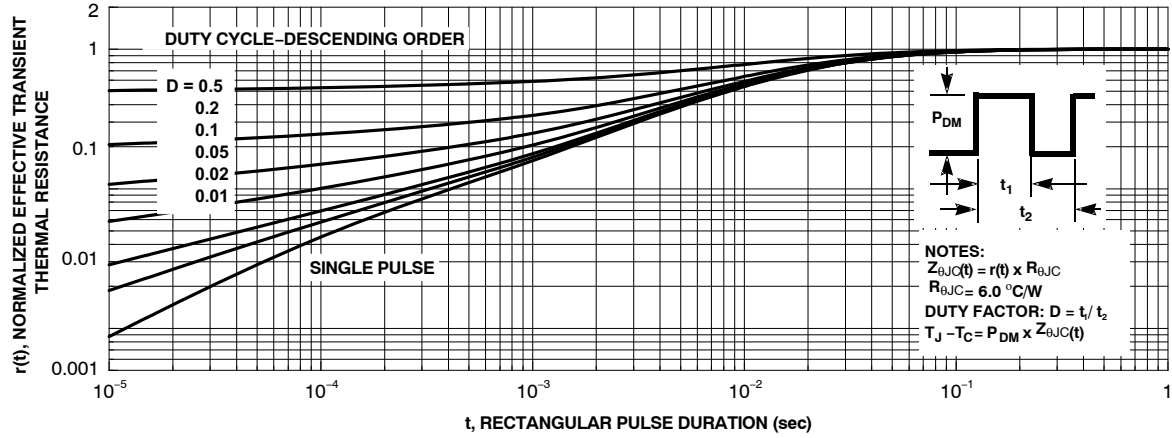
(T_J = 25°C unless otherwise noted)

Figure 13. Junction-to-Case Transient Thermal Response Curve

TYPICAL CHARACTERISTICS (Q2 N-CHANNEL)

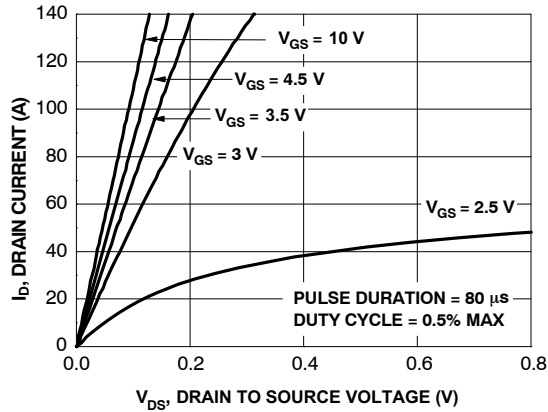
(T_J = 25°C unless otherwise noted)

Figure 14. On-Region Characteristics

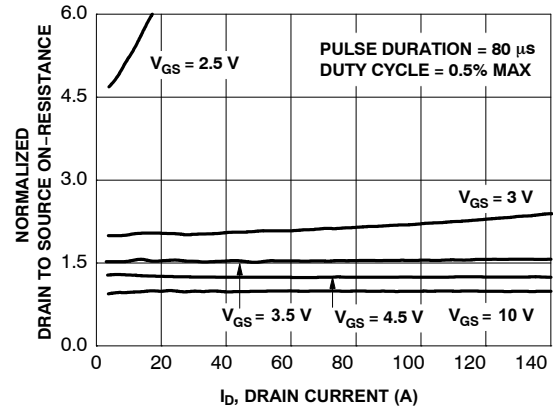


Figure 15. Normalized On-Resistance vs. Drain Current and Gate Voltage

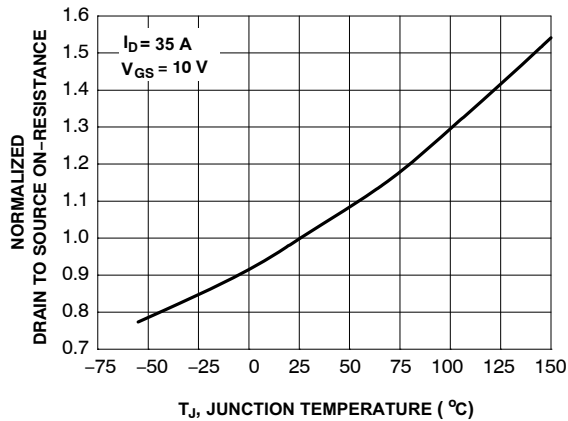


Figure 16. Normalized On-Resistance vs. Junction Temperature

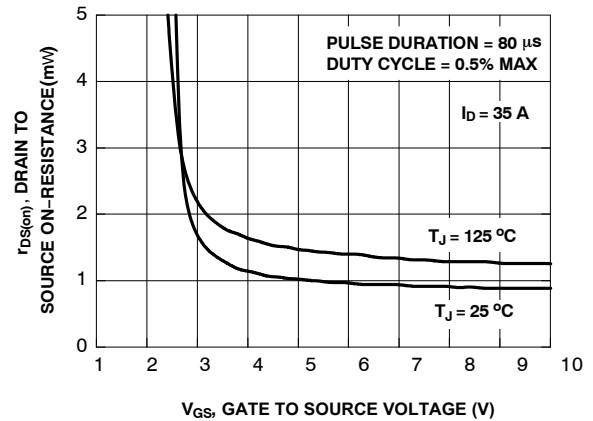


Figure 17. On-Resistance vs. Gate to Source Voltage

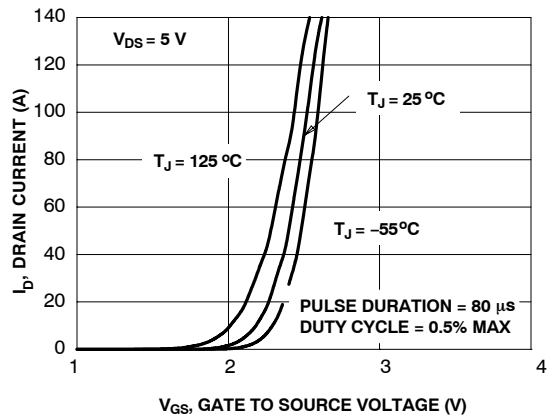


Figure 18. Transfer Characteristics

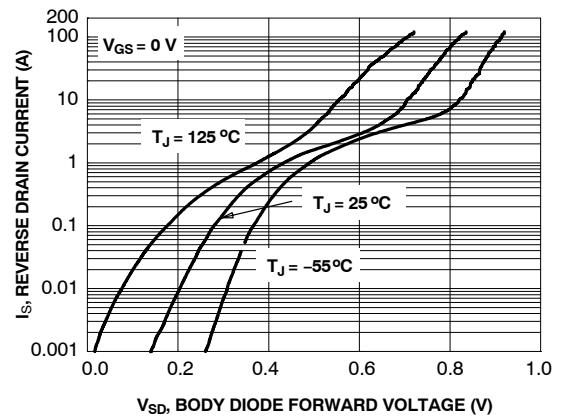


Figure 19. Source to Drain Diode Forward Voltage vs. Source Current

TYPICAL CHARACTERISTICS (Q2 N-CHANNEL)

($T_J = 25^\circ\text{C}$ unless otherwise noted)

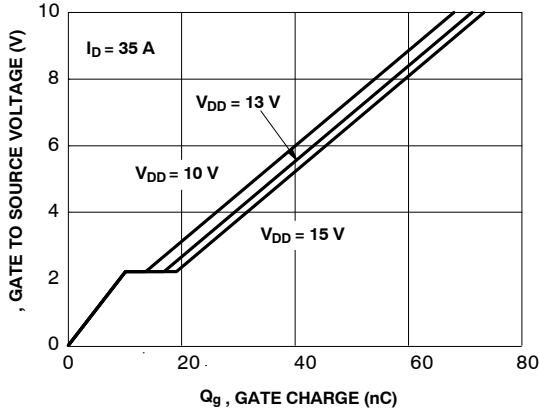


Figure 20. Gate Charge Characteristics

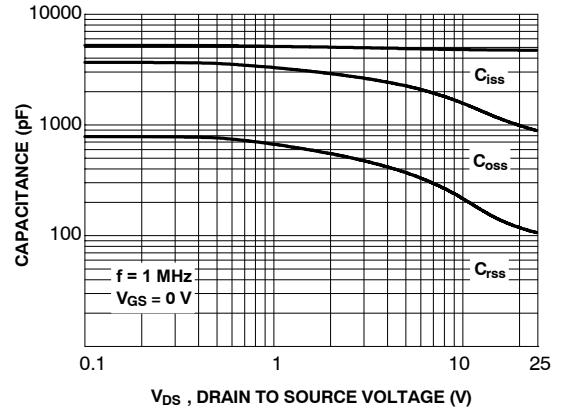


Figure 21. Capacitance vs. Drain to Source Voltage

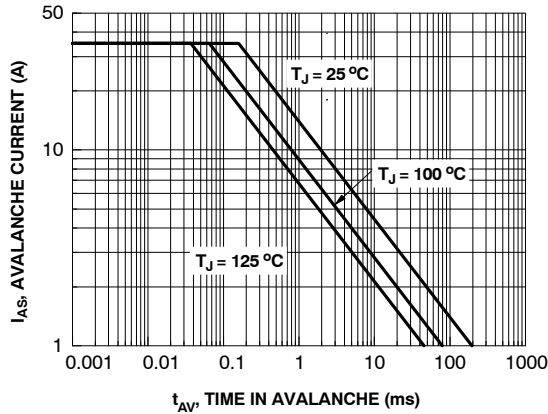


Figure 22. Unclamped Inductive Switching Capability

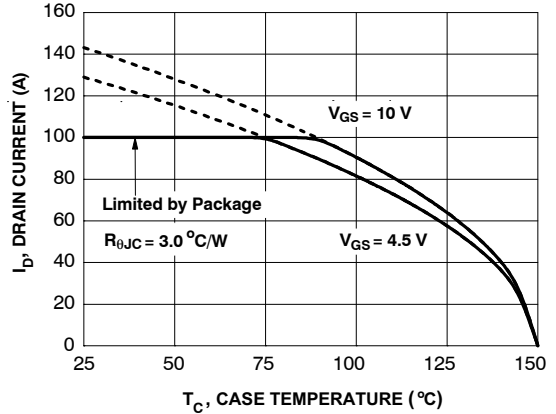


Figure 23. Maximum Continuous Drain Current vs. Case Temperature

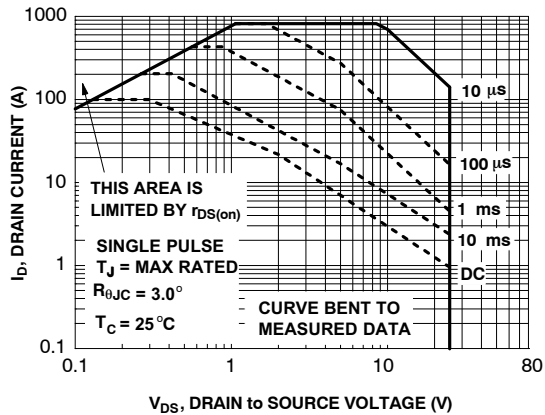


Figure 24. Forward Bias Safe Operating Area

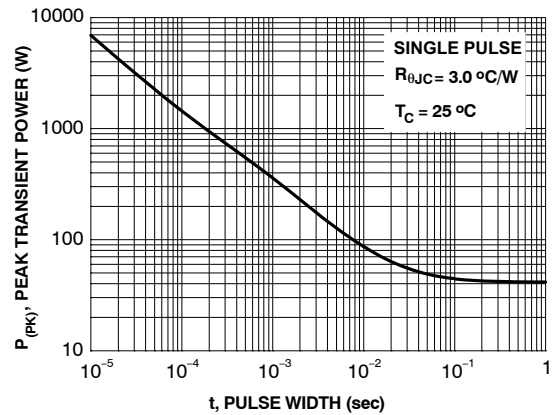


Figure 25. Single Pulse Maximum Power Dissipation

TYPICAL CHARACTERISTICS (Q2 N-CHANNEL)

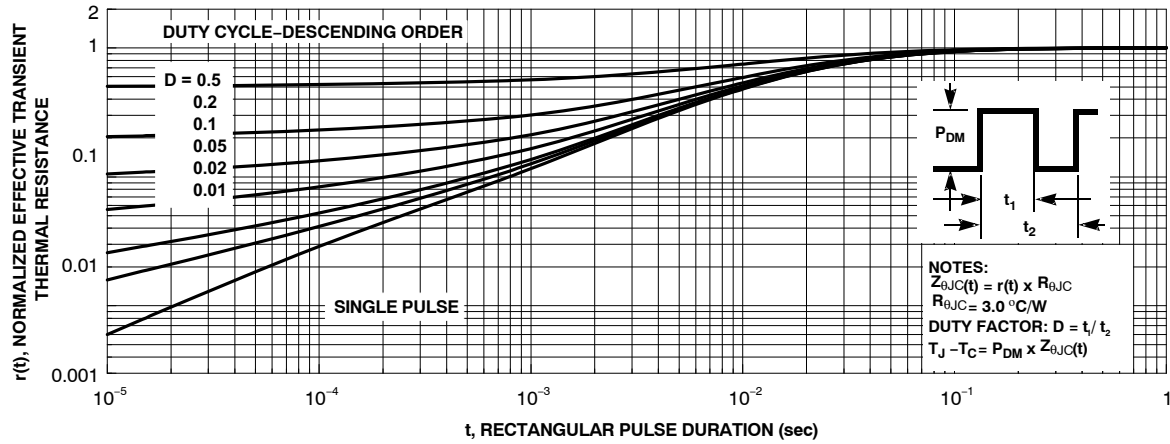
(T_J = 25°C unless otherwise noted)

Figure 26. Junction-to-Case Transient Thermal Response Curve

TYPICAL CHARACTERISTICS (continued)

SyncFET Schottky Body Diode Characteristics

ON's SyncFET process embeds a Schottky diode in parallel with PowerTrench MOSFET. This diode exhibits similar characteristics to a discrete external Schottky diode in parallel with a MOSFET. Figure 27 shows the reverse recovery characteristic of the FDPC8016S.

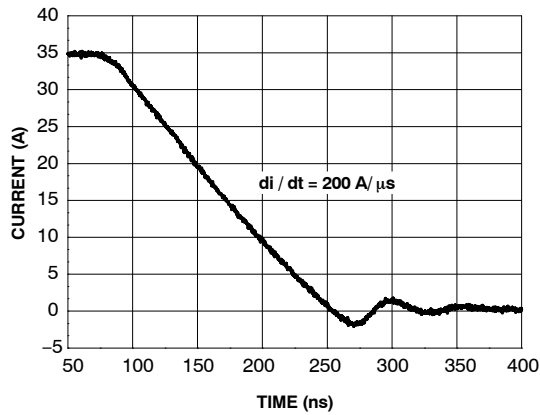


Figure 27. FDPC8016S SyncFET Body Diode Reverse Recovery Characteristic

Schottky barrier diodes exhibit significant leakage at high temperature and high reverse voltage. This will increase the power in the device.

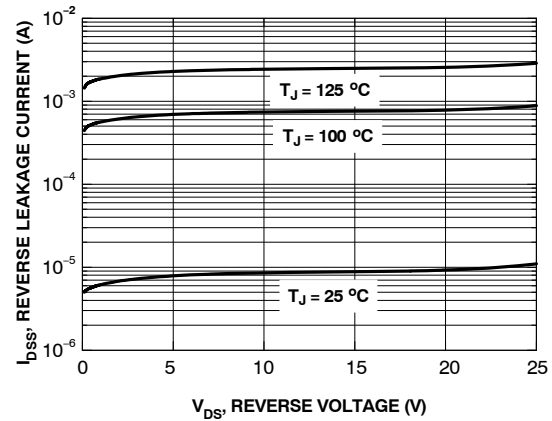
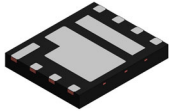
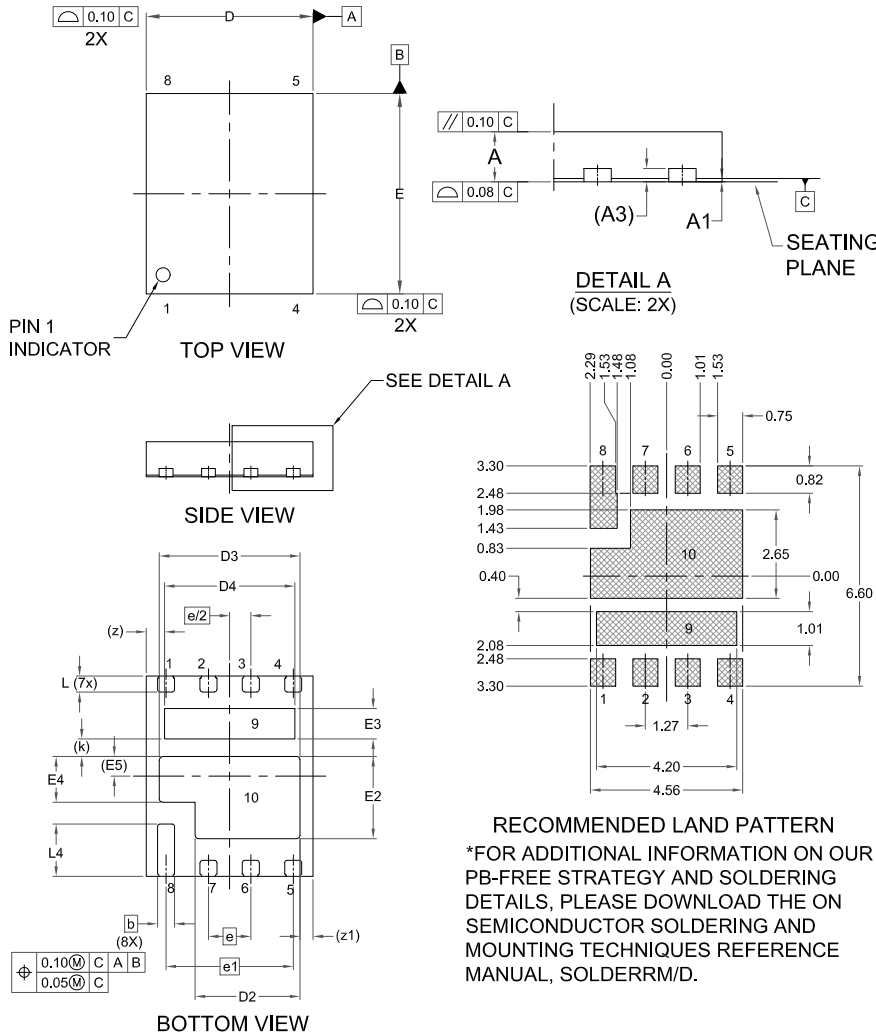


Figure 28. SyncFET Body Diode Reverse Leakage vs. Drain-Source Voltage



PQFN8 5.00x6.00x0.75, 1.27P
CASE 483AR
ISSUE D

DATE 06 NOV 2023



NOTES: UNLESS OTHERWISE SPECIFIED

- A) DOES NOT FULLY CONFORM TO JEDEC REGISTRATION, MO-229, DATED 11/2001.
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.
- D) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.00	-	0.05
A3	0.20 REF		
b	0.51 BSC		
D	4.90	5.00	5.10
D2	3.05	3.15	3.25
D3	4.12	4.22	4.32
D4	3.80	3.90	4.00
E	5.90	6.00	6.10
E2	2.36	2.46	2.56
E3	0.81	0.91	1.01
E4	1.27	1.37	1.47
E5	0.59 REF		
e	1.27 BSC		
e/2	0.635 BSC		
e1	3.81 BSC		
k	0.52 REF		
L	0.38	0.48	0.58
L4	1.47	1.57	1.67
z	0.55 REF		
z1	0.39 REF		

DOCUMENT NUMBER: 98AON13666G

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