

MOSFET – N-Channel, POWERTRENCH®

100 V, 67 A, 8.5 mΩ

FDPF045N10A

Description

This N-Channel MOSFET is Produced using onsemi’s advanced PowerTrench Process that has been tailored to minimize the on-state resistance while maintaining superior switching performance.

Features

- $R_{DS(on)} = 3.7\text{ m}\Omega$ (Typ.) @ $V_{GS} = 10\text{ V}$, $I_D = 67\text{ A}$
- Fast Switching Speed
- Low Gate Charge, $Q_g = 57\text{ nC}$ (Typ.)
- High Performance Trench Technology for Extremely Low $R_{DS(on)}$
- High Power and Current Handling Capability
- This Device is Pb-Free Halide, Free and RoHS Compliant

Applications

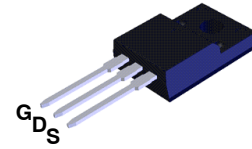
- Synchronous Rectification for ATX / Sever / Telecom PSU
- Motor Drives and Uninterruptible Power Supplies
- Micro Solar Inverter

ABSOLUTE MAXIMUM RATINGS

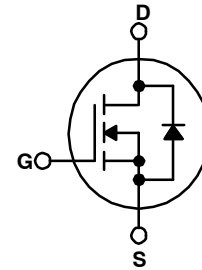
($T_C = 25^\circ\text{C}$ unless otherwise noted.)

Symbol	Parameter	Value	Unit
V_{DSS}	Drain to Source Voltage	100	V
V_{GSS}	Gate to Source Voltage	± 20	V
I_D	Drain Current – Continuous ($T_C = 25^\circ\text{C}$) – Continuous ($T_C = 100^\circ\text{C}$)	67 47	A
I_{DM}	Drain Current – Pulsed (Note 1)	268	A
E_{AS}	Single Pulsed Avalanche Energy (Note 2)	637	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	6.0	V/ns
P_D	Power Dissipation – ($T_C = 25^\circ\text{C}$) – Derate Above 25°C	43 0.29	W W/ $^\circ\text{C}$
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to $+175$	$^\circ\text{C}$
T_L	Maximum Lead Temperature for Soldering Purpose, 1/8" from Case for 5 Seconds	300	$^\circ\text{C}$

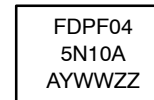
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.



TO-220F
CASE 221AT



MARKING DIAGRAM



FDPF045N10A = Specific Device Code
A = Assembly Location
YWW = Date Code (Year and Week)
ZZ = Assembly Lot Code

ORDERING INFORMATION

Device	Package	Shipping
FDPF045N10A	TO-220-3 FullPack	1000 Units / Tube

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

FDPF045N10A

THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	3.5	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max.	62.5	

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Off Characteristics						
BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 250 \mu A, V_{GS} = 0 V$	100	–	–	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250 \mu A$, Referenced to 25°C	–	0.06	–	V/°C
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 80 V, V_{GS} = 0 V$	–	–	1	μA
		$V_{DS} = 80 V, T_C = 150^\circ C$	–	–	500	
I_{GSS}	Gate to Body Leakage Current	$V_{GS} = \pm 20 V, V_{DS} = 0 V$	–	–	± 100	nA

On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250 \mu A$	2.0	–	4.0	V
$R_{DS(on)}$	Static Drain to Source On-Resistance	$V_{GS} = 10 V, I_D = 67 A$	–	3.7	4.5	m Ω
g_{FS}	Forward Transconductance	$V_{DS} = 10 V, I_D = 67 A$	–	127	–	S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 50 V, V_{GS} = 0 V, f = 1 MHz$	–	3961	5270	pF
C_{oss}	Output Capacitance		–	925	1230	
C_{rss}	Reverse Transfer Capacitance		–	34	–	
$C_{oss(er)}$	Energy Related Output Capacitance	$V_{DS} = 50 V, V_{GS} = 0 V$	–	1521	–	pF
$Q_{g(tot)}$	Total Gate Charge at 10 V	$V_{GS} = 10 V, V_{DS} = 50 V, I_D = 100 A$	–	57	74	nC
Q_{gs}	Gate to Source Gate Charge		–	17	–	
Q_{gs2}	Gate Charge Threshold to Plateau		–	8	–	
Q_{gd}	Gate to Drain “Miller” Charge		–	13	–	
ESR	Equivalent Series Resistance (G-S)		$f = 1 MHz$	–	1.9	

Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 50 V, I_D = 100 A,$ $V_{GS} = 10 V, R_{GEN} = 4.7 \Omega$ (Note 4)	–	23	56	ns
t_r	Turn-On Rise Time		–	26	62	
$t_{d(off)}$	Turn-Off Delay Time		–	50	110	
t_f	Turn-Off Fall Time		–	15	40	

Drain-Source Diode Characteristics and Maximum Ratings

I_S	Maximum Continuous Drain to Source Diode Forward Current	–	–	67	A	
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current	–	–	268	A	
V_{SD}	Drain to Source Diode Forward Voltage	$V_{GS} = 0 V, I_{SD} = 67 A$	–	–	1.3	V
t_{rr}	Reverse Recovery Time	$V_{GS} = 0 V, V_{DD} = 50 V, I_{SD} = 100 A,$ $di_F/dt = 100 A/\mu s$	–	75	–	ns
Q_{rr}	Reverse Recovery Charge		–	120	–	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTES:

1. Repetitive Rating: Pulse-width limited by maximum junction temperature.
2. L = 3 mH, $I_{AS} = 20.6 A$, $R_G = 25 \Omega$ starting $T_J = 25^\circ C$.
3. $I_{SD} \leq 100 A$, $di/dt \leq 200 A/\mu s$, $V_{DD} \leq BV_{DSS}$, starting $T_J = 25^\circ C$.
4. Essentially independent of operating temperature.

TYPICAL CHARACTERISTICS

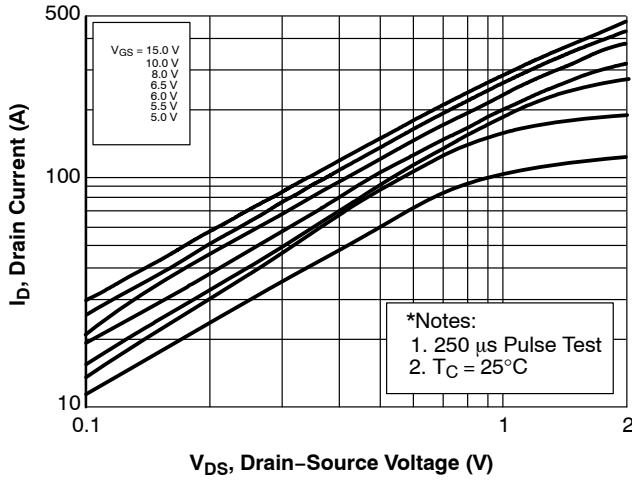


Figure 1. On-Region Characteristics

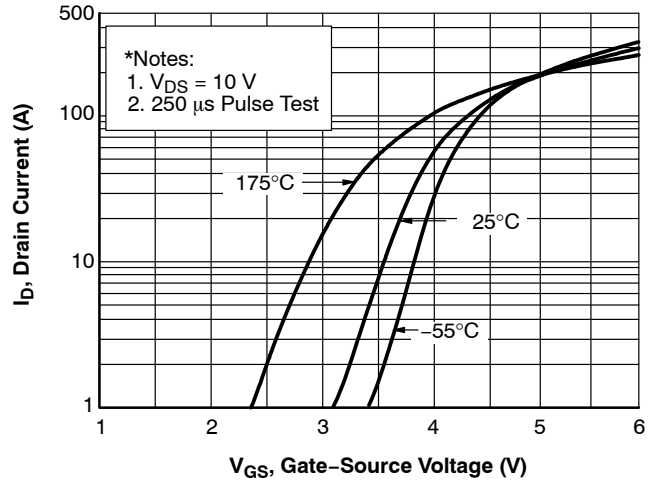


Figure 2. Transfer Characteristics

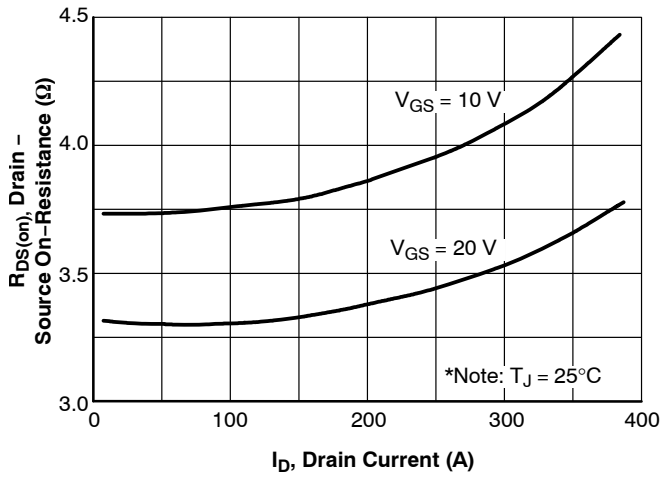


Figure 3. On-Resistance Variation vs Drain Current and Gate Voltage

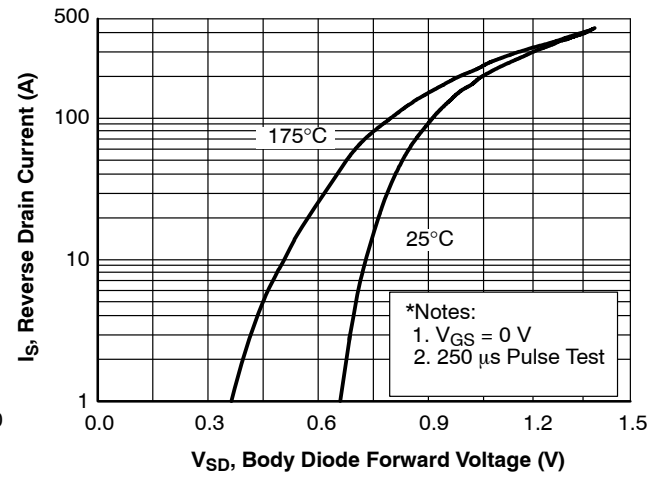


Figure 4. Body Diode Forward Voltage Variation vs Source Current and Temperature

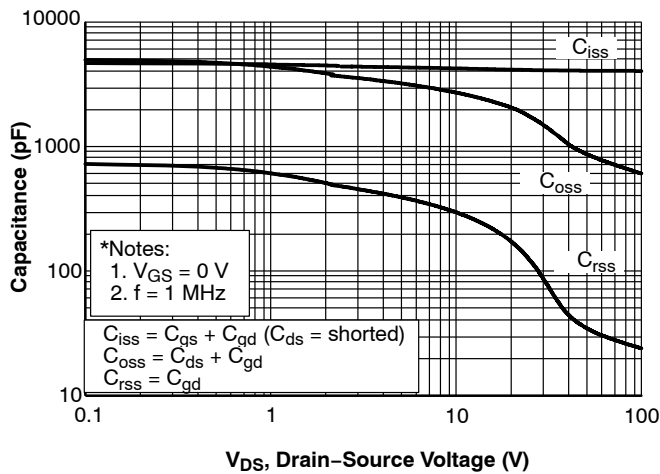


Figure 5. Capacitance Characteristics

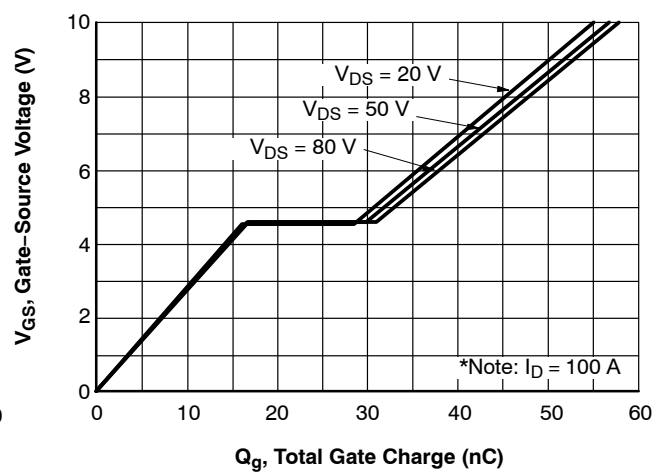


Figure 6. Gate Charge Characteristics

TYPICAL CHARACTERISTICS (CONTINUED)

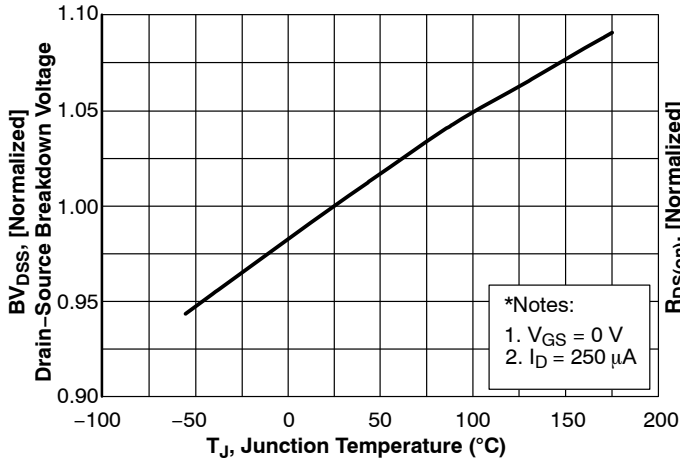


Figure 7. Breakdown Voltage Variation vs Temperature

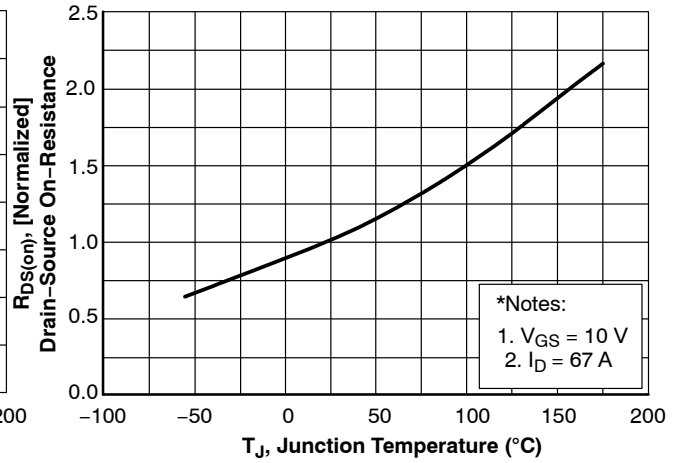


Figure 8. On-Resistance Variation vs Temperature

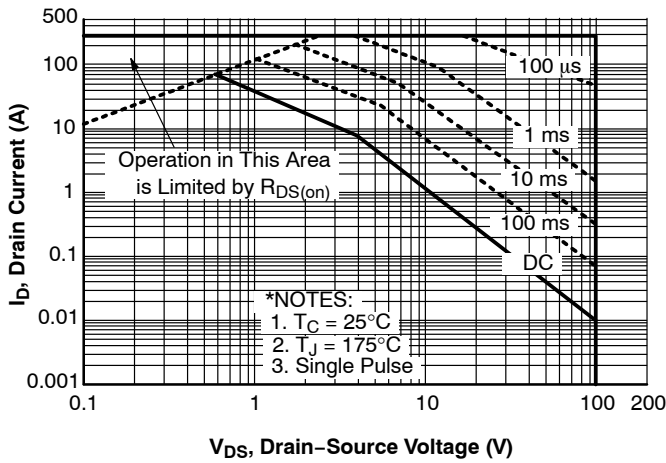


Figure 9. Maximum Safe Operating Area vs. Case Temperature

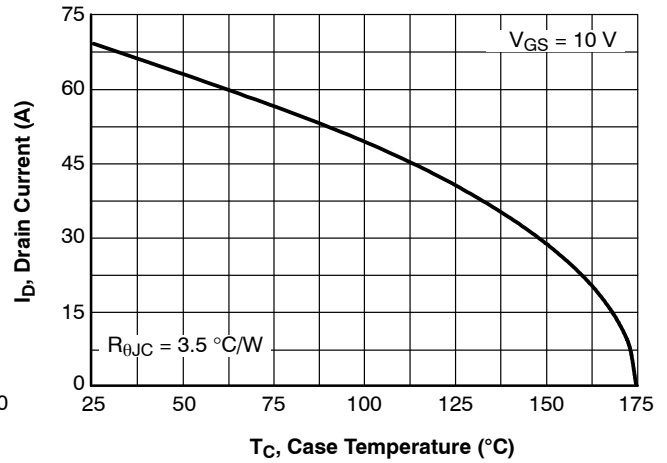


Figure 10. Maximum Drain Current

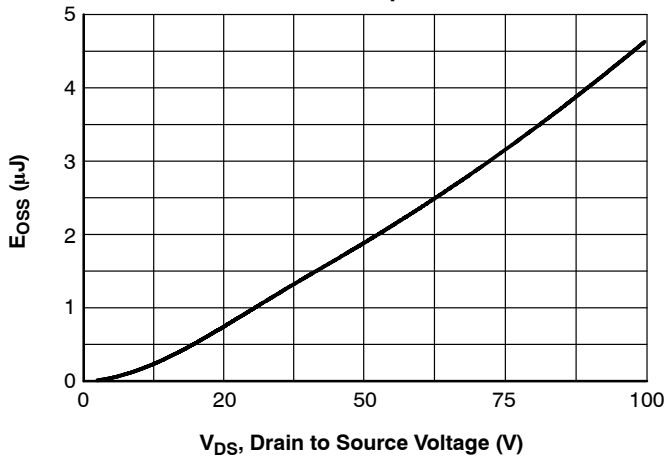


Figure 11. E_{oss} vs. Drain to Source Voltage

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TYPICAL CHARACTERISTICS (CONTINUED)

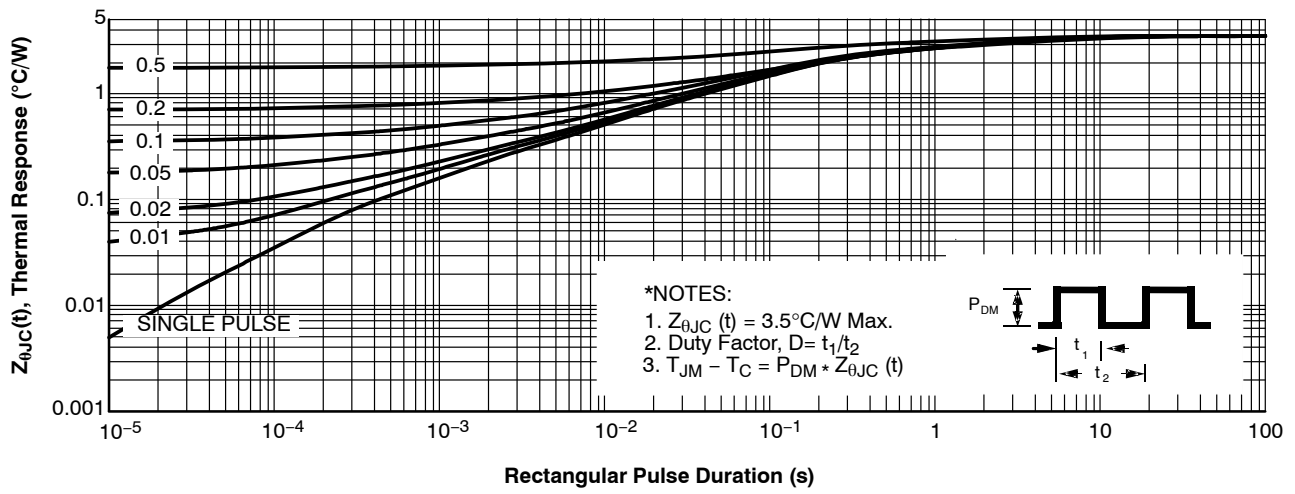


Figure 12. Transient Thermal Response Curve

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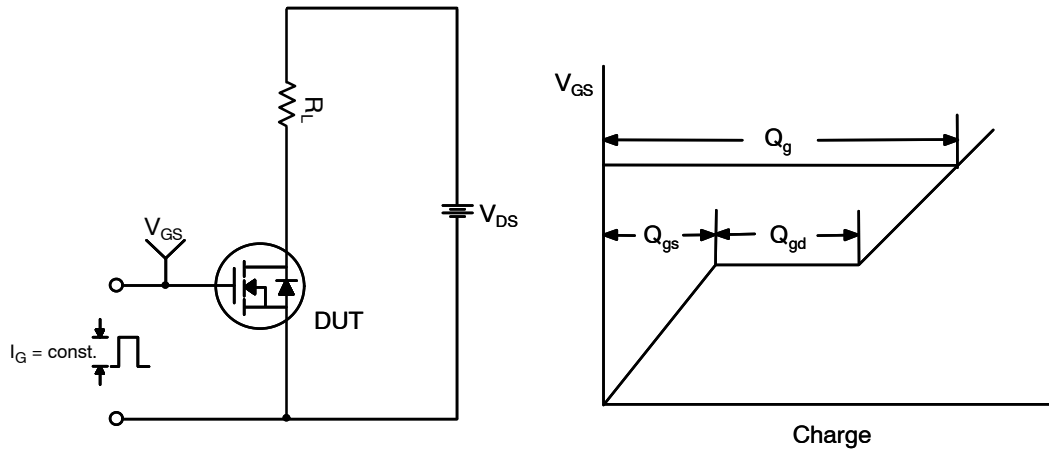


Figure 13. Gate Charge Test Circuit & Waveform

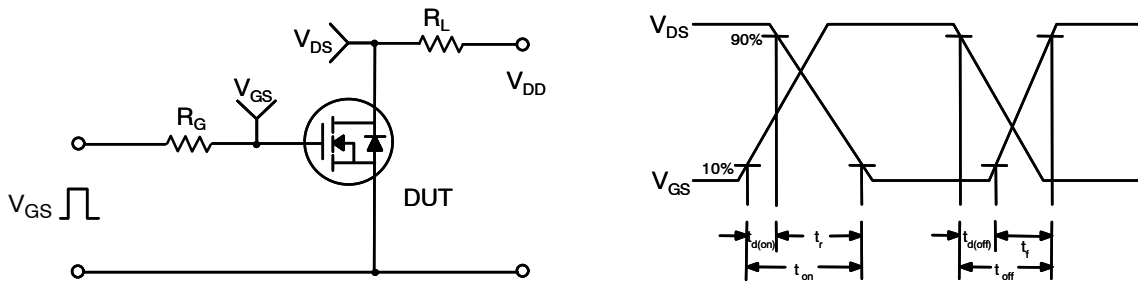


Figure 14. Resistive Switching Test Circuit & Waveforms

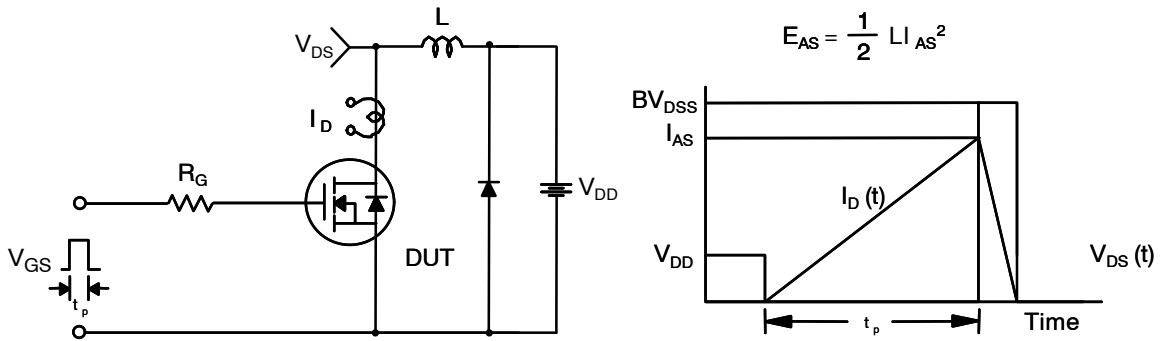


Figure 15. Unclamped Inductive Switching Test Circuit & Waveforms

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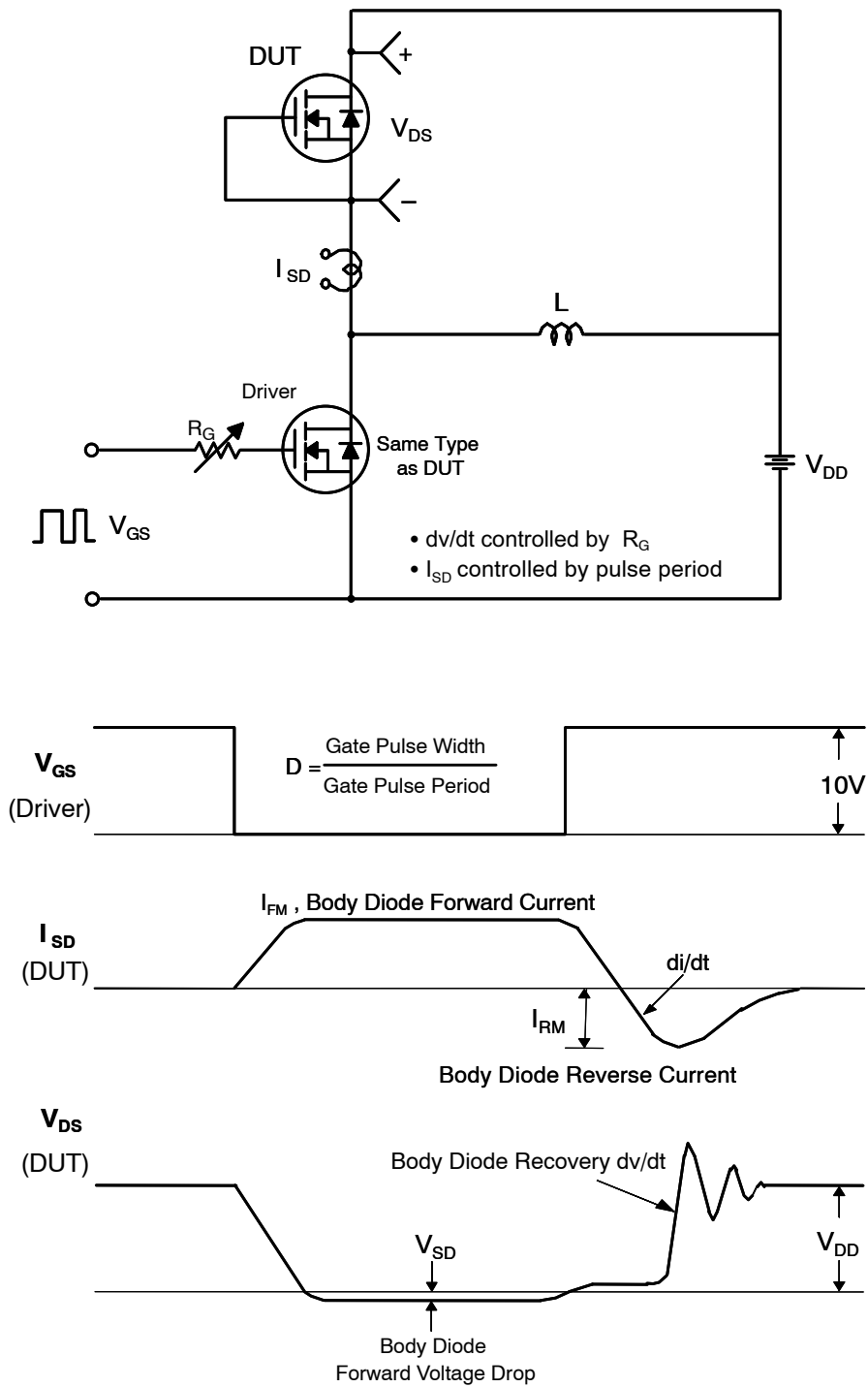


Figure 16. Peak Diode Recovery dv/dt Test Circuit & Waveforms

MECHANICAL CASE OUTLINE

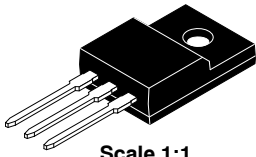
PACKAGE DIMENSIONS

ON Semiconductor®

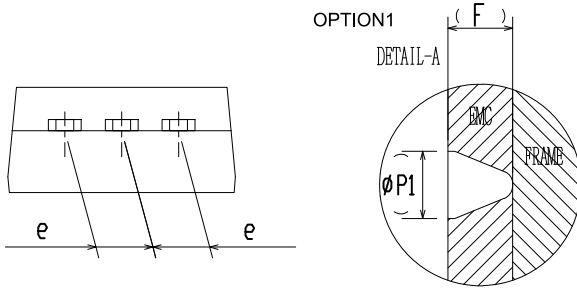
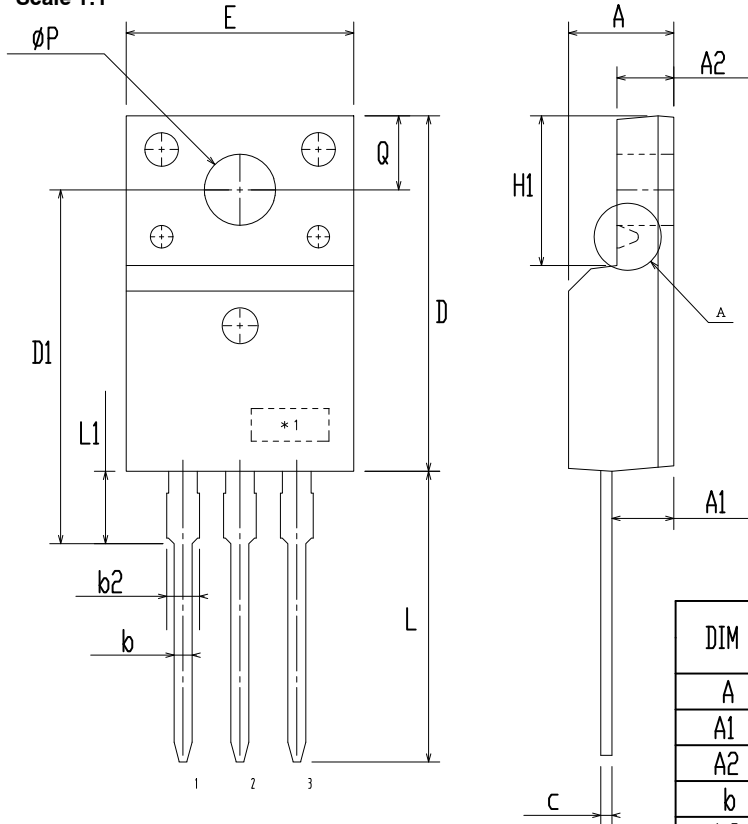


TO-220 Fullpack, 3-Lead / TO-220F-3SG
CASE 221AT
ISSUE B

DATE 19 JAN 2021



Scale 1:1



DIM	MILLIMETERS		
	MIN	NOM	MAX
A	4.50	4.70	4.90
A1	2.56	2.76	2.96
A2	2.34	2.54	2.74
b	0.70	0.80	0.90
b2	~	~	1.47
c	0.45	0.50	0.60
D	15.67	15.87	16.07
D1	15.60	15.80	16.00
E	9.96	10.16	10.36
e	2.34	2.54	2.74
F	~	0.84	~
H1	6.48	6.68	6.88
L	12.78	12.98	13.18
L1	3.03	3.23	3.43
∅ P	2.98	3.18	3.38
∅ P1	~	1.00	~
Q	3.20	3.30	3.40

NOTES:

- A. DIMENSION AND TOLERANCE AS ASME Y14.5-2009
- B. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR PROTRUCTIONS.
- C. OPTION 1 - WITH SUPPORT PIN HOLE
OPTION 2 - NO SUPPORT PIN HOLE

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