

MOSFET – Dual N-Channel, Logic Level PWM Optimized POWERTRENCH®

9.4 A, 20 V

FDS6898A

General Description

These N-Channel Logic Level MOSFETs are produced using onsemi's advanced POWERTRENCH process that has been especially tailored to minimize the on-state resistance and yet maintain superior switching performance.

These devices are well suited for low voltage and battery powered applications where low in-line power loss and fast switching are required.

Features

- 9.4 A, 20 V
 - $R_{DS(on)} = 14 \text{ m}\Omega$ at $V_{GS} = 4.5 \text{ V}$
 - $R_{DS(on)} = 18 \text{ m}\Omega$ at $V_{GS} = 2.5 \text{ V}$
- Low Gate Charge (16 nC typical)
- High Performance Trench Technology for Extremely Low $R_{DS(on)}$
- High Power and Current Handling Capability
- This Device is Pb-Free, Halide Free and is RoHS Compliant

MOSFET MAXIMUM RATINGS

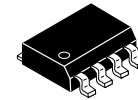
($T_A = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Ratings	Unit
V_{DSS}	Drain-Source Voltage	20	V
V_{GSS}	Gate-Source Voltage	± 12	V
I_D	Drain Current – Continuous (Note 1a) – Pulsed	9.4 38	A
P_D	Power Dissipation for Dual Operation	2	W
	Power Dissipation for Single Operation (Note 1a)	1.6	
	(Note 1b)	1	
	(Note 1c)	0.9	
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to $+150$	$^\circ\text{C}$

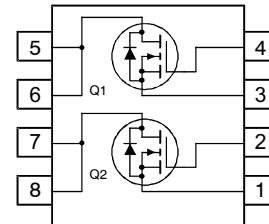
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

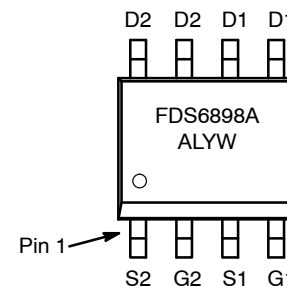
Symbol	Parameter	Ratings	Unit
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a)	78	$^\circ\text{C/W}$
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Note 1)	40	$^\circ\text{C/W}$



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MARKING DIAGRAM



FDS6898A = Specific Device Code
 A = Assembly Site
 L = Wafer Lot Number
 YW = Assembly Start Week

ORDERING INFORMATION

Device	Package	Shipping†
FDS6898A	SOIC8 (Pb-Free/ Halide Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, [BRD8011/D](#).

FDS6898A

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	20	–	–	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$, Referenced to 25°C	–	21	–	mV/ $^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 16\text{ V}, V_{GS} = 0\text{ V}$	–	–	1	μA
I_{GSSF}	Gate-Body Leakage, Forward	$V_{GS} = 12\text{ V}, V_{DS} = 0\text{ V}$	–	–	100	nA
I_{GSSR}	Gate-Body Leakage, Reverse	$V_{GS} = -12\text{ V}, V_{DS} = 0\text{ V}$	–	–	-100	nA

ON CHARACTERISTICS (Note 2)

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	0.5	1	1.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$, Referenced to 25°C	–	-3.5	–	mV/ $^\circ\text{C}$
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 4.5\text{ V}, I_D = 9.4\text{ A}$	–	10	14	m Ω
		$V_{GS} = 2.5\text{ V}, I_D = 8.3\text{ A}$	–	13	18	
		$V_{GS} = 4.5\text{ V}, I_D = 9.4\text{ A}, T_J = 125^\circ\text{C}$	–	14	21	
$I_{D(on)}$	On-State Drain Current	$V_{GS} = 4.5\text{ V}, V_{DS} = 5\text{ V}$	19	–	–	A
g_{FS}	Forward Transconductance	$V_{DS} = 5\text{ V}, I_D = 9.4\text{ A}$	–	47	–	S

DYNAMIC CHARACTERISTICS

C_{iss}	Input Capacitance	$V_{DS} = 10\text{ V}, V_{GS} = 0\text{ V}, f = 1.0\text{ MHz}$	–	1821	–	pF
C_{oss}	Output Capacitance		–	440	–	
C_{rss}	Reverse Transfer Capacitance		–	208	–	

SWITCHING CHARACTERISTICS (Note 2)

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 10\text{ V}, I_D = 1\text{ A}, V_{GS} = 4.5\text{ V}, R_{GEN} = 6\text{ }\Omega$	–	10	20	ns
t_r	Rise Time		–	15	27	
$t_{d(off)}$	Turn-Off Delay Time		–	34	55	
t_f	Fall Time		–	16	29	
Q_g	Total Gate Charge	$V_{DS} = 10\text{ V}, V_{GS} = 4.5\text{ V}, I_D = 9.4\text{ A}$	–	16	23	nC
Q_{gs}	Gate-Source Charge		–	3	–	
Q_{gd}	Gate-Drain Charge		–	4	–	

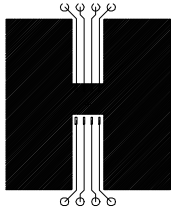
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS

I _S	Maximum Continuous Drain–Source Diode Forward Current		–	–	1.3	A
V _{SD}	Drain–Source Diode Forward Voltage	V _{GS} = 0 V, I _S = 1.3 A (Note 2)	–	0.7	1.2	V

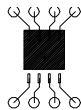
Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTES:

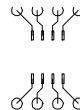
- $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a) 78°C/W when mounted on a 0.5 in^2 pad of 2 oz. copper.



b) 125°C/W when mounted on a 0.02 in^2 pad of 2 oz. copper.



c) 135°C/W when mounted on a minimum mounting pad.

Scale 1 : 1 on letter size paper

- Pulse Test: Pulse Width < $300\text{ }\mu\text{s}$, Duty Cycle < 2.0%

TYPICAL CHARACTERISTICS

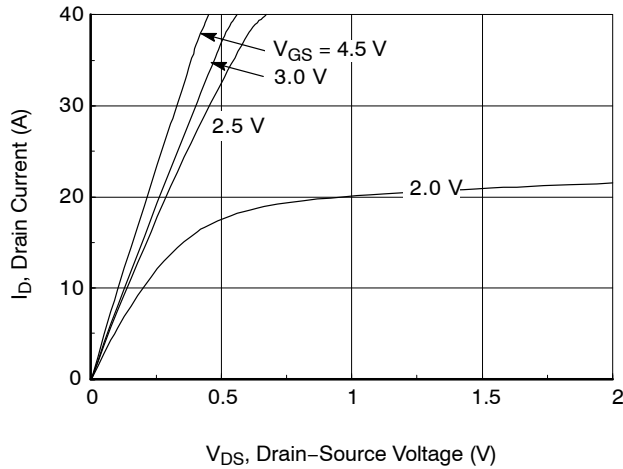


Figure 1. On-Region Characteristics

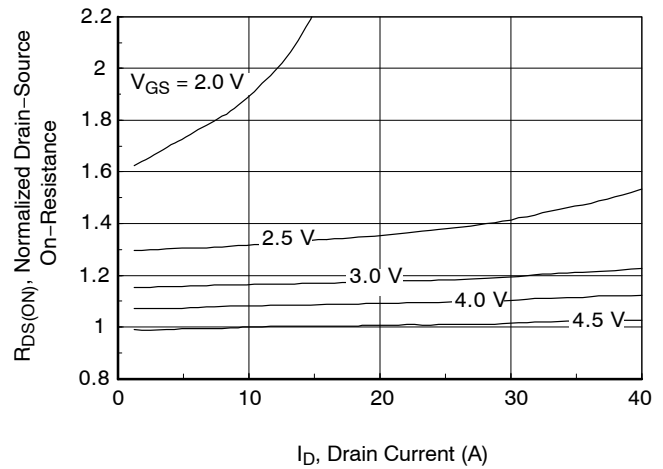


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage

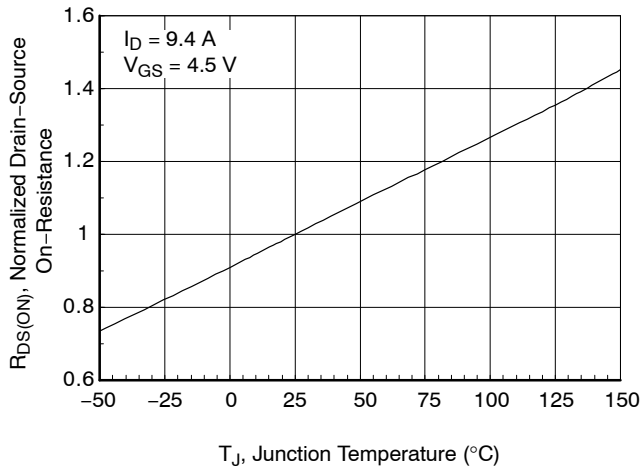


Figure 3. On-Resistance Variation with Temperature

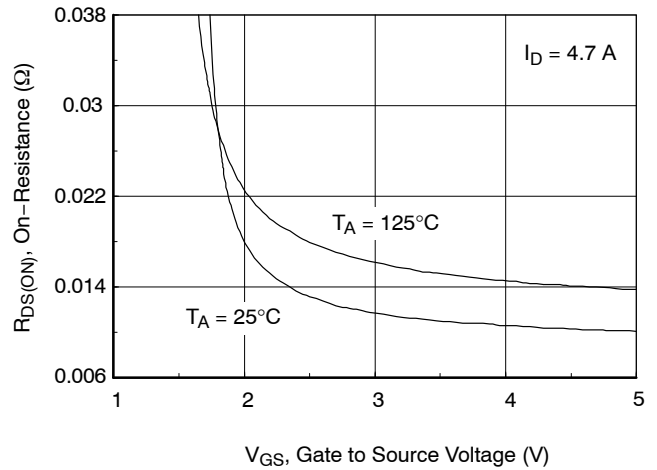


Figure 4. On-Resistance Variation with Gate-to-Source Voltage

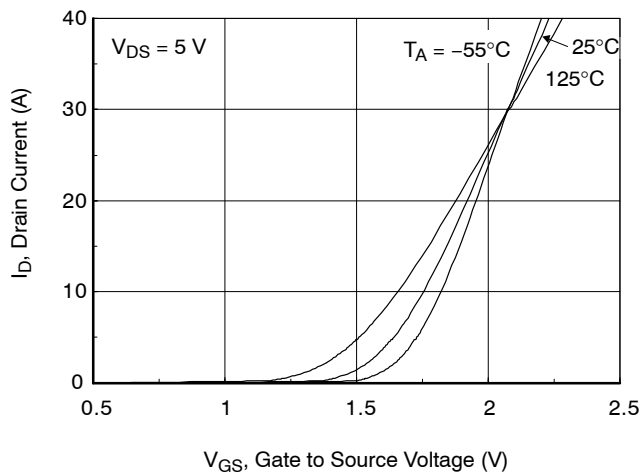


Figure 5. Transfer Characteristics

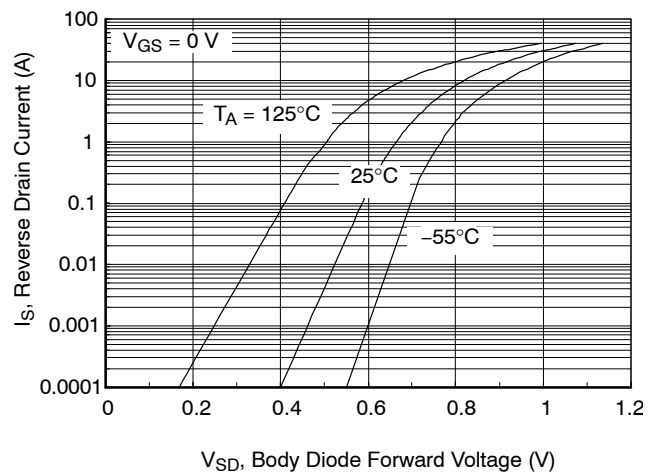


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature

TYPICAL CHARACTERISTICS (continued)

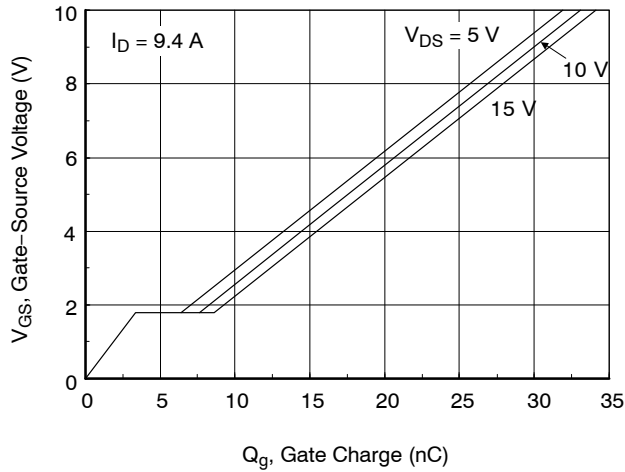


Figure 7. Gate Charge Characteristics

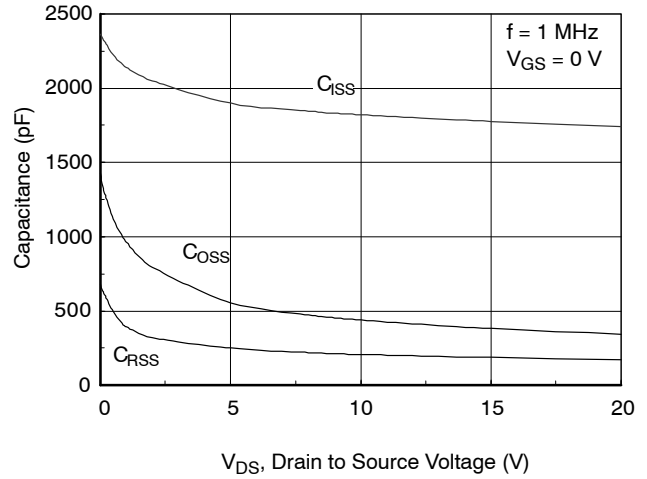


Figure 8. Capacitance Characteristics

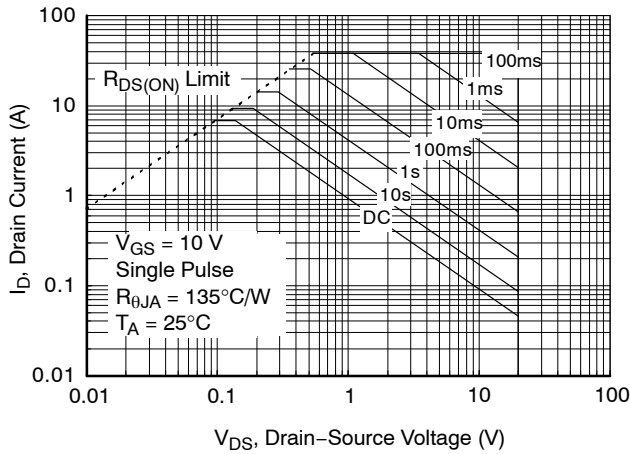


Figure 9. Maximum Safe Operating Area

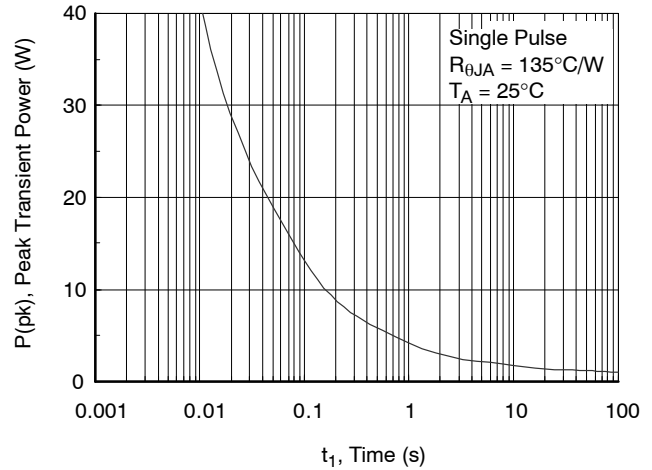


Figure 10. Single Pulse Maximum Power Dissipation

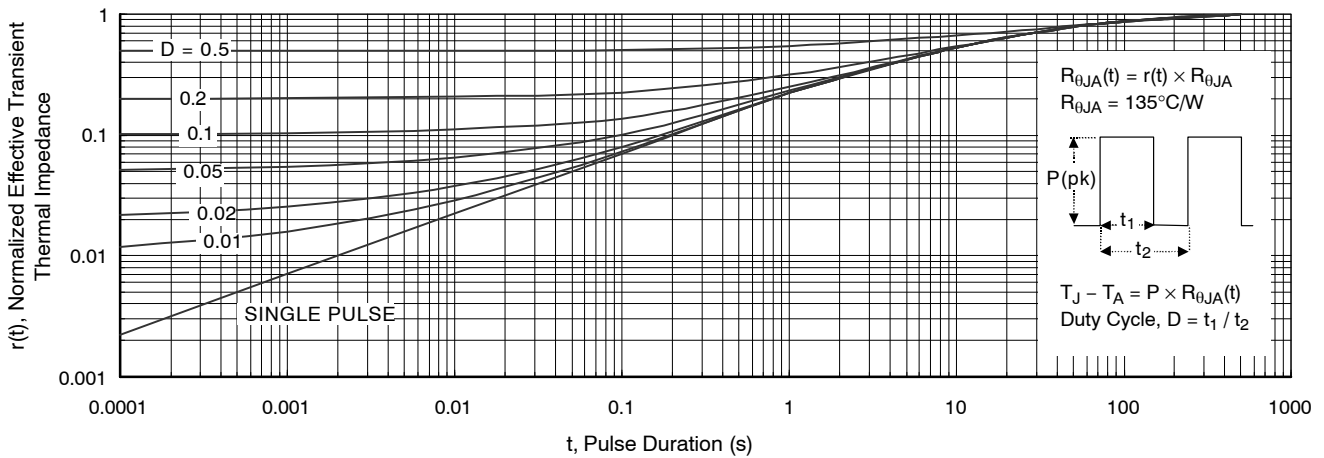
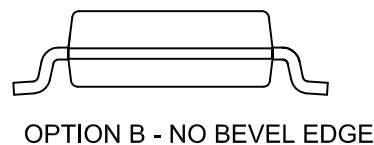
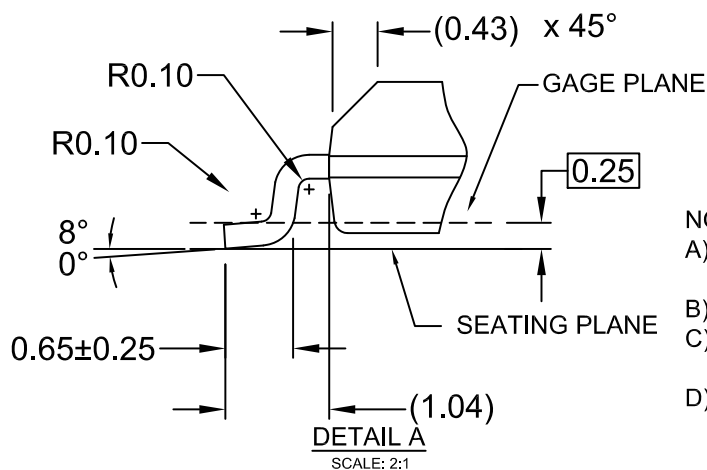
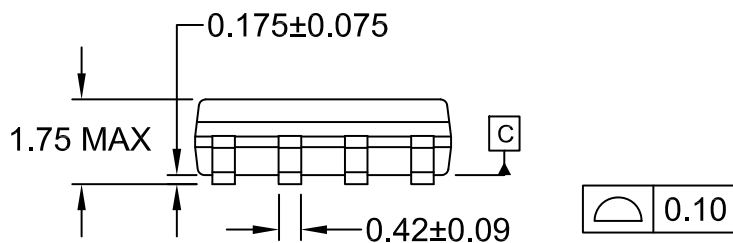


Figure 11. Transient Thermal Response Curve

Thermal characterization performed using the conditions described in Note 1c.
Transient thermal response will change depending on the circuit board design.

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ISSUE A

DATE 24 AUG 2017



- NOTES:
- A) THIS PACKAGE CONFORMS TO JEDEC MS-012, VARIATION AA.
 - B) ALL DIMENSIONS ARE IN MILLIMETERS.
 - C) DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS.
 - D) LANDPATTERN STANDARD: SOIC127P600X175-8M

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