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September 2014

# FDZ1323NZ

## Common Drain N-Channel 2.5 V PowerTrench® WL-CSP MOSFET

20 V, 10 A, 13 mΩ

### Features

- Max  $r_{S1S2(on)}$  = 13 mΩ at  $V_{GS} = 4.5$  V,  $I_{S1S2} = 1$  A
- Max  $r_{S1S2(on)}$  = 13 mΩ at  $V_{GS} = 3.8$  V,  $I_{S1S2} = 1$  A
- Max  $r_{S1S2(on)}$  = 16 mΩ at  $V_{GS} = 3.1$  V,  $I_{S1S2} = 1$  A
- Max  $r_{S1S2(on)}$  = 18 mΩ at  $V_{GS} = 2.5$  V,  $I_{S1S2} = 1$  A
- Occupies only 3 mm<sup>2</sup> of PCB area
- Ultra-thin package: less than 0.35 mm height when mounted to PCB
- High power and current handling capability
- HBM ESD protection level > 3.6 kV (Note 3)
- RoHS Compliant

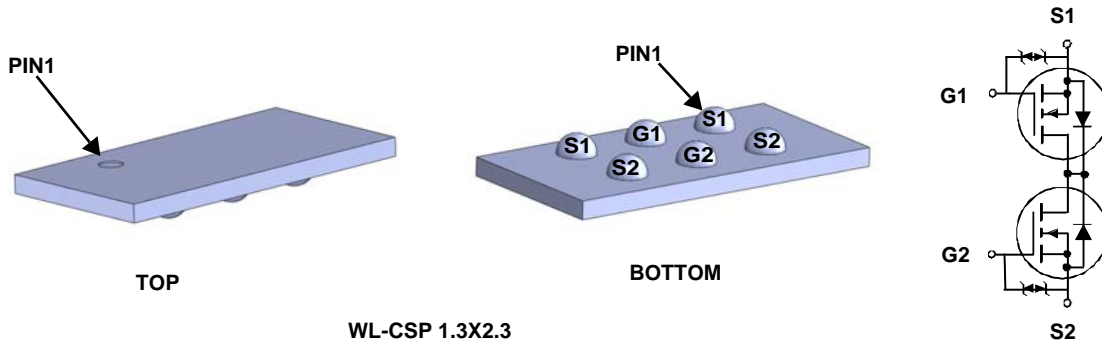


### General Description

This device is designed specifically as a single package solution for Li-Ion battery pack protection circuit and other ultra-portable applications. It features two common drain N-channel MOSFETs, which enables bidirectional current flow, on Fairchild's advanced PowerTrench® process with state of the art "low pitch" WLCSP packaging process, the FDZ1323NZ minimizes both PCB space and  $r_{S1S2(on)}$ . This advanced WLCSP MOSFET embodies a breakthrough in packaging technology which enables the device to combine excellent thermal transfer characteristics, ultra-low profile packaging, low gate charge and low  $r_{S1S2(on)}$ .

### Applications

- Battery management
- Load switch
- Battery protection



### MOSFET Maximum Ratings $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Ratings	Units
$V_{S1S2}$	Source1 to Source2 Voltage	20	V
$V_{GS}$	Gate to Source Voltage	±12	V
$I_{S1S2}$	Source1 to Source2 Current -Continuous $T_A = 25^\circ\text{C}$ (Note 1a)	10	A
	-Pulsed	40	
$P_D$	Power Dissipation $T_A = 25^\circ\text{C}$ (Note 1a)	2	W
	Power Dissipation $T_A = 25^\circ\text{C}$ (Note 1b)	0.5	
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to +150	$^\circ\text{C}$

### Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	62	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1b)	257	

### Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
EC	FDZ1323NZ	WL-CSP 1.3X2.3	7"	8 mm	5000 units

FDZ1323NZ Common Drain N-Channel 2.5 V PowerTrench® WL-CSP MOSFET

## Electrical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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### Off Characteristics

$I_{S1S2}$	Zero Gate Voltage Source1 to Source2 Current	$V_{S1S2} = 16\text{ V}, V_{GS} = 0\text{ V}$			1	$\mu\text{A}$
$I_{GSS}$	Gate to Source Leakage Current	$V_{GS} = \pm 12\text{ V}, V_{S1S2} = 0\text{ V}$			$\pm 10$	$\mu\text{A}$

### On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{S1S2}, I_{S1S2} = 250\ \mu\text{A}$	0.4	0.9	1.2	V
$r_{S1S2(on)}$	Static Source1 to Source2 On Resistance	$V_{GS} = 4.5\text{ V}, I_{S1S2} = 1\text{ A}$	4.5	9.7	13	m $\Omega$
		$V_{GS} = 3.8\text{ V}, I_{S1S2} = 1\text{ A}$	5.5	10	13	
		$V_{GS} = 3.1\text{ V}, I_{S1S2} = 1\text{ A}$	7	11	16	
		$V_{GS} = 2.5\text{ V}, I_{S1S2} = 1\text{ A}$	8	13	18	
		$V_{GS} = 4.5\text{ V}, I_{S1S2} = 1\text{ A}, T_J = 125^\circ\text{C}$		13	20	
$g_{FS}$	Forward Transconductance	$V_{S1S2} = 5\text{ V}, I_{S1S2} = 1\text{ A}$		9		S

### Dynamic Characteristics

$C_{iss}$	Input Capacitance	$V_{S1S2} = 10\text{ V}, V_{GS} = 0\text{ V},$ $f = 1\text{ MHz}$		1545	2055	pF
$C_{oss}$	Output Capacitance			269	405	pF
$C_{rss}$	Reverse Transfer Capacitance			252	380	pF

### Switching Characteristics

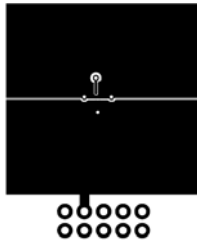
$t_{d(on)}$	Turn-On Delay Time	$V_{S1S2} = 10\text{ V}, I_{S1S2} = 1\text{ A},$ $V_{GS} = 4.5\text{ V}, R_{GEN} = 6\ \Omega$		12	22	ns
$t_r$	Rise Time			13	23	ns
$t_{d(off)}$	Turn-Off Delay Time			34	54	ns
$t_f$	Fall Time			13	23	ns
$Q_g$	Total Gate Charge			17	24	nC
$Q_{gs}$	Gate to Source1 Gate Charge	$V_{S1S2} = 10\text{ V}, I_{S1S2} = 1\text{ A},$ $V_{G1S1} = 4.5\text{ V}, V_{G2S2} = 0\text{ V}$		1.9		nC
$Q_{gd}$	Gate to Source2 "Miller" Charge			5.4		nC

### Source1 to Source2 Diode Characteristics

$I_{fss}$	Maximum Continuous Source1 to Source2 Diode Forward Current			1	A
$V_{fss}$	Source1 to Source2 Diode Forward Voltage	$V_{G1S1} = 0\text{ V}, V_{G2S2} = 4.5\text{ V},$ $I_{fss} = 1\text{ A}$ (Note 2)	0.6	1.2	V

#### Notes:

- $R_{\theta JA}$  is determined with the device mounted on a 1 in<sup>2</sup> pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.



a. 62 °C/W when mounted on a 1 in<sup>2</sup> pad of 2 oz copper.



b. 257 °C/W when mounted on a minimum pad of 2 oz copper.

- Pulse Test: Pulse Width < 300  $\mu\text{s}$ , Duty cycle < 2.0%.

- The diode connected between the gate and source serves only protection against ESD. No gate overvoltage rating is implied.

**Typical Characteristics**  $T_J = 25^\circ\text{C}$  unless otherwise noted

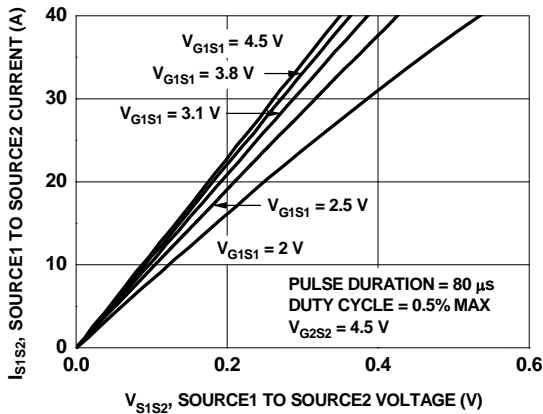


Figure 1. On-Region Characteristics

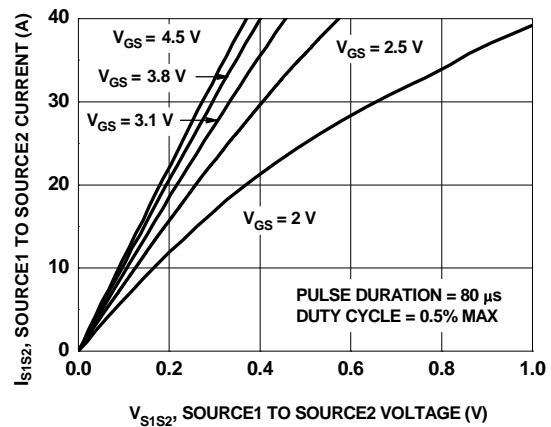


Figure 2. On-Region Characteristics

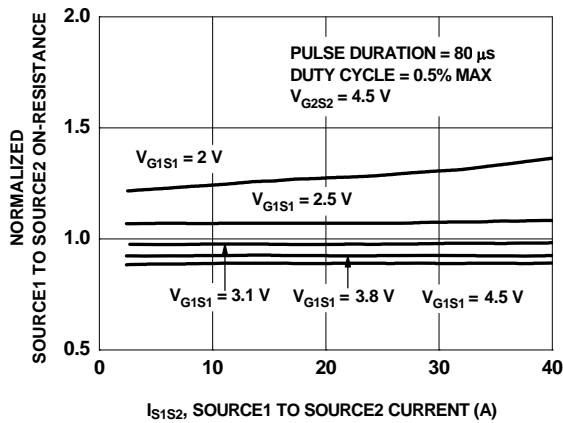


Figure 3. Normalized On-Resistance vs Source1 to Source2 Current and Gate Voltage

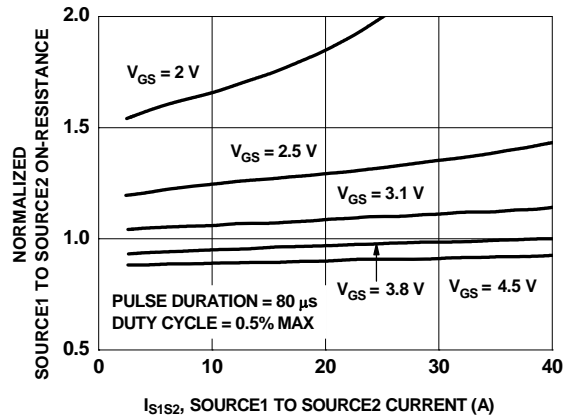


Figure 4. Normalized On-Resistance vs Source1 to Source2 Current and Gate Voltage

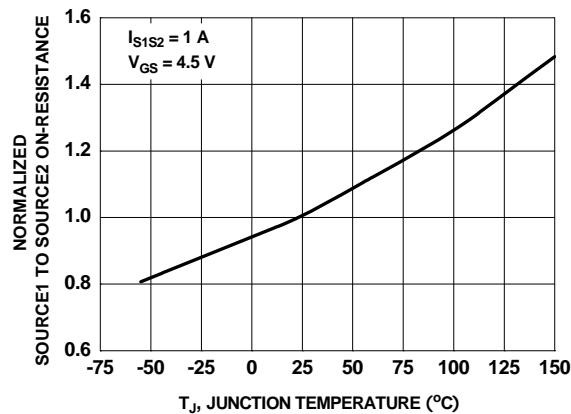


Figure 5. Normalized On Resistance vs Junction Temperature

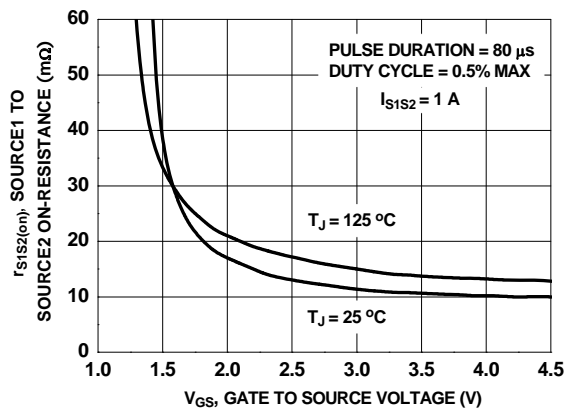
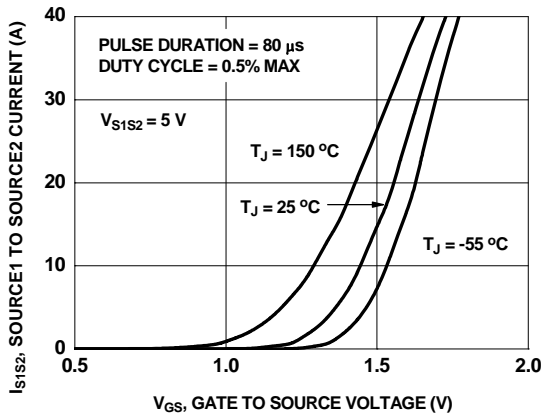
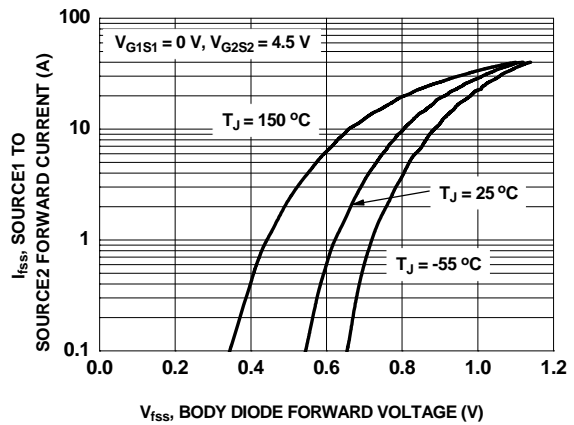


Figure 6. On Resistance vs Gate to Source Voltage

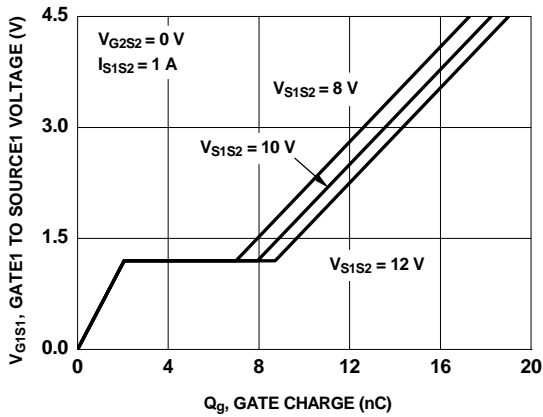
**Typical Characteristics**  $T_J = 25^\circ\text{C}$  unless otherwise noted



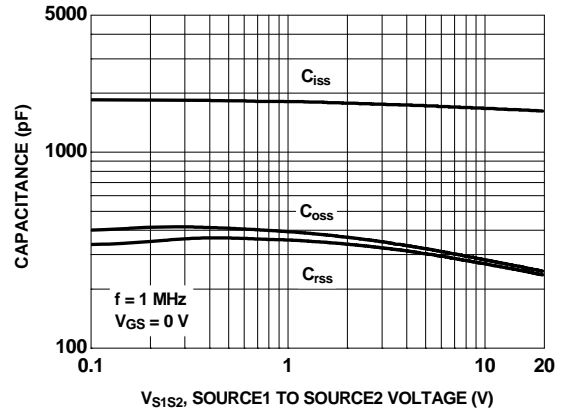
**Figure 7. Transfer Characteristics**



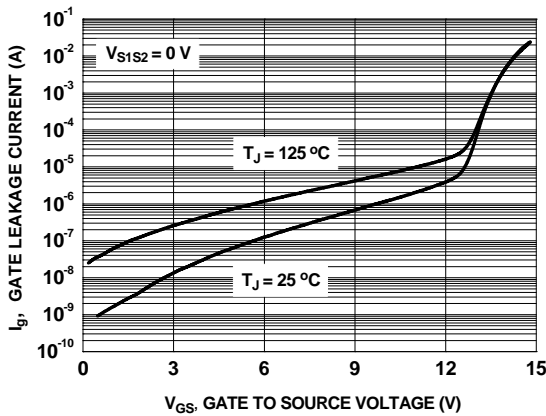
**Figure 8. Source1 to Source2 Diode Forward Voltage vs Source Current**



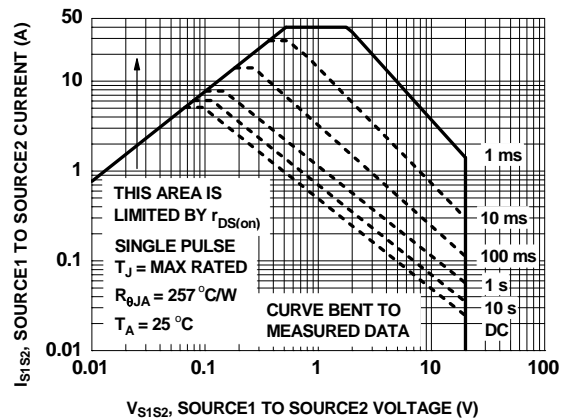
**Figure 9. Gate Charge Characteristics**



**Figure 10. Capacitance vs Source1 to Source2 Voltage**



**Figure 11. Gate Leakage Current vs Gate to Source Voltage**



**Figure 12. Forward Bias Safe Operating Area**

**Typical Characteristics**  $T_J = 25^\circ\text{C}$  unless otherwise noted

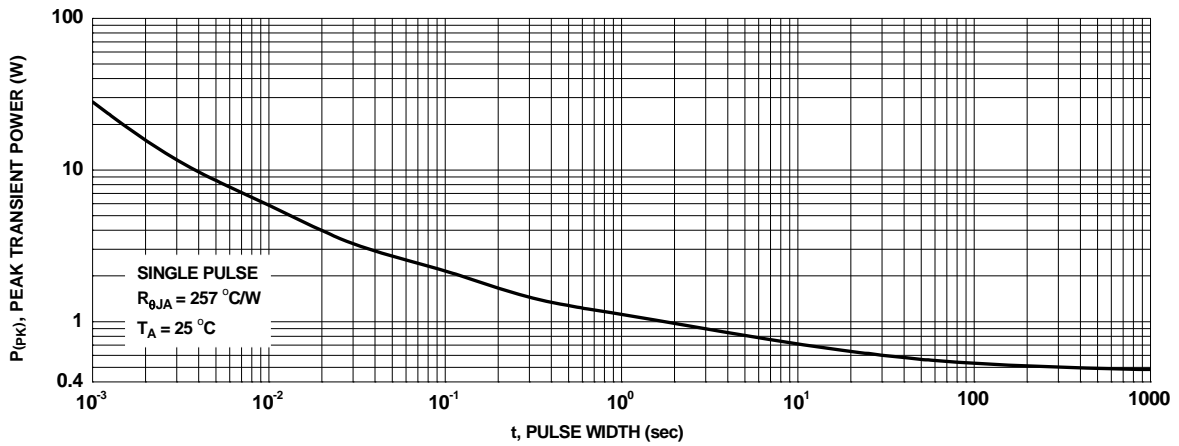


Figure 13. Single Pulse Maximum Power Dissipation

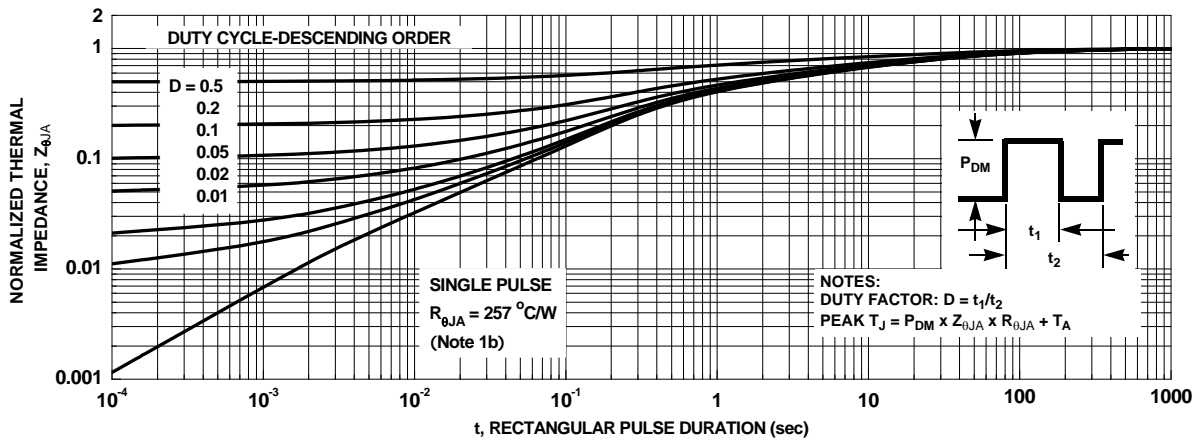
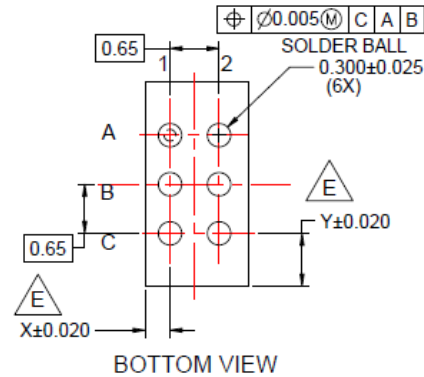
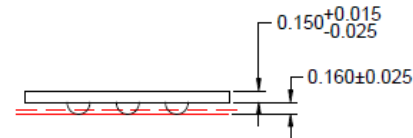
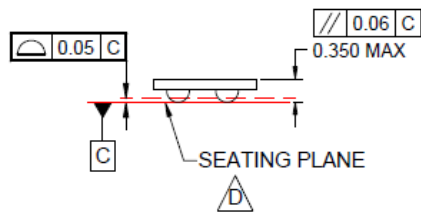
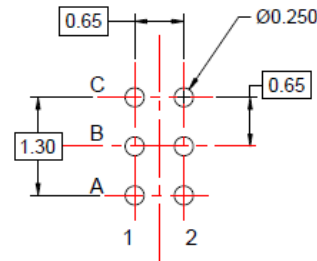
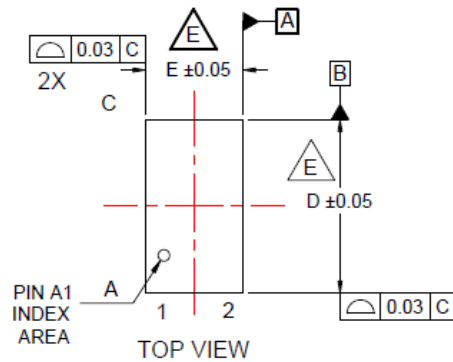


Figure 14. Junction-to-Ambient Transient Thermal Response Curve

## Dimensional Outline and Pad Layout



### NOTES:

- A. NO JEDEC REGISTRATION APPLIES.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCE PER ASME Y14.5M, 2009.
- D. DATUM C IS DEFINED BY THE SPHERICAL CROWNS OF THE BALLS.
- E. FOR DIMENSIONS D, E, X, AND Y SEE PRODUCT DATA SHEET.
- F. MKT-UC006ABREV2
- G. FOR PIN-OUT ASSIGNMENT, REFER TO DATA SHEET.



### Pin Definitions:

Gate	Source1	Source2
B1, B2	A1, C1	A2, C2

### Product Specific Dimensions:

D	E	X	Y
2.3 mm	1.3 mm	0.315 mm	0.49 mm



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