

Silicon Carbide (SiC) Schottky Diode – EliteSiC, 8 A, 650 V, D2, Power88

FFSM0865B

Silicon Carbide (SiC) Schottky Diodes use a completely new technology that provides superior switching performance and higher reliability compared to Silicon. No reverse recovery current, temperature independent switching characteristics, and excellent thermal performance sets Silicon Carbide as the next generation of power semiconductor. System benefits include highest efficiency, faster operating frequency, increased power density, reduced EMI, and reduced system size and cost.

Features

- Max Junction Temperature 175°C
- Avalanche Rated 33 mJ
- High Surge Current Capacity
- Positive Temperature Coefficient
- Ease of Paralleling
- No Reverse Recovery / No Forward Recovery
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

Applications

- General Purpose
- SMPS, Solar Inverter, UPS
- Power Switching Circuits

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

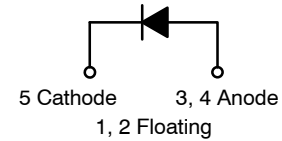
Parameter	Symbol	Value	Unit
Peak Repetitive Reverse Voltage	V _{RRM}	650	V
Single Pulse Avalanche Energy (starting T _C = 25°C, I _{L(pk)} = 11.5 A, L = 0.5 mH, V = 50 V)	E _{AS}	33	mJ
Continuous Rectified Forward Current	I _F	T _C < 153	A
		T _C < 135	
Non-Repetitive Peak Forward Surge Current (t _p = 10 μs)	I _{FM}	T _C = 25°C	A
		T _C = 150°C	
Non-Repetitive Forward Surge Current (Half-Sine Pulse)	I _{FSM}	T _C = 25°C t _p = 8.3 ms	A
Power Dissipation	P _{tot}	T _C = 25°C	W
		T _C = 150°C	
Operating Junction and Storage Temperature Range	T _J , T _{stg}	-55 to +175	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

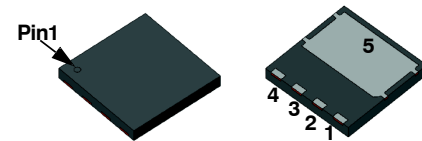
THERMAL RESISTANCE

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-Case	R _{θJC}	1.64	°C/W

V _{RRM}	I _F
650 V	8.0 A

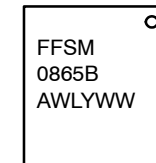


Schottky Diode



PQFN4 8×8, 2P
(Power88)
CASE 483AP

MARKING DIAGRAM



FFSM0865B	= Specific Device Code
A	= Assembly Site
WL	= Wafer Lot Number
Y	= Year
WW	= Work Week

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

FFSM0865B

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
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ON CHARACTERISTICS

V _F	Forward Voltage	I _F = 8.0 A, T _J = 25°C		1.39	1.7	V
		I _F = 8.0 A, T _J = 125°C		1.55		
		I _F = 8.0 A, T _J = 150°C		1.67		
I _R	Reverse Current	V _R = 650 V, T _J = 25°C		0.5	40	μA
		V _R = 650 V, T _J = 125°C		1.0	80	
		V _R = 650 V, T _J = 175°C		2.0	160	

CHARGES, CAPACITANCES & GATE RESISTANCE

Q _C	Total Capacitive Charge	V _C = 400 V		22		nC
C _{tot}		V _R = 1 V, f = 100 kHz		336		pF
		V _R = 200 V, f = 100 kHz		39		
		V _R = 400 V, f = 100 kHz		30		

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

PART MARKING AND ORDERING INFORMATION

Part Number	Top Mark	Package	Packing Method [†]	Quantity
FFSM0865B	FFSM0865B	PQFN4 8X8, 2P (Power88) (Halogen Free)	Tape & Reel	3000 units

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

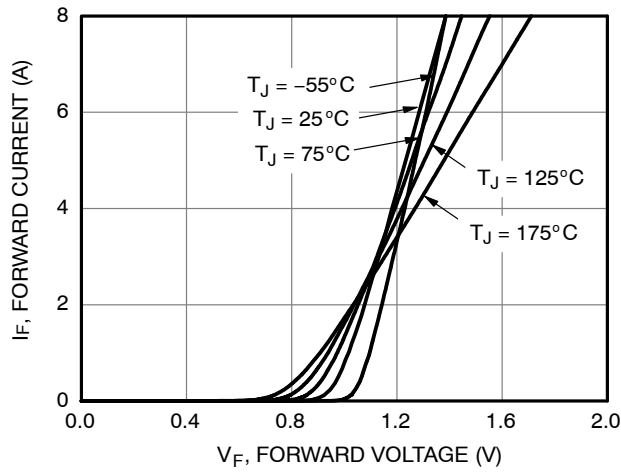
TYPICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)

Figure 1. Forward Characteristics

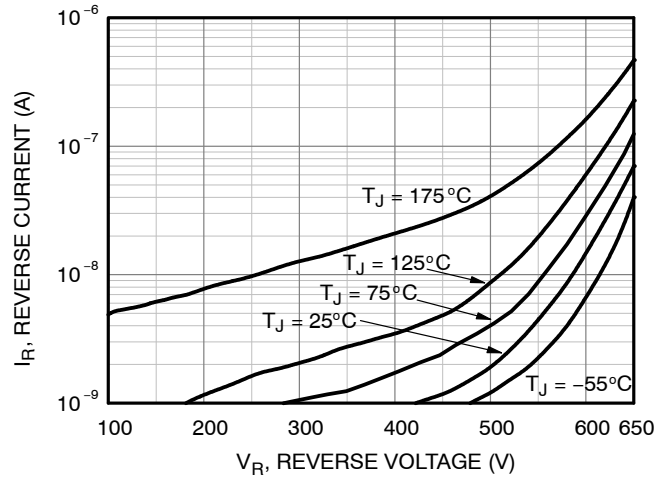


Figure 2. Reverse Characteristics

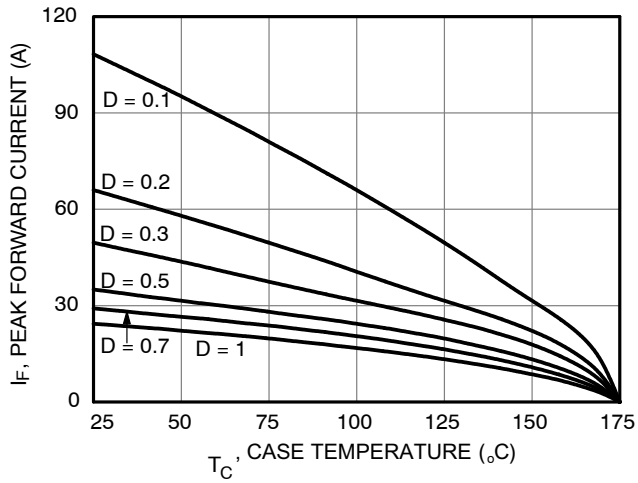


Figure 3. Current Derating

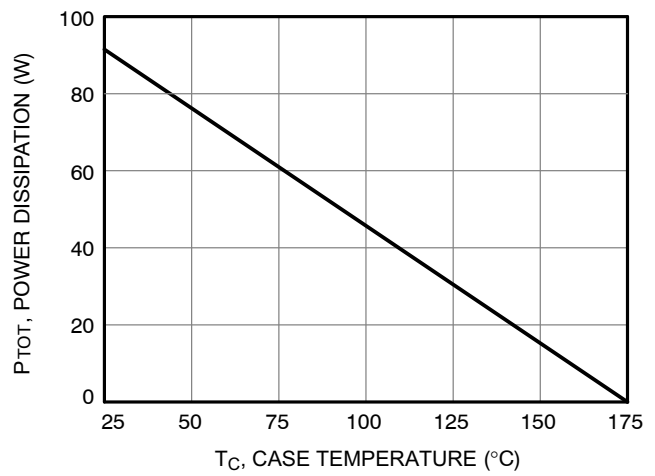


Figure 4. Power Derating

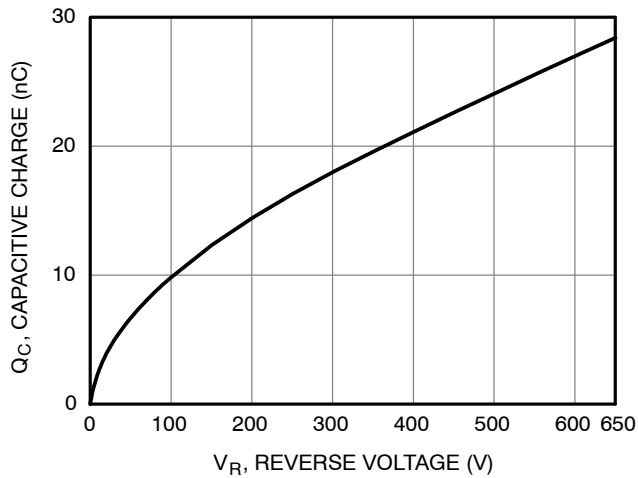


Figure 5. Capacitive Charge vs. Reverse Voltage

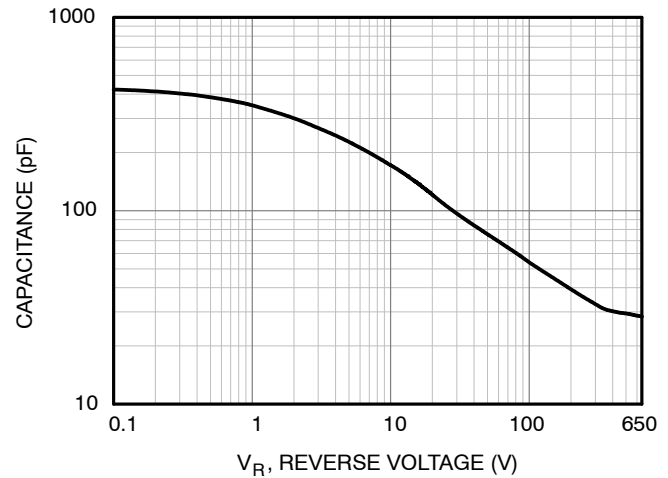


Figure 6. Capacitance vs. Reverse Voltage

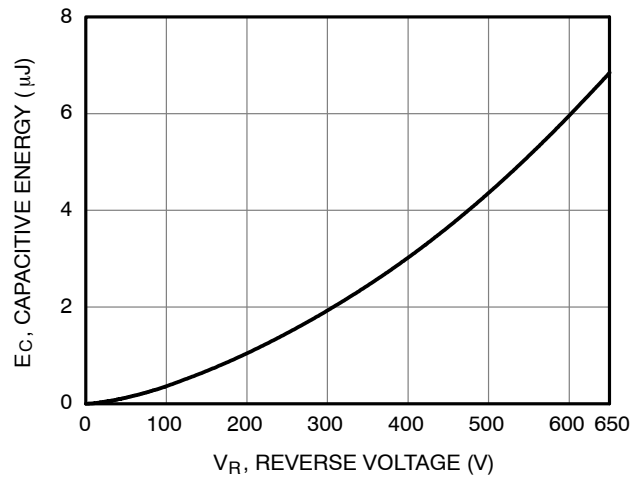
TYPICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)

Figure 7. Capacitance Stored Energy

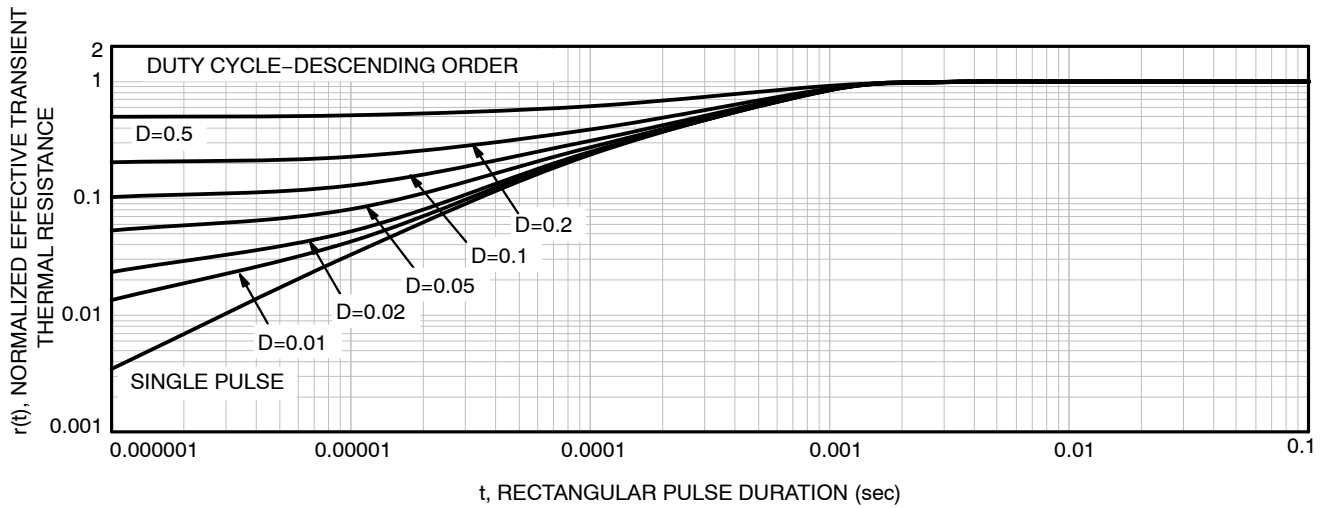
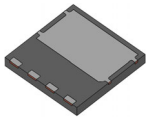
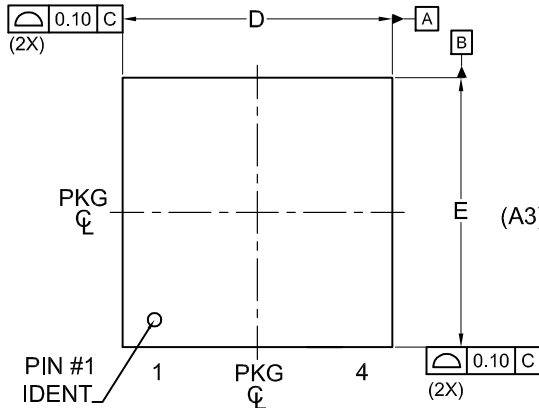


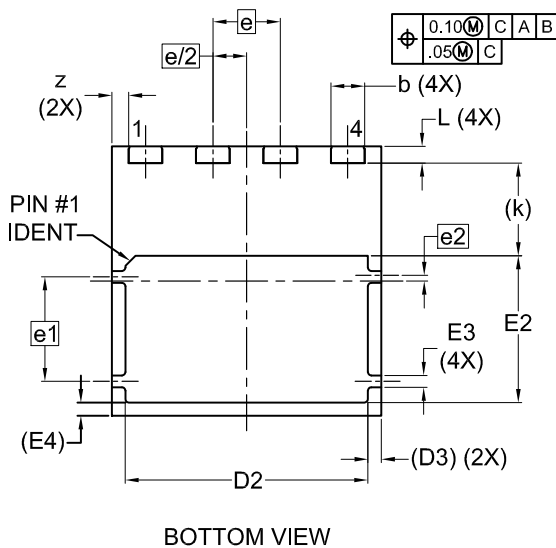
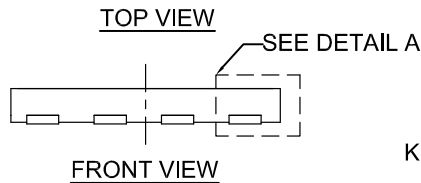
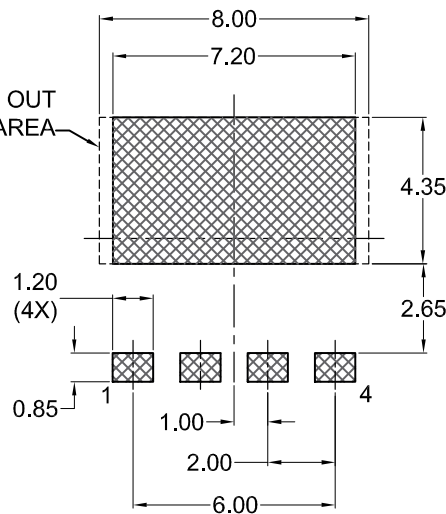
Figure 8. Junction-to-Case Transient Thermal Response


PQFN4 8X8, 2P
CASE 483AP
ISSUE A

DATE 06 JUL 2021


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.
4. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
5. SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.
6. IT IS RECOMMENDED TO HAVE NO TRACES OR VIAS WITHIN THE KEEP OUT AREA.

DETAIL A
SCALE: 2X

KEEP OUT
AREA

LAND PATTERN
RECOMMENDATION

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.90	1.00	1.10
A1	0.00	-	0.05
A3	0.20 REF		
b	0.90	1.00	1.10
D	7.90	8.00	8.10
D2	7.10	7.20	7.30
D3	0.40 REF		
E	7.90	8.00	8.10
E2	4.25	4.35	4.45
E3	0.25	0.35	0.45
E4	0.40 REF		
e	2.00 BSC		
e/2	1.00 BSC		
e1	3.10 BSC		
e2	0.17 BSC		
k	2.75 REF		
L	0.40	0.50	0.60

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DESCRIPTION: PQFN4 8X8, 2P

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