

EcoSPARK[®] 2 Ignition IGBT

320 mJ, 450 V, N-Channel Ignition IGBT

FGD3245G2-F085V

Features

- SCIS Energy = 320 mJ at $T_J = 25^\circ\text{C}$
- Logic Level Gate Drive
- Low Saturation Voltage
- AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant

Applications

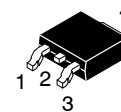
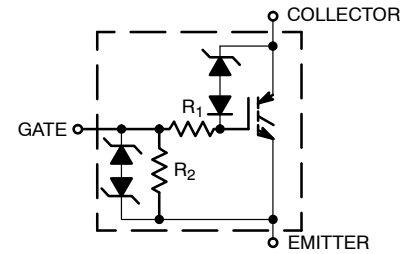
- Automotive Ignition Coil Driver Circuits
- High Current Ignition System
- Coil on Plug Application

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise stated)

Symbol	Parameter	Value	Unit
BV_{CER}	Collector to Emitter Breakdown Voltage ($I_C = 1\text{ mA}$)	450	V
BV_{ECS}	Emitter to Collector Voltage – Reverse Battery Condition ($I_C = 10\text{ mA}$)	28	V
E_{SCIS25}	ISCIS = 14.6 A, L = 3.0 mHy, RGE = 1 K Ω , $T_C = 25^\circ\text{C}$ (Note 1)	320	mJ
$E_{SCIS150}$	ISCIS = 10.9 A, L = 3.0 mHy, RGE = 1 K Ω , $T_C = 150^\circ\text{C}$ (Note 2)	180	mJ
I_{C25}	Collector Current Continuous at $V_{GE} = 4.0\text{ V}$, $T_C = 25^\circ\text{C}$	23	A
I_{C110}	Collector Current Continuous at $V_{GE} = 4.0\text{ V}$, $T_C = 110^\circ\text{C}$	23	A
V_{GEM}	Gate to Emitter Voltage Continuous	± 10	V
PD	Power Dissipation Total, $T_C = 25^\circ\text{C}$	150	W
	Power Dissipation Derating, $T_C > 25^\circ\text{C}$	1.1	W/ $^\circ\text{C}$
T_J, T_{STG}	Operating Junction and Storage Temperature	-55 to $+175$	$^\circ\text{C}$
T_L	Lead Temperature for Soldering Purposes (1/8" from case for 10 s)	300	$^\circ\text{C}$
T_{PKG}	Reflow Soldering according to JESD020C	260	$^\circ\text{C}$
ESD	HBM–Electrostatic Discharge Voltage at 100 pF, 1500 Ω	4	kV
	CDM–Electrostatic Discharge Voltage at 1 Ω	2	kV

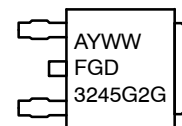
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Self clamped inductive Switching Energy (E_{SCIS25}) of 320 mJ is based on the test conditions that is starting $T_J = 25^\circ\text{C}$, L = 3 mHy, ISCIS = 14.6 A, VCC = 100 V during inductor charging and VCC = 0 V during time in clamp.
2. Self Clamped inductive Switching Energy ($E_{SCIS150}$) of 180 mJ is based on the test conditions that is starting $T_J = 150^\circ\text{C}$, L = 3mHy, ISCIS = 10.9 A, VCC = 100 V during inductor charging and VCC = 0 V during time in clamp.



DPAK (SINGLE GAUGE)
CASE 369C

MARKING DIAGRAM



A = Assembly Location
Y = Year
WW = Work Week
FGD3245G2 = Device Code
G = Pb-Free Package

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

FGD3245G2–F085V

THERMAL RESISTANCE RATINGS

Characteristic	Symbol	Max	Units
Junction–to–Case – Steady State (Drain)	$R_{\theta JC}$	0.9	°C/W

ELECTRICAL CHARACTERISTICS ($T_J = 25^{\circ}\text{C}$ unless otherwise specified)

Symbol	Parameter	Test Conditions	Min	Typ.	Max.	Units
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OFF CHARACTERISTICS

BV _{CER}	Collector to Emitter Breakdown Voltage	I _{CE} = 2 mA, V _{GE} = 0 V, R _{GE} = 1 kΩ, T _J = −40 to 150°C		420	–	480	V
BV _{CES}	Collector to Emitter Breakdown Voltage	I _{CE} = 10 mA, V _{GE} = 0 V, R _{GE} = 0, T _J = −40 to 150°C		440	–	500	V
BV _{ECS}	Emitter to Collector Breakdown Voltage	I _{CE} = −75 mA, V _{GE} = 0 V, T _J = 25°C		28	–	–	V
BV _{GES}	Gate to Emitter Breakdown Voltage	I _{GES} = ±2 mA		±12	±14	–	V
I _{CER}	Collector to Emitter Leakage Current	V _{CE} = 175 V R _{GE} = 1 kΩ	T _J = 25°C	–	–	25	μA
			T _J = 150°C	–	–	1	
I _{ECS}	Emitter to Collector Leakage Current	V _{EC} = 24 V	T _J = 25°C	–	–	1	mA
			T _J = 150°C	–	–	40	
R ₁	Series Gate Resistance			–	120	–	Ω
R ₂	Gate to Emitter Resistance			10K	–	30K	Ω

ON CHARACTERISTICS

$V_{CE(SAT)}$	Collector to Emitter Saturation Voltage	$I_{CE} = 6\text{ A}$, $V_{GE} = 4\text{ V}$, $T_J = 25^{\circ}\text{C}$	–	1.13	1.25	V
$V_{CE(SAT)}$	Collector to Emitter Saturation Voltage	$I_{CE} = 10\text{ A}$, $V_{GE} = 4.5\text{ V}$, $T_J = 150^{\circ}\text{C}$	–	1.32	1.50	V
$V_{CE(SAT)}$	Collector to Emitter Saturation Voltage	$I_{CE} = 15\text{ A}$, $V_{GE} = 5\text{ V}$, $T_J = 150^{\circ}\text{C}$	–	1.64	1.85	V

DYNAMIC CHARACTERISTICS

Q _{G(ON)}	Gate Charge	I _{CE} = 10 A, V _{CE} = 12 V, V _{GE} = 5 V		–	23	–	nC
V _{GE(TH)}	Gate to Emitter Threshold Voltage	I _{CE} = 1 mA V _{CE} = V _{GE}	T _J = 25°C	1.3	1.6	2.2	V
			T _J = 150°C	0.75	1.1	1.8	
V _{GEP}	Gate to Emitter Plateau Voltage	V _{CE} = 12 V, I _{CE} = 10 A		–	2.7	–	V

SWITCHING CHARACTERISTICS

$t_{d(ON)R}$	Current Turn–On Delay Time–Resistive	$V_{CE} = 14\text{ V}$, $R_L = 1\text{ }\Omega$, $V_{GE} = 5\text{ V}$, $R_G = 470\text{ }\Omega$, $T_J = 25^{\circ}\text{C}$	–	0.9	4	μs
t_{rR}	Current Rise Time–Resistive		–	2.6	7	
$t_{d(OFF)L}$	Current Turn–Off Delay Time–Inductive	$V_{CE} = 300\text{ V}$, $L = 1\text{ mH}$, $V_{GE} = 5\text{ V}$, $R_G = 470\text{ }\Omega$, $I_{CE} = 6.5\text{ A}$, $T_J = 25^{\circ}\text{C}$	–	5.4	15	
t_{fL}	Current Fall Time–Inductive		–	2.7	15	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

PACKAGE MARKING AND ORDERING INFORMATION

Device Marking	Device	Package	Reel Diameter	Tape Width	Qty [†]
FGD3245G2	FGD3245G2–F085V	DPAK (Pb–Free)	330 mm	16 mm	2500

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

TYPICAL CHARACTERISTICS

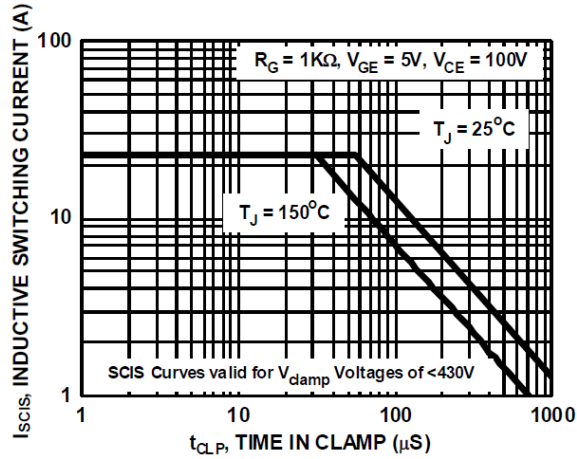


Figure 1. Self Clamped Inductive Switching Current vs. Time in Clamp

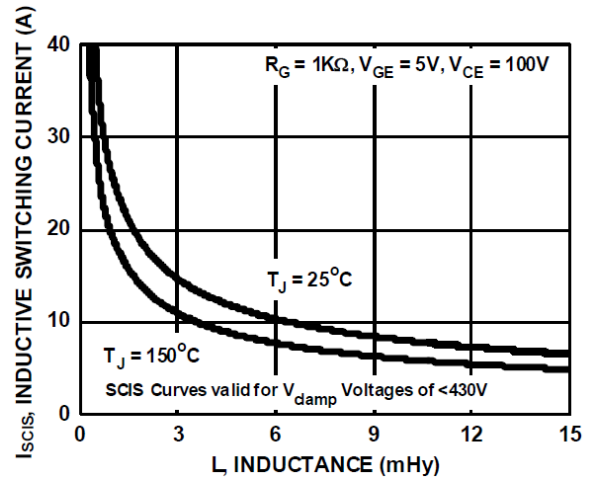


Figure 2. Self Clamped Inductive Switching Current vs. Inductance

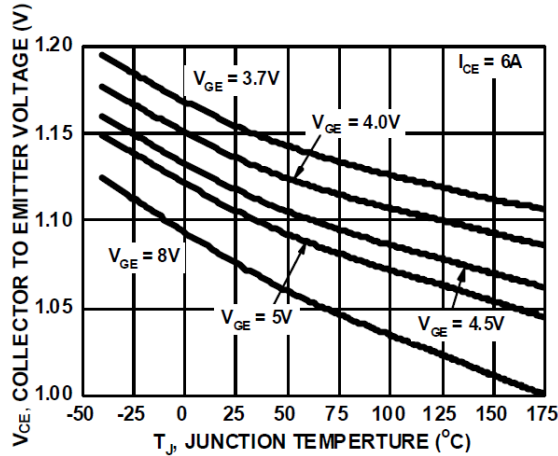


Figure 3. Collector to Emitter On-State Voltage vs. Junction Temperature

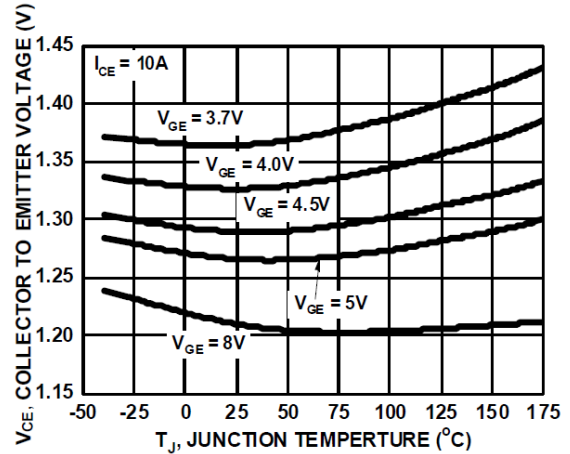


Figure 4. Collector to Emitter On-State Voltage vs. Junction Temperature

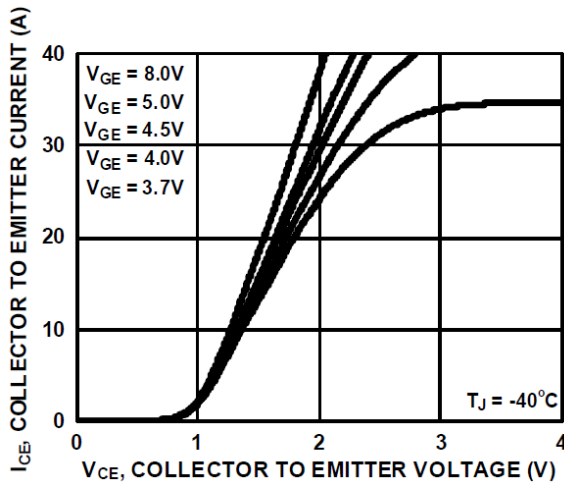


Figure 5. Collector to Emitter On-State Voltage vs. Collector Current

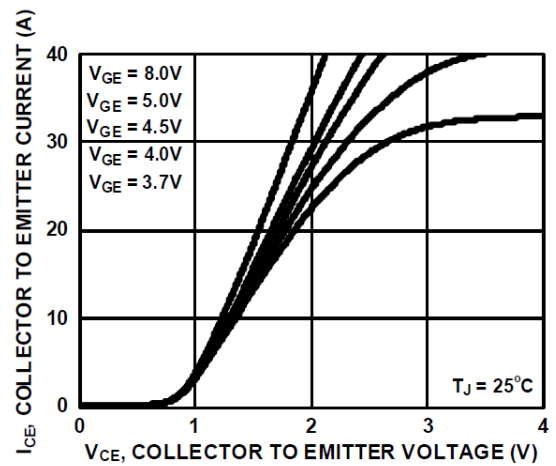


Figure 6. Collector to Emitter On-State Voltage vs. Collector Current

TYPICAL CHARACTERISTICS (continued)

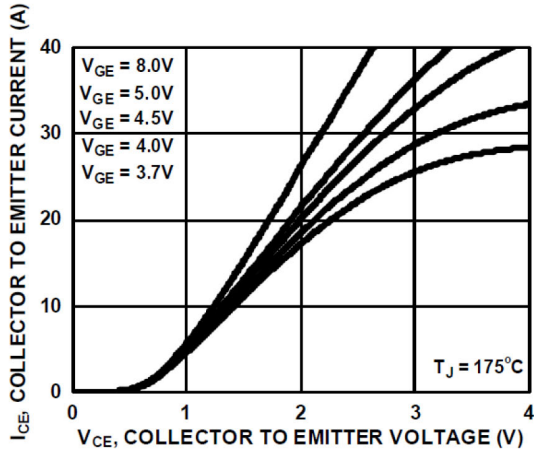


Figure 7. Collector to Emitter On-State Voltage vs. Collector Current

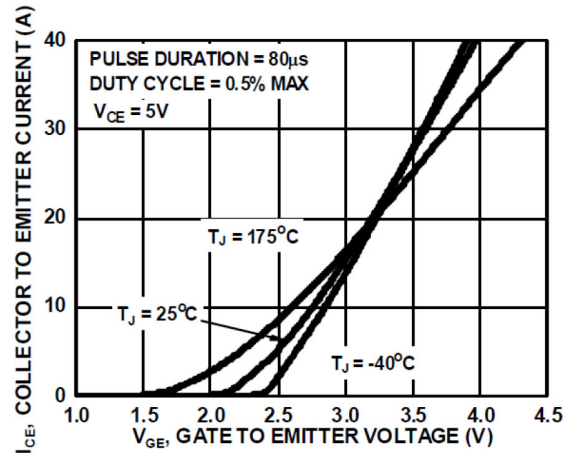


Figure 8. Transfer Characteristics

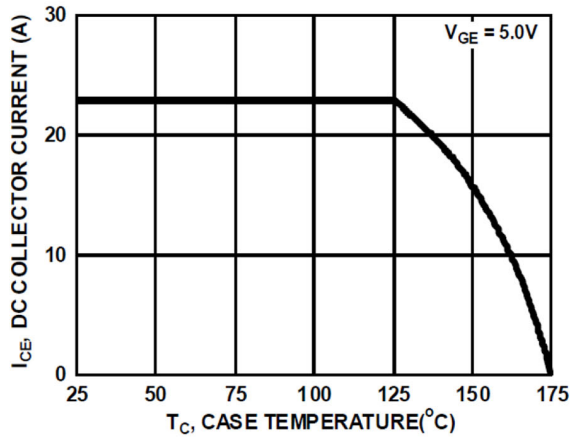


Figure 9. DC Collector Current vs. Case Temperature

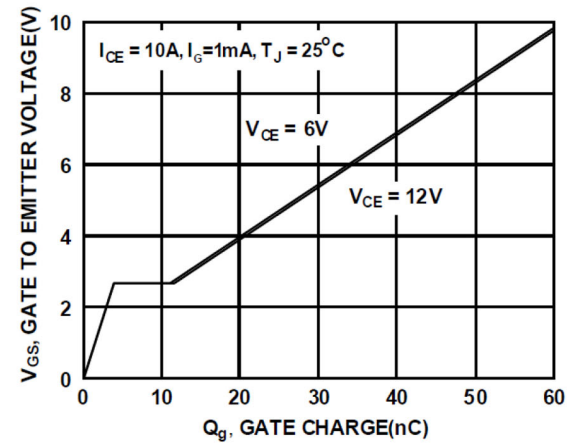


Figure 10. Gate Charge

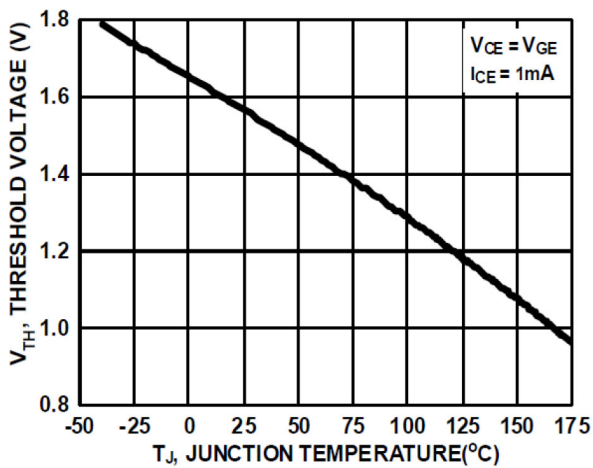


Figure 11. Threshold Voltage vs. Junction Temperature

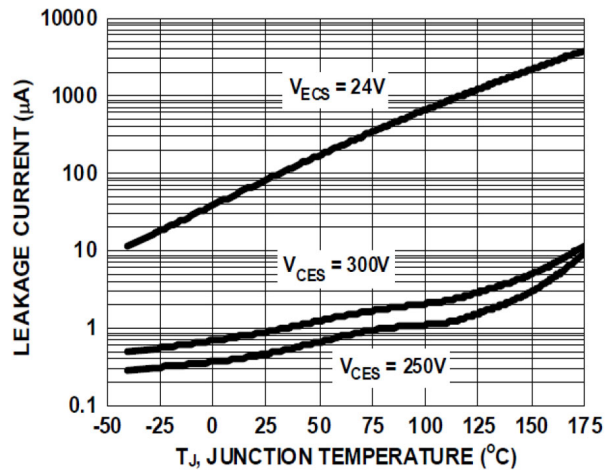


Figure 12. Leakage Current vs. Junction Temperature

TYPICAL CHARACTERISTICS (continued)

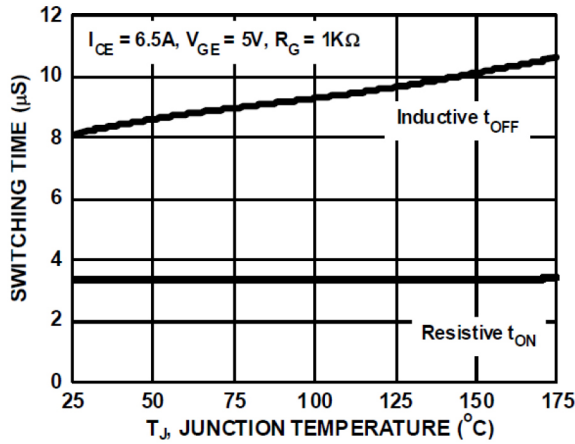


Figure 13. Switching Time vs. Junction Temperature

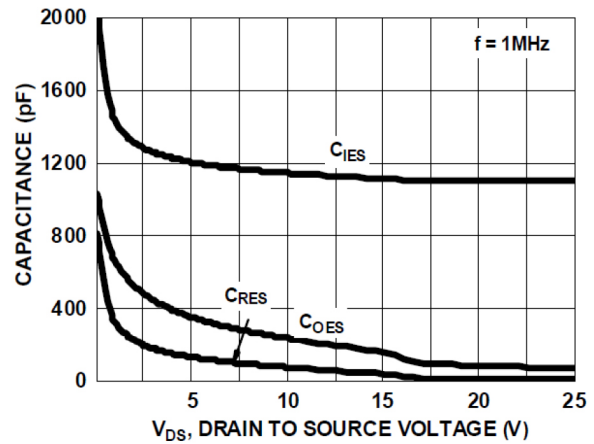


Figure 14. Capacitance vs. Collector to Emitter

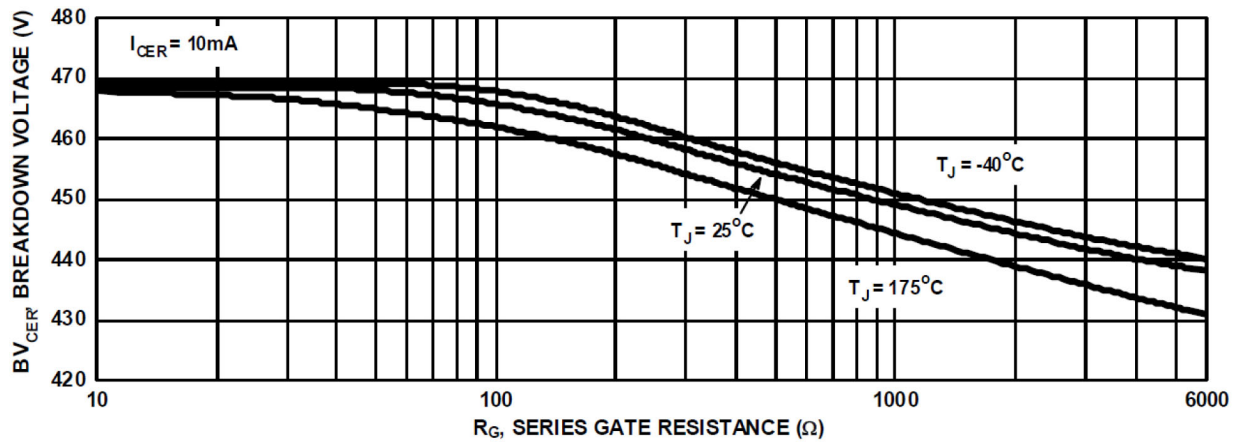


Figure 15. Break Down Voltage vs. Series Resistance

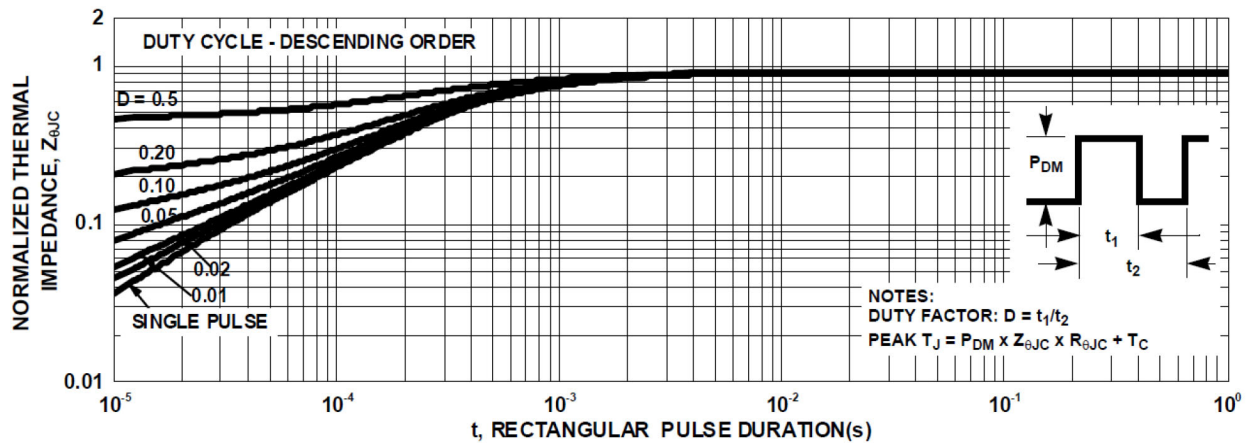


Figure 16. IGBT Normalized Transient Thermal Impedance, Junction to Case

TEST CIRCUIT AND WAVEFORMS

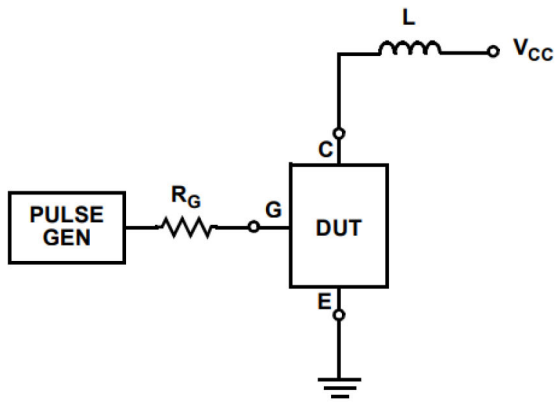


Figure 17. Inductive Switching Test Circuit

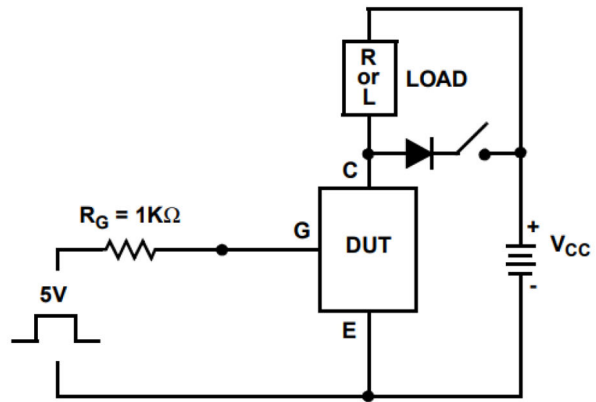


Figure 18. t_{ON} and t_{OFF} Switching Test Circuit

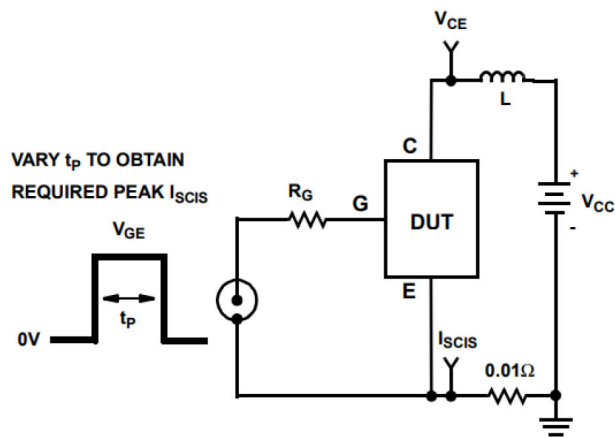


Figure 19. Energy Test Circuit

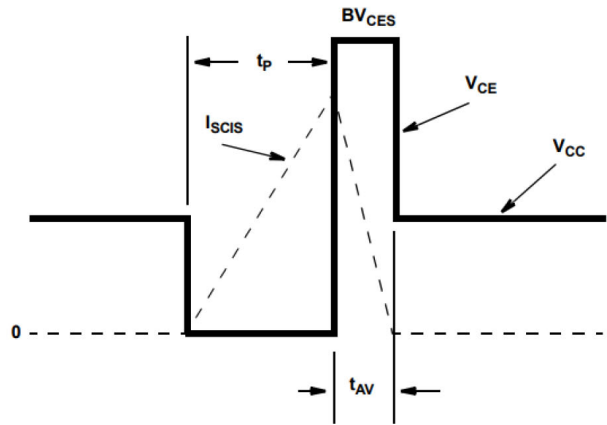


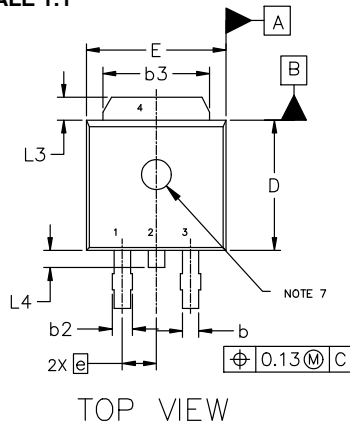
Figure 20. Energy Waveforms



DPAK3 6.10x6.54x2.28, 2.29P
CASE 369C
ISSUE J

DATE 12 AUG 2025

SCALE 1:1



MILLIMETERS			
DIM	MIN	NOM	MAX
A	2.18	2.28	2.38
A1	0.00	---	0.13
b	0.63	0.76	0.89
b2	0.72	0.93	1.14
b3	4.57	5.02	5.46
c	0.46	0.54	0.61
c2	0.46	0.54	0.61
D	5.97	6.10	6.22
E	6.35	6.54	6.73
e	2.29 BSC		
H	9.40	9.91	10.41
L	1.40	1.59	1.78
L1	2.90 REF		
L2	0.51 BSC		
L3	0.89	---	1.27
L4	---	---	1.01
Z	3.93	---	---



NOTES:

1. DIMENSIONING AND TOLERANCING ASME Y14.5M, 2018.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3, AND Z.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15mm PER SIDE.
5. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.
7. OPTIONAL MOLD FEATURE.



RECOMMENDED MOUNTING FOOTPRINT*

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ONSEMI SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERM/D.

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DPAK3 6.10x6.54x2.28, 2.29P
CASE 369C
ISSUE J

DATE 12 AUG 2025

GENERIC
MARKING DIAGRAM*



XXXXXX = Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
WW = Work Week
G = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLE 1: PIN 1. BASE 2. COLLECTOR 3. EMITTER 4. COLLECTOR	STYLE 2: PIN 1. GATE 2. DRAIN 3. SOURCE 4. DRAIN	STYLE 3: PIN 1. ANODE 2. CATHODE 3. ANODE 4. CATHODE	STYLE 4: PIN 1. CATHODE 2. ANODE 3. GATE 4. ANODE	STYLE 5: PIN 1. GATE 2. ANODE 3. CATHODE 4. ANODE
STYLE 6: PIN 1. MT1 2. MT2 3. GATE 4. MT2	STYLE 7: PIN 1. GATE 2. COLLECTOR 3. EMITTER 4. COLLECTOR	STYLE 8: PIN 1. N/C 2. CATHODE 3. ANODE 4. CATHODE	STYLE 9: PIN 1. ANODE 2. CATHODE 3. RESISTOR ADJUST 4. CATHODE	STYLE 10: PIN 1. CATHODE 2. ANODE 3. CATHODE 4. ANODE

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