FLS6617

Primary-Side Regulation PWM with Power MOSFET Integrated

ON Semiconductor®

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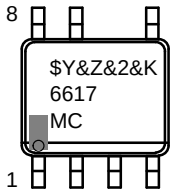
SOIC7
CASE 751ED

MARKING DIAGRAM



$Y	= ON Semiconductor Logo
&Z	= Assembly Plant Code
&2	= Numeric Date Code
&K	= Lot Code
6617	= Specific Device Code

Description

This third−generation Primary Side Regulation (PSR) and highly integrated PWM controller provides several features to enhance the performance of low−power flyback converters. The proprietary TRUECURRENT® technology of FLS6617 enables precise CC regulation and simplified circuit design for battery−charger applications leading to lower−cost, smaller, and lighter chargers, compared to a conventional design or a linear transformer.

To minimize standby power consumption, the proprietary green mode provides off−time modulation to linearly decrease PWM frequency under light−load conditions. Green mode assists the power supply in meeting power conservation requirements.

By using the FLS6617, a charger can be implemented with few external components and minimized cost. A typical output CV/CC characteristic envelope is shown in Figure 1.

Features

- Low Standby Power under 30 mW
- High−Voltage Startup
- Fewest External Component Counts
- Constant−Voltage (CV) and Constant−Current (CC) Control without Secondary−Feedback Circuitry
- Green−Mode: Linearly Decreasing PWM Frequency with Cycle Skipping
- Fixed PWM Frequency at 50 kHz with Proprietary Frequency Hopping to Solve EMI Problem
- Peak−Current−Mode Control in CV Mode
- Cycle−by−Cycle Current Limiting
- V_{DD} Over−Voltage Protection with Auto Restart
- V_{DD} Under−Voltage Lockout (UVLO)
- Gate Output Maximum Voltage Clamped at 15 V
- Fixed Over−Temperature Protection with Auto Restart
- Available in the 7−Lead SOP Package
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Applications

- Battery Chargers for Cellular Phones, Cordless Phones, PDA, Digital Cameras, Power Tools, etc.
- Replaces Linear Transformers and RCC SMPS

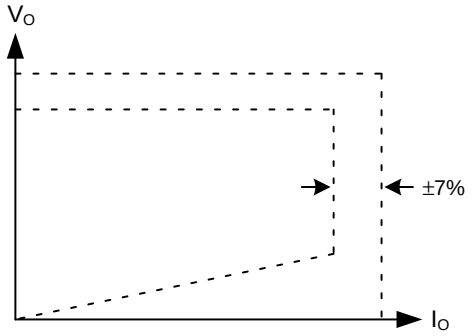


Figure 1. Typical Output V−I Characteristic

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

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ORDERING INFORMATION

Part Number	Operating Temperature Range	Package	Shipping†
FLS6617MX	−40°C to 125°C	SOIC7 (Pb−Free)	2500 Units / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

Application Diagram

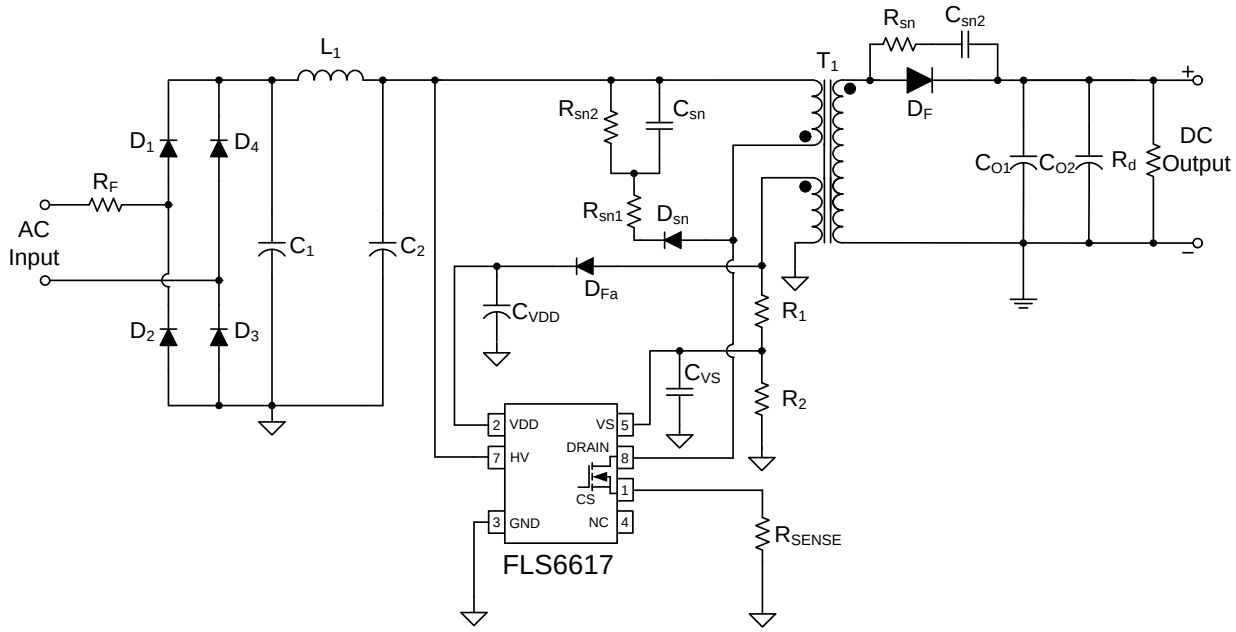

Figure 2. Application Diagram

Internal Block Diagram

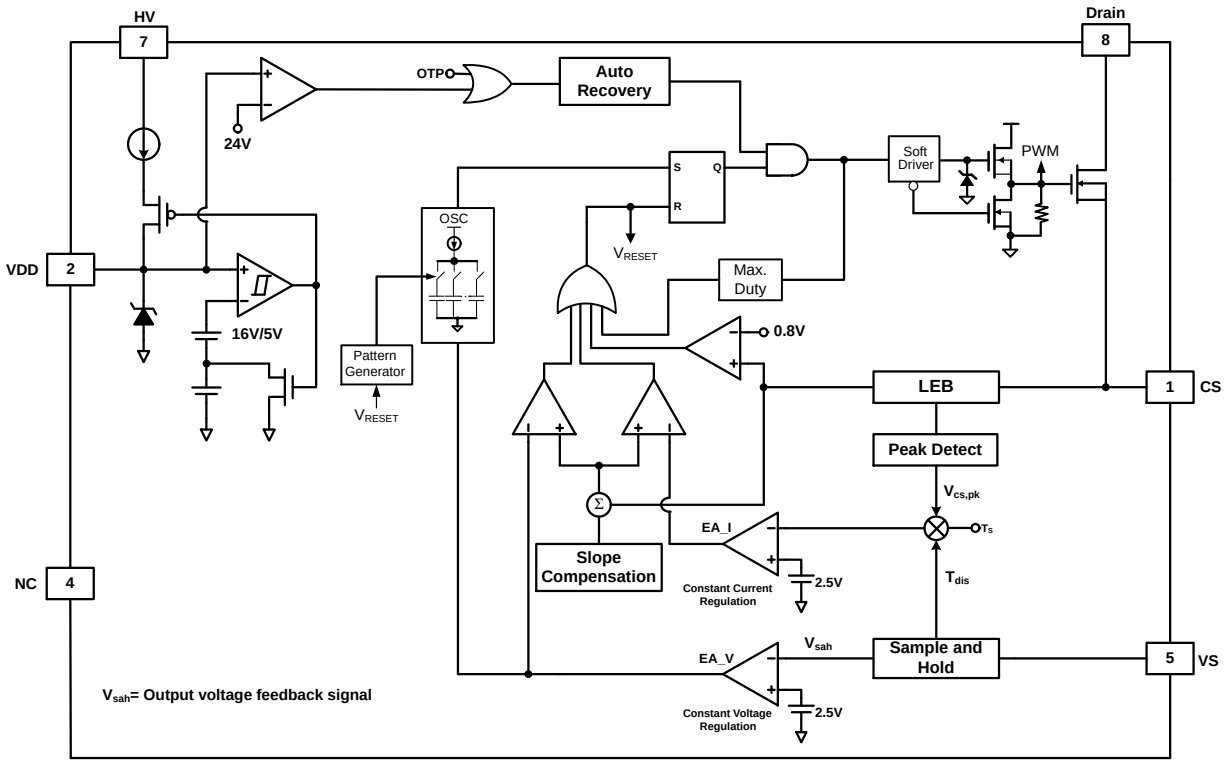

Figure 3. Functional Block Diagram

Pin Configuration

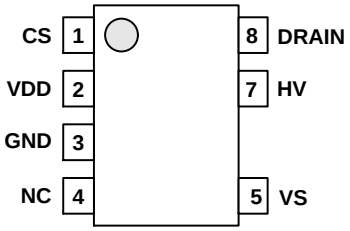

Figure 4. Pin Configuration

PIN DEFINITIONS

Pin #	Name	Description
1	CS	**Current Sense**. This pin connects to current−sense resistor. Detect the MOSFET current for peak−current−mode control in CV mode and provide the output−current regulation in CC mode.
2	VDD	**Power Supply**. IC operating current and MOSFET driving current are supplied through this pin. This pin is connected to an external V_{DD} capacitor of typically 10 μF. The threshold voltages for startup and turn−off are 16 V and 5 V, respectively. The operating current is lower than 5 mA.
3	GND	**Ground**
4	NC	**No Connection**
5	VS	**Voltage Sense**. This pin detects the output voltage information and discharge time based on voltage of auxiliary winding.
7	HV	**High Voltage**. This pin connects to bulk capacitor for high−voltage startup.
8	DRAIN	**Driver Output**. Power MOSFET drain. This pin is the high−voltage power MOSFET drain.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Min.	Max.	Units
V_{HV}	HV Pin Input Voltage			500	V
V_{VDD}	DC Supply Voltage (1, 2)			30	V
V_{VS}	VS Pin Input Voltage		−0.3	6.0	V
V_{CS}	CS Pin Input Voltage		−0.3	6.0	V
V_{COMV}	Voltage Error Amplifier Output Voltage		−0.3	6.0	V
V_{COMI}	Current Error Amplifier Output Voltage		−0.3	6.0	V
V_{DS}	Drain−Source Voltage			700	V
I_D	Continuous Drain Current	T_A = 25°C		1	A
		T_A = 100°C		0.6	A
I_{DM}	Pulsed Drain Current			4	A
E_{AS}	Single Pulse Avalanche Energy			50	mJ
I_{AR}	Avalanche Current			1	A
P_D	Power Dissipation (T_A < 50°C)			660	mW
θ_{JA}	Thermal Resistance (Junction−to−Air)			147	°C/W
Ψ_{JT}	Thermal Resistance (Junction−to−Case)			11	°C/W
T_J	Operating Junction Temperature		−40	+150	°C
T_{STG}	Storage Temperature Range		−55	+150	°C
T_L	Lead Temperature (Wave Soldering or IR, 10 Seconds)			+260	°C
ESD	Electrostatic Discharge Capability (Except HV Pin)	Human Body Model, JEDEC−JESD22_A114	4.0		kV
		Charged Device Model, JEDEC−JESD22_C101	2.0		

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device.
2. All voltage values, except differential voltages, are given with respect to the GND pin.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min.	Max.	Units
T_A	Operating Ambient Temperature	−40	125	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, V_{DD} = 15 V and T_A = 25°C

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{DD} Section						
V_{OP}	Continuously Operating Voltage				23	V
V_{DD-ON}	Turn−On Threshold Voltage		15	16	17	V
V_{DD-OFF}	Turn−Off Threshold Voltage		4.5	5.0	5.5	V
I_{DD-OP}	Operating Current			2.5	5.0	mA
$I_{DD-GREEN}$	Green−Mode Operating Supply Current			0.95	1.2	mA
V_{DD-OVP}	V_{DD} Over−Voltage−Protection Level (OVP)			24		V
$t_{D-VDDOVP}$	V_{DD} Over−Voltage−Protection Debounce Time		90	200	350	μs
HV Startup Current Source Section						
V_{HV-MIN}	Minimum Startup Voltage on HV Pin (3)				50	V
I_{HV}	Supply Current Drawn from HV Pin	V_{AC} = 90 V (V_{DC} = 100 V), V_{DD} = 0 V	1	2.0	5.0	mA
I_{HV-LC}	Leakage Current after Startup	HV = 500 V, $V_{DD}=V_{DD-OFF}+1$ V		0.5	3.0	μA
Oscillator Section						
f_{OSC}	Normal Frequency 1 — Center Frequency	> Vo * 0.78	44	50	56	kHz
	Normal Frequency 1 — Frequency Hopping Range	> Vo * 0.78	±1.6	±3.4	±5.2	kHz
	Normal Frequency 2 — Center Frequency	< Vo * 0.78		36		kHz
	Normal Frequency 2 — Frequency Hopping Range	< Vo * 0.78		±2.5		kHz
$V_{F-JUM-53}$	Frequency Jumping Point	50 kHz → 36 kHz, Vs	1.75	1.95	2.15	V
$V_{F-JUM-35}$	Frequency Jumping Point	36 kHz → 50 kHz, Vs	2.05	2.25	2.45	V
$f_{OSC-N-MIN}$	Minimum Frequency at No−Load		270	395	520	Hz
$f_{OSC-CM-MIN}$	Minimum Frequency at CCM			13		kHz
$V_{S-F-SKIPH}$	COMV Level for High Cycle Skipping Period Change (3)			1.14		V
$V_{S-F-SKIPL}$	COMV Level for Low Cycle Skipping Period Change (3)			0.80		V
$T_{SKIP-CV}$	Cycle skipping period (3)	$V_{S-F-SKIPH}$ < COMV < V_N		240		ms
	Cycle skipping period (3)	$V_{S-F-SKIPL}$ > COMV		160		ms
f_{DV}	Frequency Variation vs. V_{DD} Deviation	V_{DD} = 10 V, 25 V		1	2	%
f_{DT}	Frequency Variation vs. Temperature Deviation	T_A=−40°C to 105°C			15	%
Voltage−Sense Section						
I_{tc}	IC Bias Current			10		μA
$V_{BIAS-COMV}$	Adaptive Bias Voltage Dominated by V_{COMV}	R_{VS} = 20 kΩ		1.4		V
Current−Sense Section						
t_{PD}	Propagation Delay to GATE Output			90	200	ns
t_{MIN-N}	Minimum On Time at No−Load		700	850	1050	ns
V_{TH}	Threshold Voltage for Current Limit			0.8		V
Voltage Error Amplifier Section						
V_{VR}	Reference Voltage		2.475	2.500	2.525	V

ELECTRICAL CHARACTERISTICS (continued)
Unless otherwise specified, V_{DD} = 15 V and T_A = 25°C

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_N	Green−Mode Starting Voltage on EA_V	f_{OSC} = Normal Frequency 1 − 2 kHz		2.5		V
V_G	Green−Mode Ending Voltage on EA_V	f_{OSC} = 1 kHz		0.5		V
Current Error Amplifier Section						
V_{IR}	Reference Voltage		2.475	2.500	2.525	V
Internal MOSFET Section (Note 4)						
DCY_{MAX}	Maximum Duty Cycle		60	75	85	%
BV_{DSS}	Drain−Source Breakdown Voltage	I_D = 250 μA, V_{GS} = 0 V	700			V
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, Referenced to T_A = 25°C		0.53		V/°C
$R_{DS(ON)}$	Static Drain−Source On−Resistance	I_D = 0.5 A, V_{GS} = 10 V		13	16	Ω
I_S	Maximum Continuous Drain−Source Diode Forward Current				1	A
I_{DSS}	Drain−Source Leakage Current	V_{DS} = 700 V, T_A = 25°C			10	μA
		V_{DS} = 560 V, T_A = 100°C			100	
t_{D-ON}	Turn−On Delay Time	V_{DS} = 350 V, I_D = 1 A, R_G = 25 Ω (Note 5)		10	30	ns
t_{D-OFF}	Turn−Off Delay Time			20	50	ns
C_{ISS}	Input Capacitance	V_{GS} = 0 V, V_{DS} = 25 V, f_S = 1 MHz		175	200	pF
C_{OSS}	Output Capacitance			23	25	pF
Over−Temperature Protection Section						
T_{OTP}	Threshold Temperature for OTP (Note 6)			140		°C

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Guaranteed by design.
4. These parameters, although guaranteed, are not 100% tested in production.
5. Pulse test: pulse width ≦ 300 μs, duty cycle ≦ 2%.
6. When the over−temperature protection is activated, the power system enter auto−restart mode and output is disabled.

TYPICAL PERFORMANCE CHARACTERISTICS

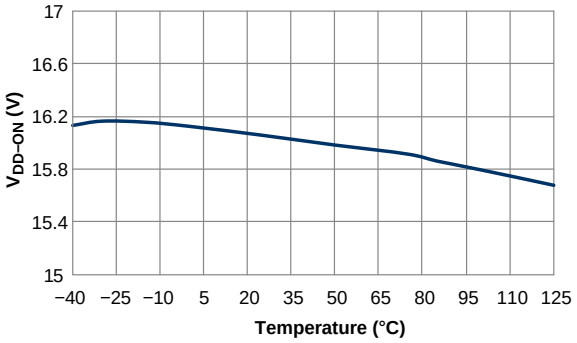

Figure 5. Turn−on Threshold Voltage (V_{DD-ON}) vs. Temperature

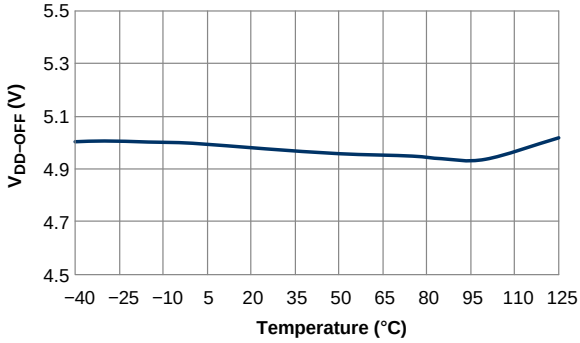

Figure 6. Turn−off Threshold Voltage (V_{DD-OFF}) vs. Temperature

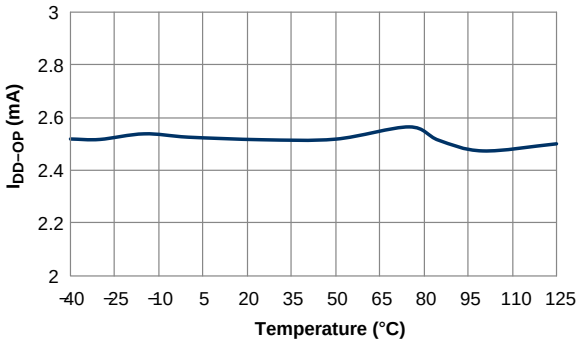

Figure 7. Operating Current (I_{DD-OP}) vs. Temperature

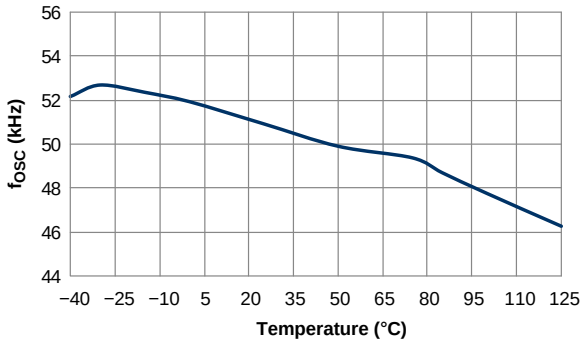

Figure 8. Normal Frequency 1 (f_{OSC}) vs. Temperature

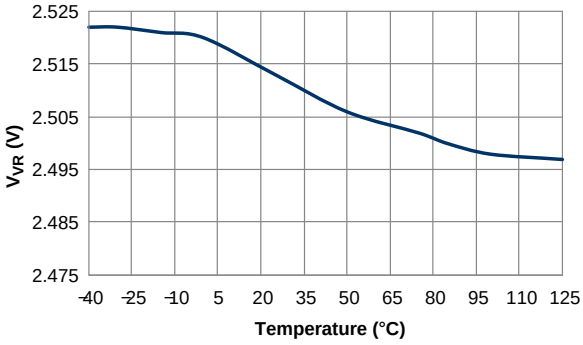

Figure 9. Reference Voltage (V_{VR}) vs. Temperature

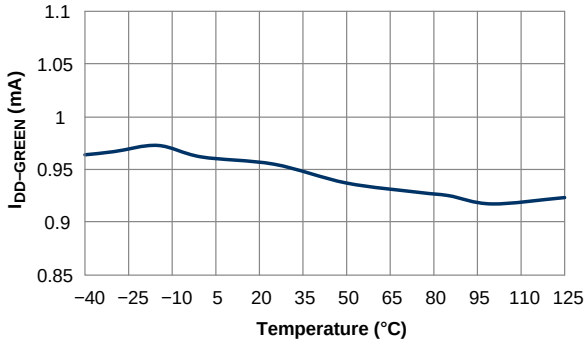

Figure 10. Green Mode Operating Supply Current ($I_{DD-GREEN}$) vs. Temperature

TYPICAL PERFORMANCE CHARACTERISTICS

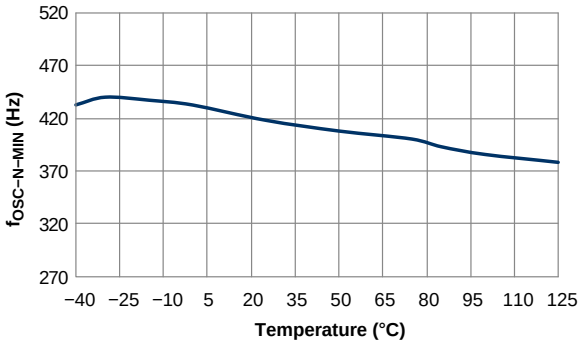

Figure 11. Minimum Frequency at No Load ($f_{OSC-N-MIN}$) vs. Temperature

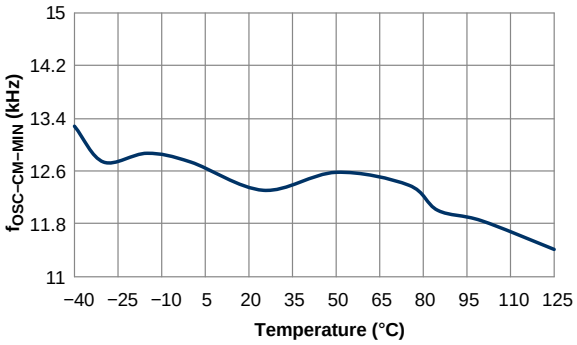

Figure 12. Minimum Frequency at CCM ($f_{OSC-CM-MIN}$) vs. Temperature

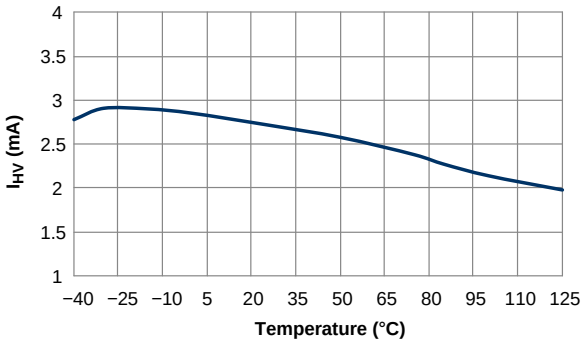

Figure 13. Supply Current Drawn from HV Pin (I_{HV}) vs. Temperature

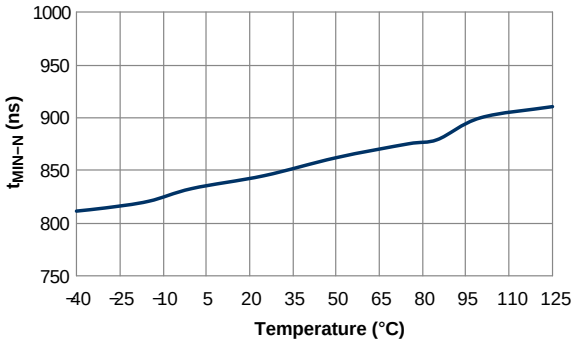

Figure 14. Minimum On Time at No Load (t_{MIN-N}) vs. Temperature

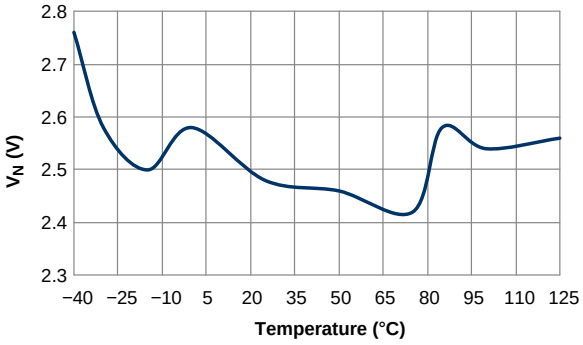

Figure 15. Green Mode Starting Voltage on EA_V (V_N) vs. Temperature

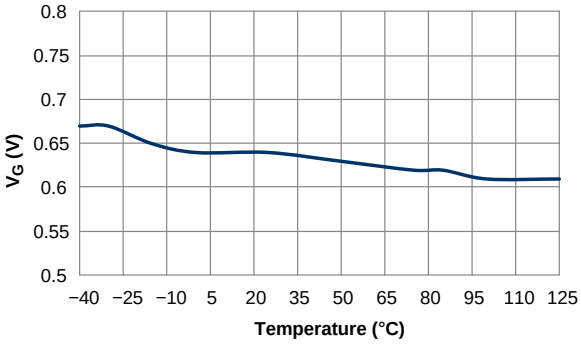

Figure 16. Green Mode Ending Voltage on EA_V (V_G) vs. Temperature

TYPICAL PERFORMANCE CHARACTERISTICS

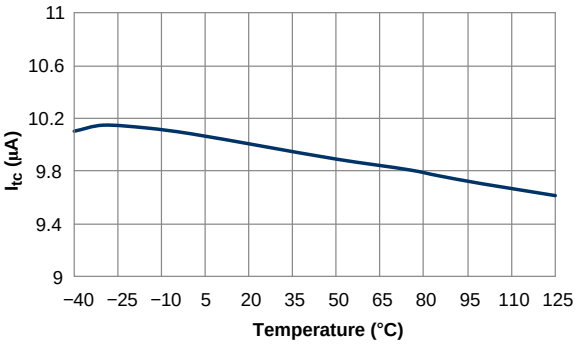

Figure 17. IC Bias Current (I_{tc}) vs. Temperature

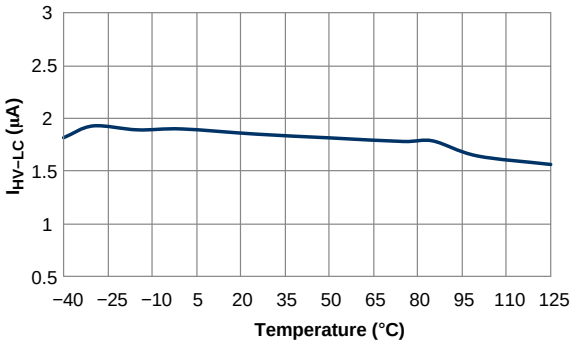

Figure 18. Leakage Current after Startup (I_{HV-LC}) vs. Temperature

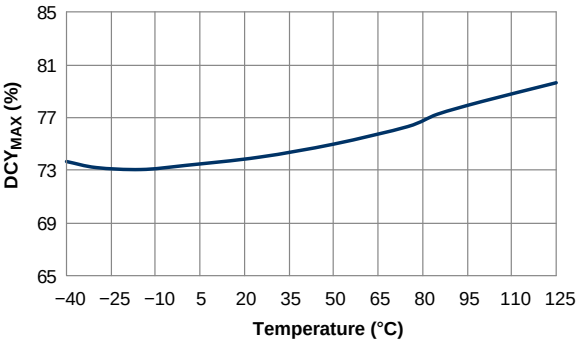

Figure 19. Maximum Duty Cycle (DCY_{MAX}) vs. Temperature

Functional Description

Figure 20 shows the basic circuit diagram of primaryside regulated flyback converter, with typical waveforms shown in Figure 21. Generally, Discontinuous Conduction Mode (DCM) operation is preferred for primary−side regulation because it allows better output regulation. The operation principles of DCM flyback converter are as follows:

During the MOSFET on time (t_{ON}), input voltage (V_{DL}) is applied across the primary−side inductor (L_m). Then MOSFET current (I_{ds}) increases linearly from zero to the peak value (I_{pk}). During this time, the energy is drawn from the input and stored in the inductor.

When the MOSFET is turned off, the energy stored in the inductor forces the rectifier diode (D) to be turned on. While the diode is conducting, the output voltage (V_o), together with diode forward−voltage drop (V_F), is applied across the secondary−side inductor ($L_m \times N_s^2 / N_p^2$) and the diode current (I_D) decreases linearly from the peak value ($I_{pk} \times N_p / N_s$) to zero. At the end of inductor current discharge time (t_{DIS}), all the energy stored in the inductor has been delivered to the output.

When the diode current reaches zero, the transformer auxiliary winding voltage (V_w) begins to oscillate by the resonance between the primary−side inductor (L_m) and the effective capacitor loaded across the MOSFET.

During the inductor current discharge time, the sum of output voltage and diode forward−voltage drop is reflected to the auxiliary winding side as $(V_o+V_F) \times N_a / N_s$. Since the diode forward−voltage drop decreases as current decreases, the auxiliary winding voltage reflects the output voltage best at the end of diode conduction time where the diode current diminishes to zero. Thus, by sampling the winding voltage at the end of the diode conduction time, the output voltage information can be obtained. The internal error amplifier for output voltage regulation (EA_V) compares the sampled voltage with internal precise reference to generate error voltage (V_{COMV}), which determines the duty cycle of the MOSFET in CV mode.

Meanwhile, the output current can be estimated using the peak drain current and inductor current discharge time because output current is same as the average of the diode current in steady state.

The output current estimator identifies the highest value of the drain current with a peak detection circuit and calculates the output current using the inductor discharge time (t_{DIS}) and switching period (t_s). This output information is compared with an internal precise reference to generate error voltage (V_{COMI}), which determines the duty cycle of the MOSFET in CC Mode. With ON Semiconductor's innovative TRUECURRENT technique, constant current (CC) output can be precisely controlled.

Among the two error voltages, V_{COMV} and V_{COMI}, the smaller one determines the duty cycle. Therefore, during constant voltage regulation mode, V_{COMV} determines the duty cycle while V_{COMI} is saturated to HIGH. During constant current regulation mode, V_{COMI} determines the duty cycle while V_{COMV} is saturated to HIGH.

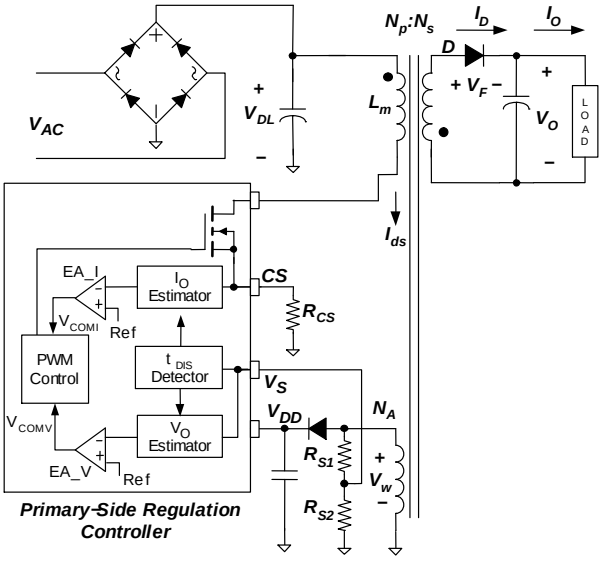

Figure 20. Simplified PSR Flyback Converter Circuit

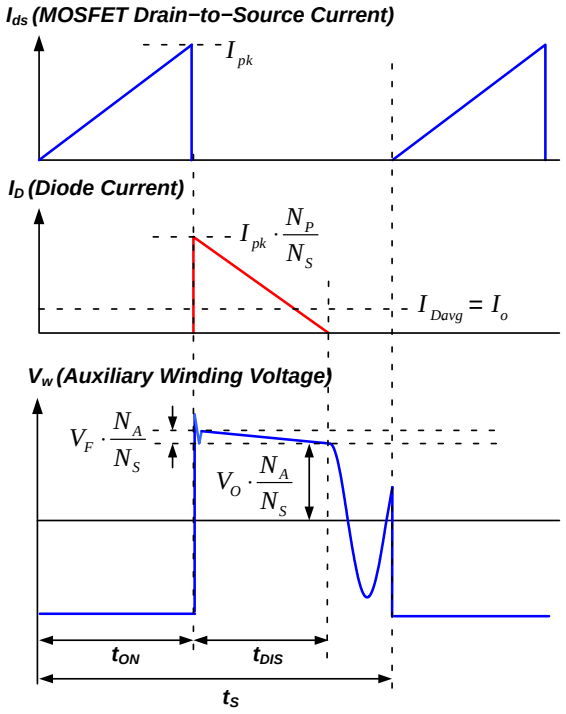

Figure 21. Key Waveforms of DCM Flyback Converter

Operating Current

The FLS6617 operating current is as small as 2.5 mA, which results in higher efficiency and reduces the V_{DD} hold−up capacitance requirement. Once FLS6617 enters “deep” green mode, the operating current is reduced to 0.95 mA, assisting the power supply in meeting power conservation requirements.

Green−Mode Operation

The FLS6617 uses voltage regulation error amplifier output (V_{COMV}) as an indicator of the output load and modulates the PWM frequency as shown in Figure 22. The switching frequency decreases with cycle skipping as the load decreases. In heavy load conditions, the switching frequency is fixed at 50 kHz. Once V_{COMV} decreases below V_N, the PWM frequency linearly decreases with cycle skipping from 50 kHz to reduce switching losses.

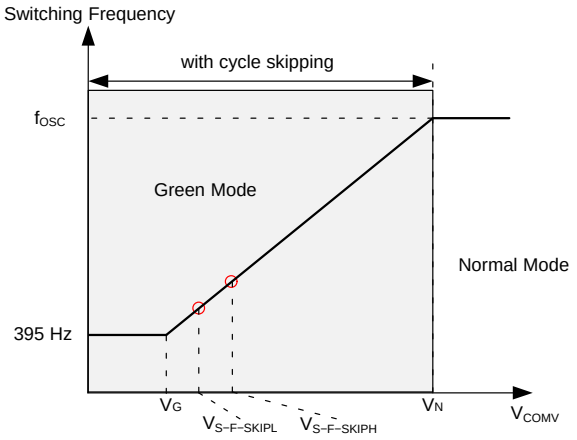

Figure 22. Switching Frequency in Green Mode

Frequency Hopping

EMI reduction is accomplished by frequency hopping, which spreads the energy over a wider frequency range than the bandwidth measured by the EMI test equipment. FLS6617 has a proprietary internal frequency hopping circuit that changes the switching frequency between 44 kHz and 56 kHz.

High−Voltage Startup

Figure 23 shows the HV−startup circuit for FLS6617 applications. The HV pin is connected to the line input or bulk capacitor through a resistor, R_{START} (100 kΩ recommended). During startup status, the internal startup circuit is enabled. Meanwhile, line input supplies the current, $I_{STARTUP}$, to charge the hold−up capacitor, CDD, through R_{START}. When the V_{DD} voltage reaches V_{DDON}, the internal startup circuit is disabled, blocking $I_{STARTUP}$ from flowing into the HV pin. Once the IC turns on, C_{DD} is the only energy source to supply the IC consumption current before the PWM starts to switch. Thus, C_{DD} must be large enough to prevent V_{DD} from dropping down to $V_{DD−OFF}$ before the power can be delivered from the auxiliary winding.

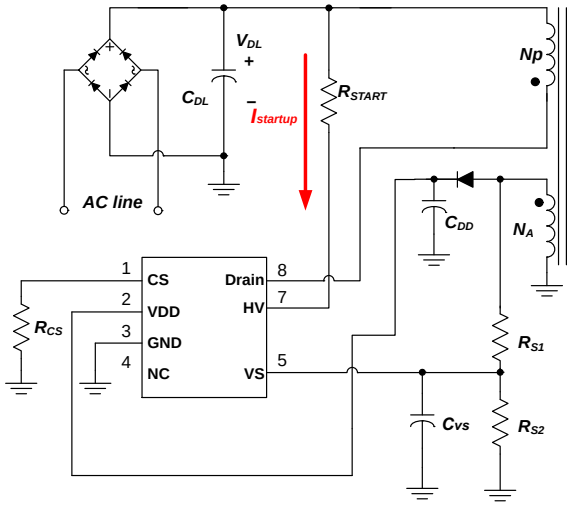

Figure 23. HV Startup Circuit

Under−Voltage Lockout (UVLO)

The turn−on and turn−off thresholds are fixed internally at 16 V and 5 V, respectively. During startup, the hold−up capacitor must be charged to 16 V through the startup resistor to enable the FLS6617. The hold−up capacitor continues to supply V_{DD} until power can be delivered from the auxiliary winding of the main transformer. V_{DD} is not allowed to drop below 5 V during this startup process. This UVLO hysteresis window ensures that hold−up capacitor properly supplies VDD during startup.

Protections

The FLS6617 has several self−protection functions, such as Over−Voltage Protection (OVP), Over−Temperature Protection (OTP), and pulse−by−pulse current limit. All the protections are implemented as auto−restart mode. Once the abnormal condition occurs, the switching is terminated and the MOSFET remains off, causing V_{DD} to drop. When V_{DD} drops to the V_{DD} turn−off voltage of 5 V, internal startup circuit is enabled again and the supply current drawn from the HV pin charges the holdup capacitor. When V_{DD} reaches the turn−on voltage of 16 V, normal operation resumes. In this manner, the auto−restart alternately enables and disables the switching of the MOSFET until the abnormal condition is eliminated (see Figure 24).

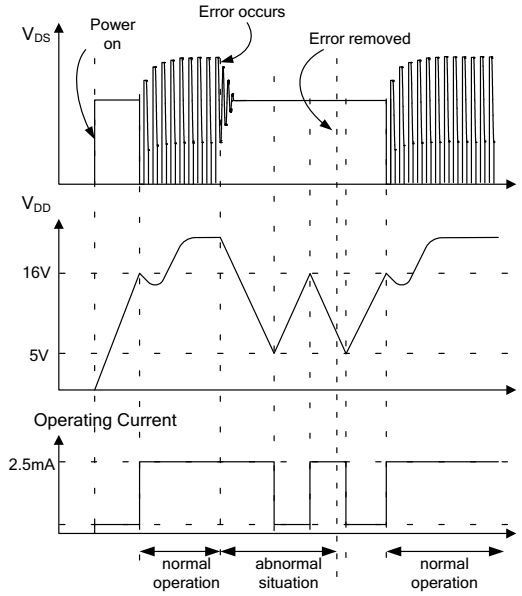

Figure 24. Auto−Restart Operation

V_{DD} Over−Voltage Protection (OVP)

V_{DD} over−voltage protection prevents damage from overvoltage conditions. If the V_{DD} voltage exceeds 24 V at open−loop feedback condition, OVP is triggered and the PWM switching is disabled. The OVP has a debounce time (typically 200 μs) to prevent false triggering due to switching noises.

Over−Temperature Protection (OTP)

The built−in temperature−sensing circuit shuts down PWM output if the junction temperature exceeds 140°C.

Pulse−by−pulse Current Limit

When the sensing voltage across the current−sense resistor exceeds the internal threshold of 0.8 V, the MOSFET is turned off for the remainder of switching cycle. In normal operation, the pulse−by−pulse current limit is not triggered since the peak current is limited by the control loop.

Leading−Edge Blanking (LEB)

Each time the power MOSFET switches on, a turn−on spike occurs at the sense resistor. To avoid premature termination of the switching pulse, a leading−edge blanking time is built in. During this blanking period, the current−limit comparator is disabled and cannot switch off the gate driver. As a result conventional RC filtering can be omitted.

Gate Output

The FLS6617 output stage is a fast totem−pole gate driver. Cross conduction has been avoided to minimize heat dissipation, increase efficiency, and enhance reliability. The output driver is clamped by an internal 15 V Zener diode to protect the power MOSFET transistors against undesired over−voltage gate signals.

Built−In Slope Compensation

The sensed voltage across the current−sense resistor is used for current mode control and pulse−by−pulse current limiting. Built−in slope compensation improves stability and prevents sub−harmonic oscillations due to peak−current mode control. The FLS6617 has a synchronized, positive−slope ramp built−in at each switching cycle.

Noise Immunity

Noise from the current sense or the control signal can cause significant pulse width jitter, particularly in continuous−conduction mode. While slope compensation helps alleviate these problems, further precautions should still be taken. Good placement and layout practices should be followed. Avoiding long PCB traces and component leads, locating compensation and filter components near the FLS6617, and increasing the power MOS gate resistance are advised.

Operation Area

Figure 25 shows operation area. FLS6617 has two switching frequency (f_s) in constant current mode. In order to ensure IC can normally work at DCM under constant current mode, frequency will jump to lower level (36 kHz) when system is operated at low output voltage.

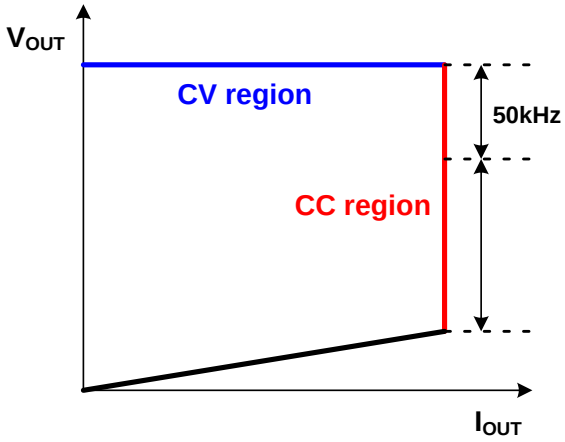

Figure 25. Operation Area

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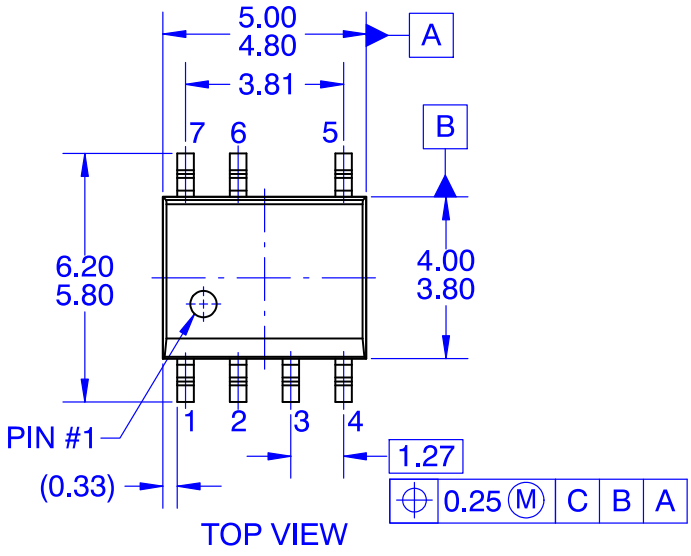
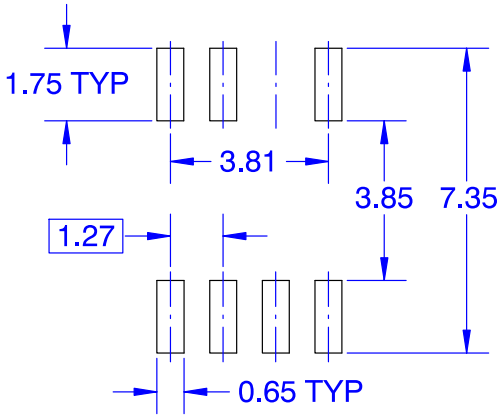
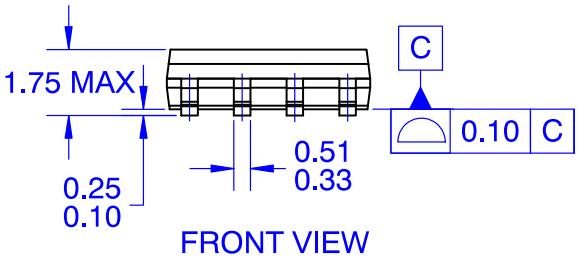


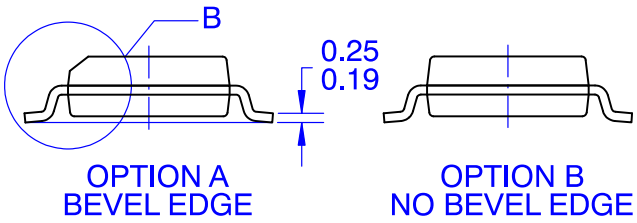
TOP VIEW



LAND PATTERN RECOMMENDATION



FRONT VIEW

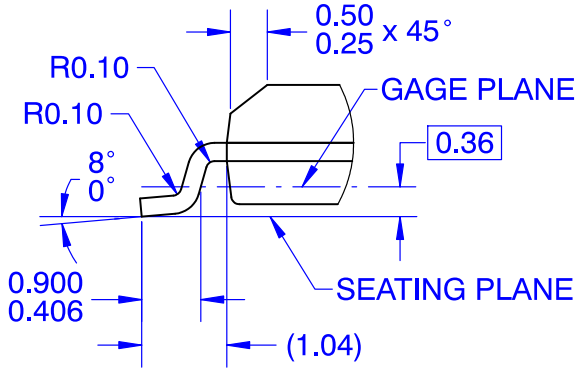


OPTION A
BEVEL EDGE

OPTION B
NO BEVEL EDGE

SIDE VIEW

NOTES:
A. THIS PACKAGE DOES NOT FULLY CONFORM TO JEDEC MS−012, VARIATION AA
B. ALL DIMENSIONS ARE IN MILLIMETERS
C. DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS



DETAIL B
SCALE 2:1

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